UNIVERSIDADE FEDERAL DO PARANÁ

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STUDY AND DESIGN OF AN IMPULSE RADIO UWB SYNTHESIZER FOR 3.1-10.6 GHZ BAND IN 28 NM CMOS FD-SOI TECHNOLOGY

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Dissertação apresentada no Programa de Pós-Graduação em Engenharia Elétrica, Setor de Tecnologia, Universidade Federal do Paraná como requisito parcial à obtenção do grau de Mestre em Engenharia Elétrica.

Orientador: Prof. Ph.D. André Augusto Mariano
Coorientador: Prof. Ph.D. Rémy Vauche

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RESUMO

Este trabalho de dissertação de mestrado apresenta o estudo e desenvolvimento de sintetizador de pulsos de rádio ultra banda larga para a banda 3,1-10,6 GHz em tecnologia 28 nm CMOS FD-SOI. A primeira utilização dessa banda de frequência foi autorizada pela comissão federal de comunicações dos Estados Unidos em 2002. Visando a explorar essa banda de frequência, o padrão IEEE 802.15.4 escolheu as comunicações baseadas em pulsos de rádio em detrimento das comunicações tradicionais de banda estreita. Uma linha importante de pesquisa é o estudo e desenvolvimento de um transmissor ultra bandalarga, capaz de endereçar múltiplas bandas e múltiplos padrões diferentes, que é consistido em um sintetizador de pulsos de rádio devendo ter a capacidade de cobrir a banda 3,1-10,6 GHz. Para atingir tal objetivo, visa-se à implementação de uma arquitetura versátil baseada em um gerador de pulsos constituído principalmente por um oscilador controlado por tensão, e um circuito de formatação da envoltória do pulso, em que é possível fazer ajuste da duração e da frequência central dos pulsos, e compensar variações PVT (Processo, Tensão e Temperatura). O objetivo principal deste trabalho de dissertação de mestrado é estudo e desenvolvimento de um sintetizador de pulsos baseado nessa arquitetura em tecnologia 28 nm CMOS FD-SOI, de maneira que esse circuito seja capaz de cobrir toda banda 3.1-10.6 GHz e ao mesmo tempo cumprir os requerimentos espectrais estabelecidos pelos padrões IEEE 802.15.4 e IEEE 802.15.6. No projeto do circuito proposto, utilizou-se a técnica de síntese de pulso por transposição de frequência, constituído principalmente por um oscilador local comutado, permitindo a redução do consumo de energia, em que o sinal produzido pelo oscilador é modulado por um pulso em banda base. Em relação à metodologia do projeto, trata-se de um projeto totalmente personalizado, em que se utilizou as logicas CMOS e CML (Lógica Diferencial), e se considerou capacitâncias parasitas estimadas no intuito de melhorar o dimensionamento dos transistores. A arquitetura do oscilador escolhida neste projeto foi o oscilador em anel, a qual permite de se obter uma banda de frequência suficientemente alta. Acerca da formatação do pulso, escolheu-se uma envoltória possível de se implementar com circuito digital reprogramável, visando a endereçar os diferentes canais do padrão IEEE 802.15.4 e IEEE 802.15.6. O sistema implementado, em nível de esquemático de transistor considerando capacitâncias parasitas estimadas, apresenta um desempenho satisfatório sobre a toda a banda de frequência de interesse, em que os pulsos gerados respeitam os gabaritos espectrais impostos pelos padrões IEEE, evidenciando a capacidade do circuito prosposto de ser multi-banda e cobrir toda a banda de frequencia de interesse. Em relação ao consumo de potencia, esse é influenciado pela duração do pulso e sua frequência central. Ademais, obteve-se um consumo de potência estática 14 μW e um consumo de energia por pulso emitido maximo de 308 pJ, em que para esse caso, o

pulso apresenta um energia transmitida de 11,7 pJ por pulso, assim apresentando uma eficiência de 3,8 %.

Palavras-chaves: Gerador de Pulsos. Máscaras espectrais. Padrões IEEE. Pulso de Rádio. Ultra bandalarga.

ABSTRACT

This dissertation work concerns the study and design of an impulse radio ultra-wide band synthesizer for 3.1-10.6 GHz frequency band in 28 nm CMOS FD-SOI technology. Indeed, this frequency band exploitation was initially authorized by the federal communications commission of United States in 2002. Targeting to exploit this frequency band, the IEEE 802.15.4 standard has chosen the communications based on impulse radio instead of the traditional narrowband communications. Besides, the impulse radio communications should respect communications standards, like the IEEE 802.15.4 for wireless personal networks, or IEEE 802.15.6 for wireless body networks. These IEEE standards define the generated pulse bandwidth and its central frequency. An important line of research is the study and design of a multi-standard or multi-band UWB transmitter, consisted by a pulse synthesizer that should be able to address all the standardized channels. To accomplish this, a proposed solution reposes on design of versatile architecture based on pulse generator and an envelope shaping circuit, where it is possible to tune the pulse duration and central frequency, and also to compensate PVT variations (Process, Voltage and Temperature). The dissertation work main goal is the study and design of a pulse synthesizer based on this architecture in 28 nm CMOS FD-SOI technology, such that the designed system is capable to cover all the 3.1-10.6 GHz and at same time to comply the spectral requirements established by IEEE 802.15.4 and 802.15.6 standards. In relation of the proposed circuit design, it is applied the pulse synthesis technique based on frequency transposition, that is mainly composed by a local oscillator that can be turned on and off, which allows to reduce the power consumption. The generated oscillation is modulated by a baseband pulse. Concerning the design methodology, it is a full-custom project, where CMOS and CML logics were used, and estimated parasitic capacitances were considered to achieve more reliable transistor sizing. The oscillator architecture chosen is based on ring oscillator, which allows to reach a frequency range sufficiently large. For the pulse shaping, it was chosen a envelope that is feasible to implement with fully digital circuit, targeting to address all IEEE 802.15.4 and IEEE 802.15.6 standard channels. The implemented system presents, in schematic levels considering parasitic capacitances, a satisfactory performance over all the 3.1-10.6 GHz band, where the generated pulses respect the spectral requirements imposed by the IEEE standards, therefore indicating that the proposed circuit is multi-band and able to cover all frequency band of interest. In terms of power consumption, it was achieved a power leakage of 14 μW and a maximal energy per pulse consumption of 308 pJ, where for this case, the pulse has an emitted energy of 11.7 pJ per pulse, therefore a efficiency of 3.8 %.

Key-words: IEEE standards, Impulse Radio. Low-power. Pulse Generator. Spectral masks. Ultra-Wideband.

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LIST OF ABBREVIATIONS AND ACRONYMS

ANATEL The National Telecommunications Agency of Brazil

BPSK Binary Phase Shift Keying Modulation

CEPT Conference of Postal and Telecommunications Administrations

CML Current Mode Logic

CMOS Complementary Metal Oxide Semiconductor

DB-DCO Dual-band Digitally Controlled Oscillator

DCA Digitally Controlled Amplifier

DCO Digitally Controlled Oscillator

ECC Electronic Communications Committee

EIRP Equivalent Isotropically Radiated Power

FCC Federal Communication Commission

FD-SOI Fully Depleted Silicon On Insulator

FM-UWB Frequency Modulation Ultra-Wide Band

FinFET Fin Field-effect Transistor

IEEE Institute of Electrical and Electronics Engineers

IR Impulse Radio

IoT Internet of Things

LFS Low Frequency Signal

LNA Low Noise Amplifier

LP-WPAN Low Power Wireless Personal Area Networks

MOS Metal Oxide Semiconductor

OOK Off-On Keying Modulation

PA Power Amplifier

PAM Pulse Amplitude Modulation

PD Power Down

PDB Power Up

PSD Power Spectral Density

PVT Process, Voltage and Temperature

RF Radio Frequency

SNR Signal Noise Ratio

UMTS Universal Mobile Telecommunications System

UTBB Ultra-thin Body and Buried Oxide

UWB Ultra-Wide Band

VCDL Voltage Controlled Delay Line

VCO Voltage-Controlled Oscillator

VCRO Voltage-Controlled Ring Oscillator

WBAN Wireless Body Area Network

WLAN Wireless Local Area Network

WSN Wireless Sensor Network

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1 INTRODUCTION

1.1 CONTEXT

Since the development of the first integrated circuits, that has been held around 60 years ago, the integrated circuits and its transistors have become more compact in order to meet an increasing demand of higher data rate, lower power consumption and better battery autonomy. Besides, the rise of Internet of Things (IoT) and the 5G communications, along with the growing number of devices connected to WSN, WPAN and WBAN will require wireless systems capable to offer high data rate with low error rate and low latency within short and medium range applications like smart cars, medical imaging, vehicular radar, sensor networks, brain-machine interface and surveillance systems (WANG; WANG, 2013; KIM; CHOI; KIM, 2020).

These systems present a challenging circuit design due to IEEE standard spectral restrictions and several trade-offs, like low complexity, compact chipset and low power consumption. For nanometer scale integrated circuits, there are two interesting technologies that have been studied, being an alternative to traditional bulk CMOS technology: The Fully Depleted Silicon on Insulator (FD-SOI) and the fin field-effect transistor (FinFET).

The Federal Communication Comission (FCC) has authorized in 2002 the exploitation of 3.1-10.6 GHz frequency band for Ultra-Wide Band (UWB) communications (COMMISSION, 2002). They have the particularity to spread the signal energy on a frequency bandwidth of order of GHz. Since then, several standards for this frequency band were defined, especially IEEE 802.15.4 and IEEE 802.15.6, which have chosen Ultra-Wide Band Impulse Radio (IR-UWB) rather than traditional narrowband carrier modulations to exploit the 3.1-10.6 GHz band (OPPERMANN; HÄMÄLÄINEN; IINATTIN, 2004). The IR-UWB is a technique that consists of transmission of low duty-cycle short pulses, typically in the order of nanoseconds. Moreover, for impulse modulations the emitted power spectral density is directly proportional to the modulus squared of the emitted pulse spectrum. The IR-UWB is pretty suitable for wireless sensor networoks (WSN), wireless personal area networks (WPAN) and wireless body area networks (WBAN) applications, thus being an interesting and promising technology (GOAVEC et al., 2017).

The IR-UWB signals present a high energy efficiency due to its gated cycled nature, which allows the transmitter chain, especially the core of the pulse generator, to be turned on only during an IR-UWB pulse transmission (HAAPALA; HALONEN, 2018). In a case of a farther distance targeted, the output voltage amplitude and the transmitted

pulse energy should be stronger, therefore the driver transistors in the transmitter circuit should become larger, such that leakage current will become more significant, which is inconvenient of UWB projects.

The IR-UWB technique can be seen as the multiplication of a baseband pulse by a carrier, where the baseband pulse envelope must be shaped to match regional regulations spectral requirements and spectral masks imposed by IEEE Standards (BOURDEL et al., 2010). Also, the IEEE standards define several channels, each one having a different central frequency and bandwidth, that can be used on the IR-UWB signal transmission for particular applications.

1.2 MOTIVATIONS

The IR-UWB communications have been studied because they are an interesting solution to data transmission with high data-rate and low power within small and medium coverage areas. In particular, the design of multi-standard and multi-band transmitters has become an important research topic, where these transmitters are based on a pulse synthesizer capable to cover all the frequency band regulated by the FCC and to compensate Process, Voltage and Temperature (PVT) variations (VAUCHE, 2011). The presented work is a continuation of the research work done in (MUHR, 2016; SCHOULTEN, 2020). The achieved results in these works were used as a starting point for circuit design in this work.

In the literature, several published works present UWB pulse generator in bulk CMOS technology using either direct pulse synthesis or frequency transposition pulse synthesis techniques. In relation of direct pulse synthesis technique, the pulse is directly generated within the frequency band of interest using an architecture based on delay lines (KIM; PARK; JOO, 2004). On the other hand, for the frequency transposition pulse synthesis, a baseband pulse modulates a voltage-controlled oscillator (VCO), where the reported architectures are based on mixers, LC-tank oscillators and ring oscillators. These oscillators can be turned off during two consecutive generated pulses transmission, thereby saving power. The UWB transmitter based on delay lines is able to generate pulses with a central frequency range around 4 GHz, which is not enough to cover all the 3.1-10.6 GHz (VAUCHE; MUHR; FOURQUIN et al., 2017; HAAPALA; HALONEN, 2018; MIRANDA; MENG, 2010). Meanwhile, regarding the UWB transmitters using a local gated oscillator, the ones composed by mixers presents a narrow range of pulse central frequency (2 GHz) and higher power leakage (MIR-MOGHTADAEI et al., 2014). UWB transmitters composed by LC oscillators also produce pulses with a not large range of central frequency, however they present a low power leakage (5 μW) (DOKANIA, R. et al., 2010; PHAN et al., 2008; SCHMICKL; FASETH; PRETL, 2020). Finally, UWB transmitters based on ring oscillators are able to cover a

larger pulse central frequency range and produces pulses that can address a larger number of the IEEE 802.15.4 and IEEE 802.15.6 standardized channels (ZHAO; LI; WU, 2013; RYCKAERT et al., 2007; STREEL et al., 2017).

Nevertheless, in this dissertation, a pulse generator that covers entirely the 3.1-10.6 GHz frequency band and address all IEEE 802.15.4 and 802.15.6 channels is intended, or in other words, a multi-standard and multi-channel pulse generator. An interesting UWB transmitter is the one based on ring oscillator, that are able to cover a larger frequency band and allows a less complex control of the generated pulse duration. Therefore, a feasible option is an architecture based on ring gated oscillator, whose frequency is tuned by controlling the cells delay through transistor gate voltage biasing, with an envelope shaping circuit. Most reported pulse generators implemented in bulk CMOS technologies (65 nm or greater) presented difficulties to cover entirely the 3.1-10.6 GHz frequency band. The UWB transmitter reported in (SCHMICKL; FASETH; PRETL, 2020) was able to cover this frequency band, however not able to address all IEEE 802.15.4 standardized channels, mostly the channels with larger bandwidth. Meanwhile, the 28 nm FD-SOI technology is a potential solution to cover the targeted band, address all the IEEE 802.15.4 and 802.15.6 standardized channels, and to achieve a lesser power consumption (STREEL et al., 2017).

1.3 OBJECTIVES

1.3.1 General

The general objective of this dissertation is to develop, test and validate a pulse synthesizer circuit using an architecture based mainly on ring oscillator and envelope shaping circuit, employing 28 nm CMOS FD-SOI technology.

1.3.2 Specific

The specific objectives of this dissertation are:

- The pulse generator design
- The digitally controlled amplifier design (DCA)
- The envelope shaping circuit design, having an architecture with the lowest power consumption
- The dual-band digitally controlled oscillator design (DB-DCO)
- The memory for data storage design
- Schematic simulations of pulse synthesizer taking into account possible parasite capacitances addressing several IEEE standardized channels

- Verify in simulations if the final circuit is able to fully comply the spectral requirements imposed by FCC regulations and IEEE standards
- Calculate from simulations the leakage power and the energy per pulse consumption of the final circuit
- Comparison of the proposed IR-UWB pulse synthesizer with UWB transmitters reported in literature

1.4 STRUCTURE

Chapter 2 addresses the UWB communications. It presents the UWB regulations from the United States, Europe and Brazil, and an overview of IEEE 802.15.4 and IEEE 802.15.6 standards. Besides, it presents the basic concepts of UWB signals, the Impulse Radio UWB communications, the IR-UWB pulse generation principle and some pulse envelopes reported in the literature.

Chapter 3 addresses the state of the art. It presents the two pulse synthesis methods reported in literature, which are the direct synthesis and synthesis by frequency transposition.

Chapter 4 addresses the proposed circuit design. Firstly, a system overview is done and the FD-SOI technology is introduced. Then, the IR-UWB pulse synthesizer top-down design are presented, where for some parts of proposed system, more than one architecture is studied.

Chapter 5 addresses the developed final circuit obtained results. Firstly, parametric simulations are presented, and secondly some pulse transmission study cases are approached, addressing several IEEE 802.15.4 standardized channels, where the leakage power and drained energy per pulse from the final circuit are presented and discussed. A comparison with the state of art is made.

Chapter 6 addresses the dissertation conclusion and future perspectives.

2 UWB COMMUNICATIONS

Since the Ultra-Wide Band (UWB) communications within between 3.1 GHz and 10.6 GHz frequency band have been regulated by the First Report and Order published by Federal Communication Commission of the United States (FCC) in 2002, several standards exploiting this frequency band have been defined as well as several works have been published pointing the great capability of UWB to provide short and medium-range communications with a high-quality transfer data and low-power spectral density, thereby not disturbing the conventional narrowband radio systems operating in the adjacent channels (COMMISSION, 2002). The UWB has the particularity to spread the signal energy on a frequency bandwidth of the order of GHz, unlike the narrowband signal, that exploits usual carrier modulations (Fig. 1) (OPPERMANN; HÄMÄLÄINEN; IINATTIN, 2004). Indeed, as can be seen in Figure 2, the narrowband systems based on GPS, Universal Mobile Telecommunications System (UMTS), Bluetooth, Wi-Fi, 802.11.b and WLAN 802.11.a occupy a narrower frequency spectrum than UWB communication but present a stronger emitted signal power for a given application.

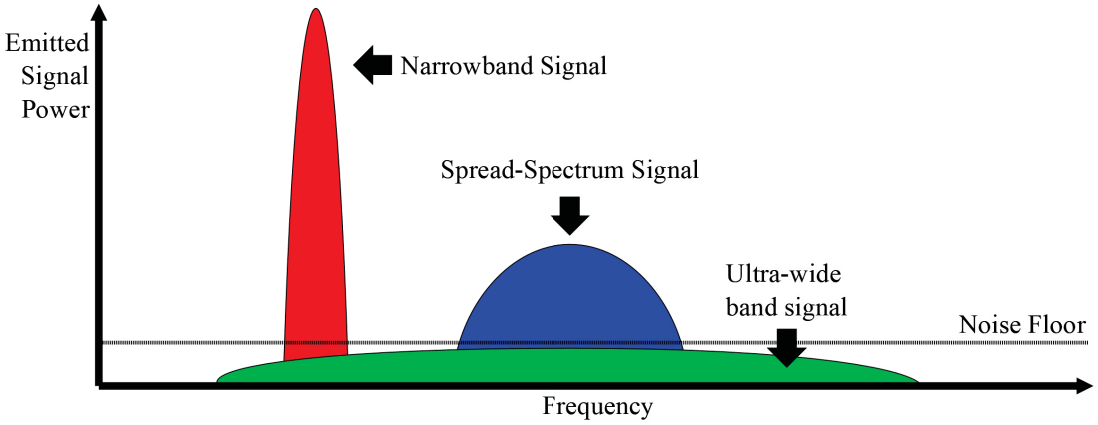


FIGURE 1 – Radiofrequency signals spectrum

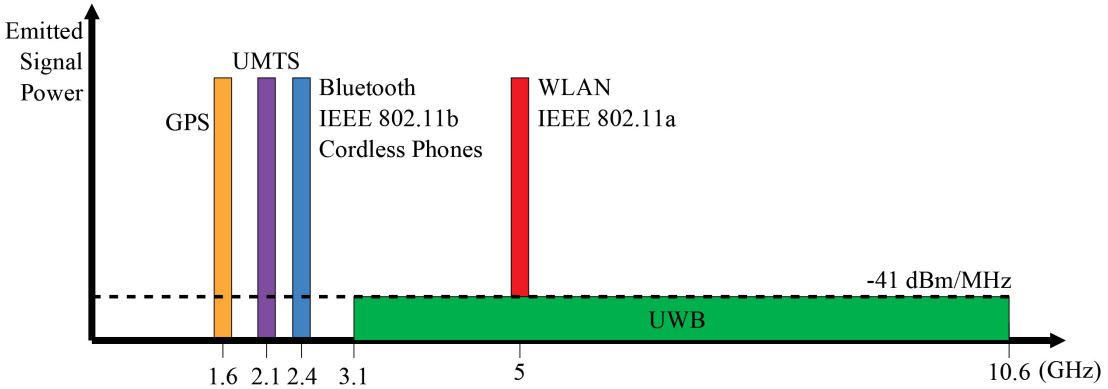


FIGURE 2 – Several technologies spectrum

The UWB signal bandwidth (BW_{XdB}) can be expressed in relation of an attenuation value (X), where that is bounded by both upper frequency (f_H) and lower frequency (f_L), such that (2.1):

$$BW_{-XdB} = f_H - f_L \tag{2.1}$$

The fractional bandwidth can be calculated as follows:

$$B_{frac} = \frac{BW_{-XdB}}{f_c} \tag{2.2}$$

The central frequency of the signal can be computed as:

$$f_c = \frac{f_H + f_L}{2} \tag{2.3}$$

Applying (2.1) and (2.3) on (2.2), the fractional bandwidth can be expressed as:

$$B_{frac} = 2\frac{f_H - f_L}{f_H + f_L} \tag{2.4}$$

A UWB signal must have either a minimal absolute bandwidth of 500 MHz or a minimal fractional bandwidth (B_{frac}) of 20%, for an attenuation of 10 dB (Fig. 3) (COMMISSION, 2002).

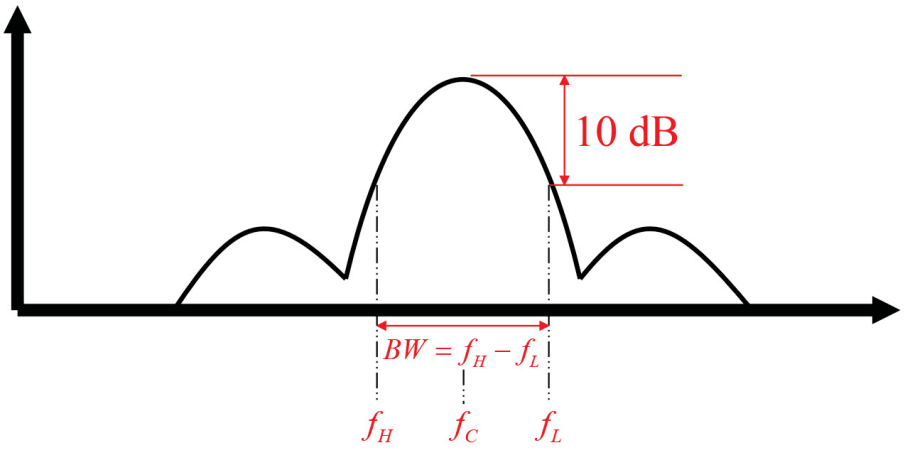


FIGURE 3 – UWB Spectrum

The transmission of ultra-wide band signals presents several interesting features. In particular, the UWB radio systems use signals, that are resistant to both multipath and jamming, and have a great time domain resolution, which makes UWB very suitable to tracking and location applications (OPPERMANN; HÄMÄLÄINEN; IINATTIN, 2004). Moreover, the pulse nature of the Impulse Radio UWB (IR-UWB) signals leads to a lower cost and lower complexity of large bandwidth signal transmission. UWB transmitters are fully able to produce short time domain pulses without RF mixing stage, which is interesting in terms of chip size.

In addition, the UWB has an improved channel capacity, where the channel is the radio-frequency spectrum within which the signal is transmitted (SHANNON, 1948). Indeed, the Shannon's limit equation is expressed below:

$$C = BW \cdot log_2(1 + SNR) \tag{2.5}$$

where C is the channel capacity (bit/s), BW the channel bandwidth and SNR the signal noise ratio, that can be written as:

$$SNR = \frac{P_r}{BW \cdot N_o} \tag{2.6}$$

where P_r is the received signal power and N_o the noise spectral density. To increase the channel capacity, the SNR should rise exponentially. Despite the UWB signal transmission positive features, it is important to pay attention to some issues. Despite the low complexity of short pulse processing, the receiver design is challenging, considering that the receiver front-end are power-hungry and both low transmitted power and wideband noise leads to a low SNR of received signal (ZOU, 2011). This can be explained by the fact that the low noise amplifier (LNA) should be operational during all time, cannot be turned-off, since it does not know precisely when the UWB pulses are transmitted. The LNA drains more power when working in higher frequencies. Meanwhile, the transmitted chain can be turned on only during pulse generation and transmission, which enables a lower power consumption.

2.1 FCC REGULATIONS (UNITED STATES)

According to Federal Communication Commission regulations, the UWB signal is authorized to be transmitted within frequency band of 3.1 – 10.6 GHz and should be transmitted with a maximum equivalent isotropically radiated power (EIRP) of -41.3 dBm/MHz and with a maximum radiated peak power, around the central frequency, of 0 dBm (BENEDETTO et al., 2006). Figure 4 shows the indoor and outdoor spectral masks defined by FCC regulations, delimiting the normalized power density (PSD) of the UWB signal to be transmitted.

2.2 EUROPEAN REGULATIONS

The Electronic Communications Committee (ECC) and committee of the Conference of Postal and Telecommunications Administrations (CEPT) in Europe authorized in 2007 the use of UWB communications and radar systems (SCHLEICHER; SCHUMACHER, 2010). According to the European regulations, an UWB signal must have a minimal bandwidth of 50 MHz for an attenuation of 13 dB, and 95% of its power should be confined within this bandwidth. Figure 5 displays the spectral mask defined

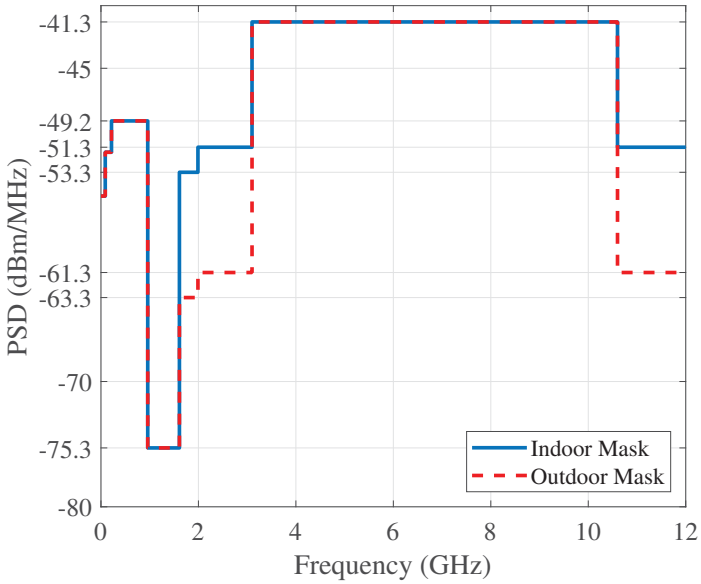


FIGURE 4 – FCC spectral masks

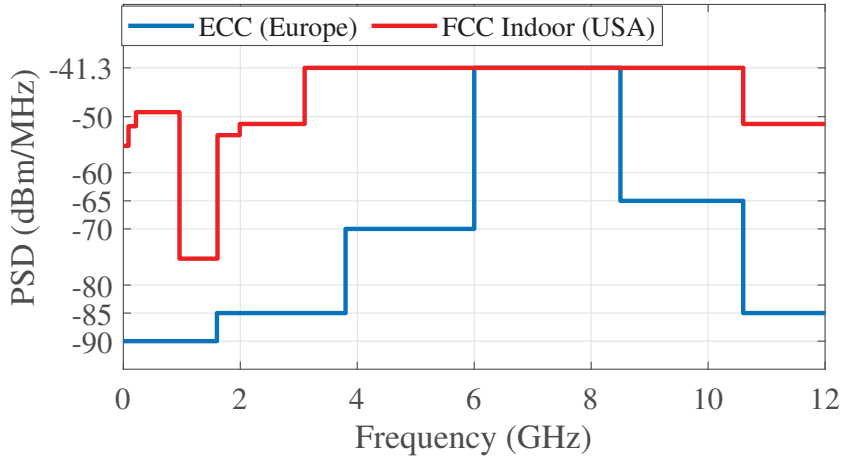


FIGURE 5 – European regulation UWB mask compared to the FCC indoor masks

by European regulations and the comparison with the FCC indoor mask. The European mask authorizes a maximum EIRP of -41.3 dBm/MHz for the frequency band between 6-8.5 GHz. The IR-UWB emitted signal must be attenuated by 28.7 dB for the frequency band between 3.8-6 GHz, 43.7 dB for the frequency band between 1.6-3.8 GHz and 23.7 dB for the frequency band between 8.5-10.6 GHz.

Moreover, the peak power and mean power defined by the European regulations are the same regulated in American regulations.

2.3 BRAZILIAN REGULATIONS

The National Telecommunications Agency of Brazil (ANATEL) has authorized the use of UWB communications within the frequency band of 3.1 – 10.6 GHz, with a transmitted UWB signal with a maximum EIRP of -41,3 dBm/MHz, like the FCC

regulations ((ETSI), 2019). According to ANATEL, a UWB signal must have a fractional bandwidth greater than or equal to 20% or an absolute bandwidth of 500 MHz for an attenuation of 10 dB. There are specific regulations for the following applications: medical imaging systems, indoor communications, and portable devices, where each one has its own frequency mask, as displayed in Figure 6.

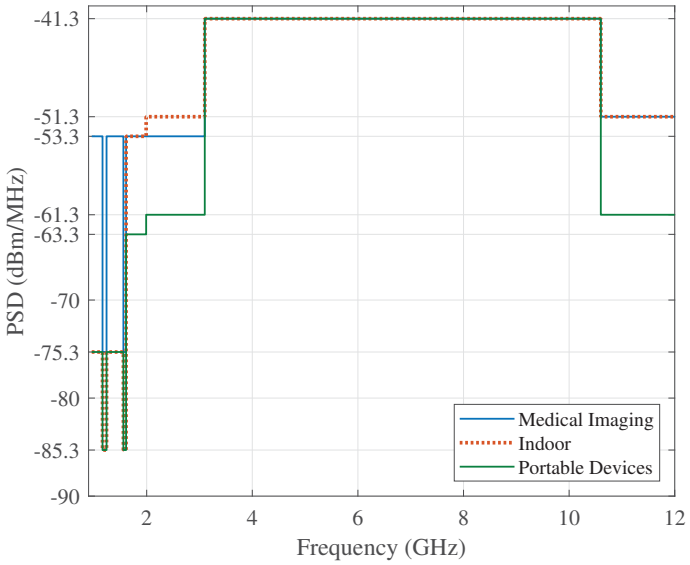


FIGURE 6 – Brazilian regulation UWB masks

2.4 IEEE 802.15.4 STANDARD OVERVIEW

UWB devices should not only respect regional regulations, but also IEEE standards spectral masks. In this sub-chapter, the IEEE 802.15.4 standard is addressed. This standard was introduced in 2011 and is dedicated to low power wireless personal area networks (LP-WPAN) applications and uses both high and low data impulse ratio (IEEE-STD-802.15.4-2020, 2020). Its frequency band plan is indicated in Figure 7. This IEEE standard defines 15 channels distributed in 3 groups: the sub-GHz band, low band and high band, where each channel has a central frequency band and a 3 dB attenuation bandwidth, that either is 499 MHz, 1081 MHz, 1331 MHz and 1355 MHz. For a particular group, the UWB device must cover one channel in particular, indicated in red in Figure 7. The first group, the sub-GHz, has only one channel of 499 MHz. The second group, the low band, presents 3 channels of 499 MHz and one of 1331 MHz within the frequency band of 3.1-4.8 GHz. The third and last group, the high band, presents 9 channels of 499 MHz, one of 1081 MHz, one of 1331 MHz and one of 1355 MHz within the frequency band of 6-10.6 GHz. Table 1 summarizes the IEEE 802.15.4 15 channels, indicating which are mandatories and the optional ones.

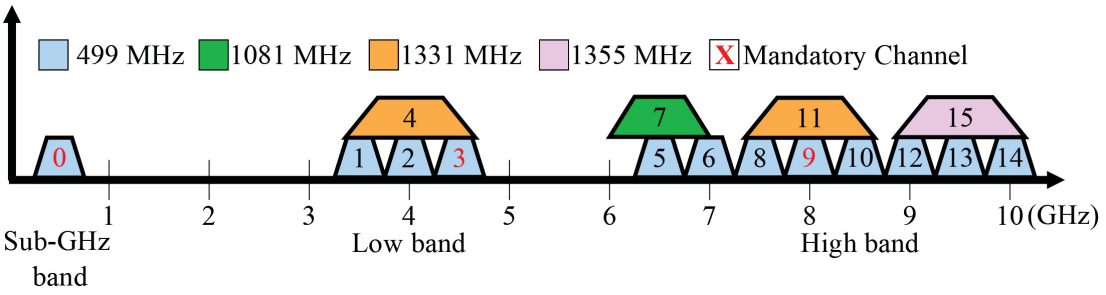


FIGURE 7 – IEEE 802.15.4 standard channels frequency plan

TABLE 1 – IEEE 802.15.4 Standard Channels

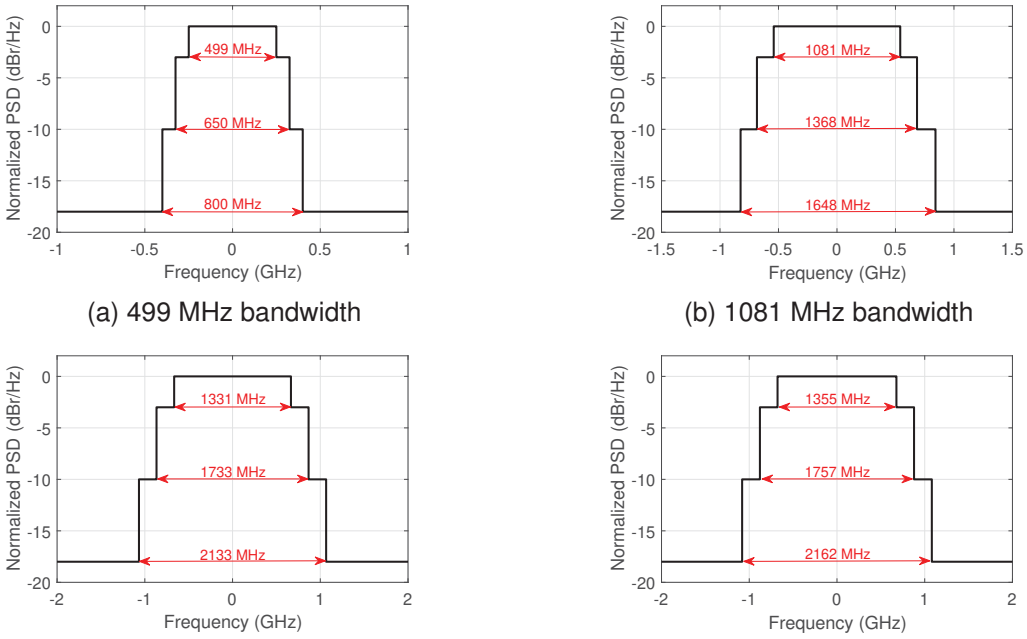
Group	Channel (n)	f_c (MHz)	$BW_{X=3\ dB}$ (MHz)	Description
0 - Sub-GHz Band	0	499.2	499.2	Mandatory
1 - Low Band	1	3494.4	499.2	Optional
	2	3993.6	499.2	Optional
	3	4482.8	499.2	Mandatory
	4	3993.6	1331.2	Optional
2 - High Band	5	6489.6	499.2	Optional
	6	6988.8	499.2	Optional
	7	6489.6	1081.2	Optional
	8	7488.0	499.2	Optional
	9	7987.2	499.2	Mandatory
	10	8496.4	499.2	Optional
	11	7987.2	1331.2	Optional
	12	8985.6	499.2	Optional
	13	9484.8	499.2	Optional
	14	9984.0	499.2	Optional
	15	9484.8	1355	Optional

Figure 8 presents the IEEE 802.15.4 standard spectral masks for all a 3 dB attenuation bandwidth displayed in Table 1 and also the frequency bandwidth for an attenuation of 3 dB, 10 dB and 18 dB.

Besides, the duration of the generated UWB pulses influences in the shape of the spectral mask for all IEEE standardized channels, as pointed in the following expression of signal relative attenuation in terms of central frequency (f_c) of a particular channel and the pulse duration (τ_p):

$$X_{dB} = \begin{cases} 0\ dBr & if\ \ |f - f_c(n)| \leq \frac{0.65}{\tau_p} \\ 10\ dBr & if\ \frac{0.65}{\tau_p} < |f - f_c(n)| \leq \frac{0.8}{\tau_p} \\ 18\ dBr & if\ \frac{0.8}{\tau_p} < |f - f_c(n)| \end{cases} \tag{2.7}$$

where f is frequency and n the channel index. From Figure 8, it can be seen that larger pulses have narrower spectrum, and shorter pulses wider spectrum. From this, it can be inferred that a pulse addressing the channel 15 will be the shortest one.



(a) 499 MHz bandwidth

(b) 1081 MHz bandwidth

(c) 1331 MHz bandwidth

(d) 1355 MHz bandwidth

FIGURE 8 – IEEE 802.15.4 spectral masks

2.5 IEEE 802.15.6 STANDARD OVERVIEW

In this sub-chapter, the IEEE 802.15.6 standard is addressed. This standard was introduced in 2012 and is dedicated to WBAN applications and uses Impulse Radio UWB or frequency modulation (FM-UWB) (IEEE-STD-802.15.6-2012, 2012). Its frequency band plan is indicated in Figure 9. It is similar to IEEE 802.15.4 frequency band plan displayed in Figure 7. This IEEE standard defines 11 channels distributed in 2 groups: low band and high band. For a particular group, the UWB device must cover one channel in particular, indicated in red in Figure 9. The first group, the low band, presents 3 channels of 499 MHz within the frequency band of 3.1-4.8 GHz. The other group, the high band, presents 8 channels of 499 MHz within the frequency band of 6-10.6 GHz. Table 2 summarizes the 11 channels, indicating which are mandatories and the optional ones. Figure 10 presents the IEEE 802.15.6 standard spectral mask.

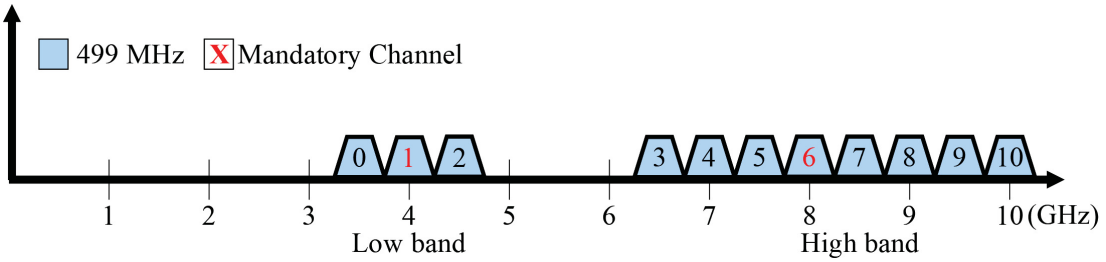


FIGURE 9 – IEEE 802.15.6 standard channels frequency plan

TABLE 2 – IEEE 802.15.6 Standard Channels

Group	Channel (n)	f_c (MHz)	$BW_{X=3\ dB}$ (MHz)	Description
1 - Low Band	0	3494.4	499.2	Optional
	1	3993.6	499.2	Mandatory
	2	4492.8	499.2	Optional
2 - High Band	3	6489.6	499.2	Optional
	4	6988.8	499.2	Optional
	5	7488.0	499.2	Optional
	6	7987.2	499.2	Mandatory
	7	8486.4	499.2	Optional
	8	8985.6	499.2	Optional
	9	9484.8	499.2	Optional
	10	9984.0	499.2	Optional

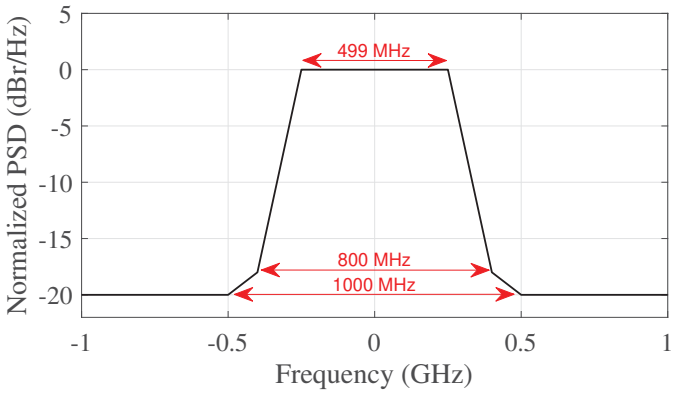


FIGURE 10 – IEEE 802.15.6 spectral mask

2.6 IMPULSE RADIO

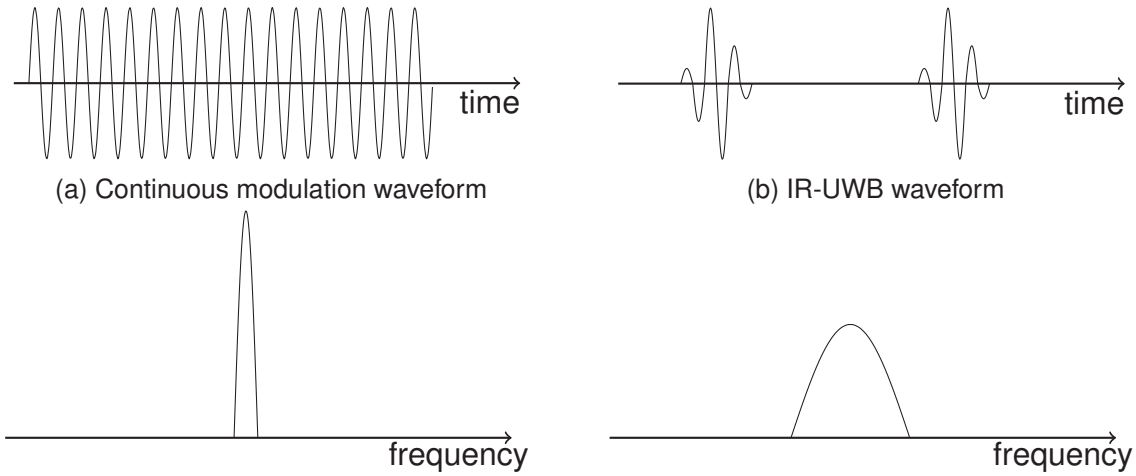
Within the UWB communications field, among the UWB signals, the impulse radio (IR) is one that is capable to perform short-range wireless applications in dense multipath environments (OPPERMANN; HÄMÄLÄINEN; IINATTIN, 2004). To exploit the 3.1 – 10.6 GHz frequency band, the IEEE 802.15.4 and IEEE 802.15.6 have chosen the impulse radio instead of the usual carrier modulations. The ultra-wide band impulse radio (IR-UWB) consists of the transmission of low duty cycle short-pulses on the contrary of the traditional carrier modulations which use continuous waves (Figs. 11a and 11b). The IR-UWB pulse is typically of nanosecond order, hence has a wider bandwidth, in comparison with traditional carrier modulations that presents a narrowband spectrum (Figs. 11c and 11d). Due to aggressive duty cycle, the modulated IR-UWB has the interesting feature to enable the power down of transceivers between two consecutive pulses transmission, such that it allows to save power and that the average power is low when compared to the single pulse instantaneous power. The mean power consumption of an emitted IR-UWB pulse can be calculated as follows:

$$P_{DC} = P_{0Hz} + E_{ac} \bullet \ PRF \tag{2.8}$$

where E_{ac} is the energy drained per IR-UWB pulse, PRF the mean pulse repetition frequency and P_{0Hz} the leakage power of the IR-UWB pulse generator. Notice that there is a linear behavior between the DC power and the pulse repletion frequency. E_{ac} is the slope factor of the expression of mean average power and can be calculated as follows:

$$E_{ac} = \frac{P_{DC_2} - P_{DC_1}}{PRF_2 - PRF_1} \tag{2.9}$$

Therefore, for a low data rate transmission, a low power consumption can be achieved, which is interesting for low-power applications like WPAN and WSN. For impulse modulations, the emitted power spectral density is directly proportional to the modulus squared of the emitted pulse spectrum. Moreover, the IR-UWB pulse is applied to a designed UWB antenna, that behaves as a filter.



(a) Continuous modulation waveform (b) IR-UWB waveform

(c) Continuous modulation spectrum (d) IR-UWB spectrum

FIGURE 11 – Traditional narrowband and IR-UWB signals comparison

To ensure that the IR-UWB communications do not interfere with narrowband radio systems operating in dedicated band, a feasible option is to spread the spectrum through either the envelope shaping or the time hopping modulation. Moreover, the IR-UWB baseband signal codification relies on some parameters like position, polarity, and amplitude.

There are two distinct IR-UWB communications classes: Carrierless and carrier-based (ZOU, 2011). For the carrierless IR-UWB, the baseband pulse is generated directly, dispensing mixers and local oscillators, hence eliminating the frequency up-conversion, making the transmitter realization simpler and with lower power. The generated pulse width is defined by the delay of the logic gates, which are usually followed by output driver and pulse shaping filter (Fig. 12).

On the other hand, the carrier-based IR-UWB is based on mixing a frequency wave with an envelope, shifting the DC energy into the targeted UWB band, providing a better spectral efficiency and better tunability capabilities. Among the envelope shapes, there are rectangular, triangular, Gaussian and root-raised cosine. Some reported transmitter topologies have been realized with a local oscillator (Fig. 13), which arises the signal synthesizer design complexity and the power consumption (WENTZLOFF; CHANDRAKASAN, 2007; DOKANIA, R. K. et al., 2011).

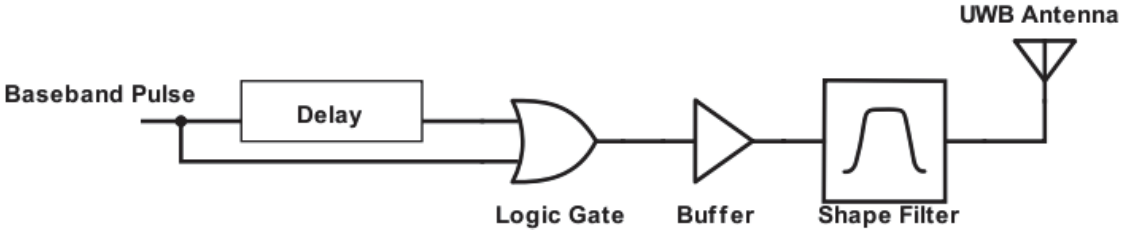


FIGURE 12 – IR-UWB Carrierless architecture based on an edge combiner

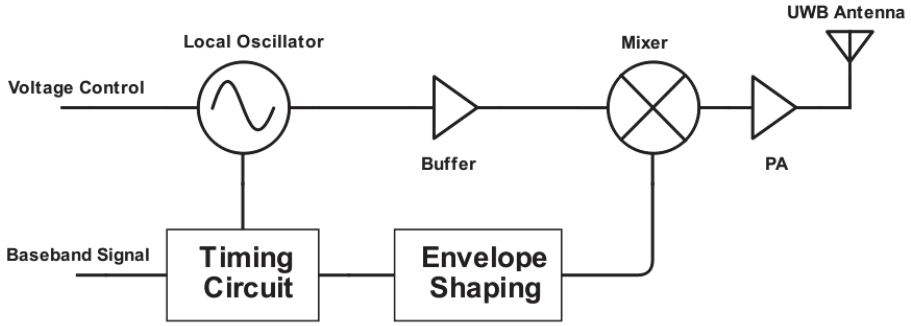


FIGURE 13 – IR-UWB Carrier-based architecture based on gated local oscillator

2.7 PULSE GENERATION PRINCIPLES

As told in previous sub-chapter, for an IR-UWB transmission, the data can be transmitted using different values of the emitted pulses parameters like amplitude, position, or polarity. In the case of a pulse amplitude modulation (PAM) (Fig. 14), the signal emitted by the UWB antenna can be expressed as a combination of single pulses, such that:

$$s\left(t\right) = \sum_{k=0}^{\infty} d_k \cdot p\left(t - \frac{k}{D_s}\right) \tag{2.10}$$

where d_k is the k^{th} emitted symbol taken from a M-ary alphabet D, D_s is the symbol rate, and $p(t)$ is the generated pulse waveform. Given that the PAM modulation is a isochronous modulation, the Bennett equation can be applied to calculate the power spectral density S_{SS}, considering that symbols d_k are independents, such that: (PROAKIS, 2007; MUHR, 2016):

$$S_{SS}(f) = S_{C_{SS}}(f) + S_{D_{SS}}(f) \tag{2.11}$$

$$S_{SS}(f) = \frac{1}{T_S}\left(E\left[D^2\right] - E[D]^2\right)|P(f)|^2 + \frac{1}{T_S}E[D]^2|P(f)|^2\delta_{f_S}(f) \tag{2.12}$$

$$\delta_{f_S}(f) = \sum_{k=-\infty}^{\infty}\delta_{f_S}\left(f - \frac{k}{T_S}\right) \tag{2.13}$$

where $S_{C_{SS}}$ is the continuous component of the spectrum and $S_{D_{SS}}$ is the discontinuous component of the spectrum. Besides, T_S is the sampling period, D the alphabet symbol, $E[D]$ the expected value of alphabet D or first moment, $E[D]^2$ the alphabet D second moment, and finally $\delta(f)$ dirac delta function.

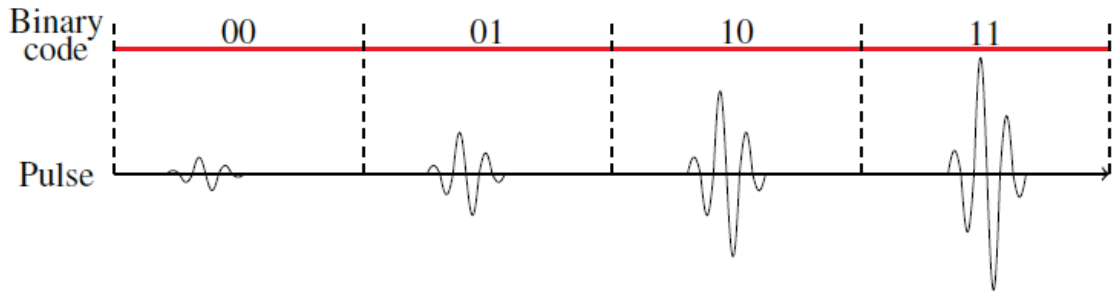


FIGURE 14 – PAM modulation time domain waveform

For an off on keying (OOK) modulation (Fig. 15), the alphabet D is:

$$D : \{d_k\} = \{0, 1\} \tag{2.14}$$

and for a binary phase shift keying (BPSK) modulation (Fig. 16), the alphabet D is:

$$D : \{d_k\} = \{-1, 1\} \tag{2.15}$$

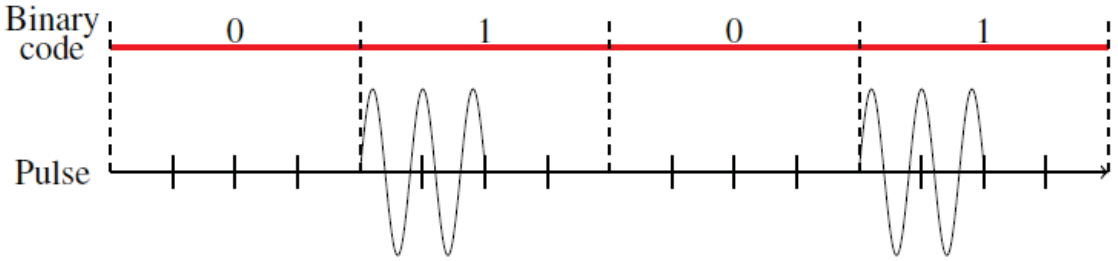


FIGURE 15 – OOK modulation time domain waveform

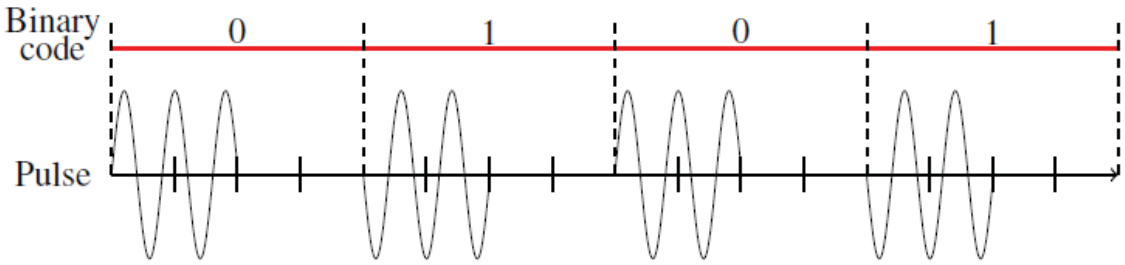


FIGURE 16 – BPSK modulation time domain waveform

For OOK and BPSK modulations, their power spectral density S_{SS} can be calculated from the following expression:

$$S_{SS}(f) = \frac{D_S}{4}\left|P(f)^2\right| + \frac{D_S^2}{4}\left|P(f)^2\right|\delta_{fs}(f) \tag{2.16}$$

The signal from Figures 15 and 16 can be generated by an IR-UWB pulse generator. The main parameters of the pulse generation by an oscillator are the oscillation duration and the oscillation frequency, that respectively determine the generated pulse bandwidth and its central frequency.

2.8 PULSE ENVELOPES OVERVIEW

In the IR-UWB pulses generation scheme, a critical point is the pulse envelope shape to be generated to obtain a pulse frequency response and an expected rejection of 18 dB for adjacent lobes, such that UWB pulse spectrum is able to fit into standard masks, mostly IEEE standards like 802.15.4 and 802.15.6. It is important to note here that the generated pulse main and side lobes should fit into regional masks, like for example the FCC (Fig. 4, and IEEE 802.15.4 and 802.15.6 standards (Figs. 8 and 10). Meanwhile, the spectre located at frequencies outside the 3.1-10.6 GHz band is not a major concern here given that the UWB antenna frequency response and its filtering over the generated pulse. An UWB antenna is not studied in this dissertation work.

The UWB pulse envelope has a major effect over pulse spectrum side lobes levels. The emitted pulse $p(t)$ can be described with a modulated sinewave, expressed as follows:

$$p(t) = x(t)\cos(2\pi f_c t - \varphi) \tag{2.17}$$

where $x(t)$ is the pulse envelope, f_c the frequency which the pulse power spectral density reaches its maximum value, and φ the sinewave phase. The emitted pulse Fourier transform can be computed as:

$$P(f) = \frac{\exp(-j\varphi)}{2}\left[X(f+f_c) + X(f-f_c)\right] \tag{2.18}$$

where $X(f)$ is the envelope Fourier transform. Since then, all envelopes approached in this work are real and even function, which means that the pulse spectrum presents a symmetry around the DC component, and also the central frequency f_c is greater than the half value of the emitted pulse passband, the mono-lateral Fourier transform of the pulse can be expressed as:

$$P^{+}(f) = \sqrt{2}P(f) - \frac{\sqrt{2}}{2}\left[X(f+f_c)\right]\exp(-j\varphi) \tag{2.19}$$

$$P^{+}(f) = \frac{\sqrt{2}}{2}\left[X(f-f_c)\right]\exp(-j\varphi) \tag{2.20}$$

In terms of pulse emitted energy E_p, this can be estimated by calculating the pulse energy drained by the load Z_L to which the pulse is applied, such that:

$$E_p = \frac{1}{Z_L}\int_{-\infty}^{\infty} |p(t)|^2 \, dt \tag{2.21}$$

Combining (2.17) and (2.21), the pulse emitted energy E_p can be calculated as follows:

$$E_p = \frac{1}{2Z_L}\int_{-\infty}^{\infty} |x(t)|^2 \, dt \tag{2.22}$$

In this manuscript, three types of envelope shapes are addressed: rectangular, triangular and sample & hold.

2.8.1 Rectangular

The rectangular envelope is the simplest to generate. This envelope is based on a rectangular function, thereby written as follows:

$$x_R(t) = A \cdot \Pi\left(\frac{t}{\tau_p}\right) \tag{2.23}$$

where A and τ_p are the generated pulse amplitude and width, respectively. This envelope performs a rectangular windowing over the sinusoidal waveform generated by a local oscillator for UWB pulse generator whose architecture is based on frequency transposition principle. Shifting to frequency domain, the rectangular envelope Fourier transform can be computed as:

$$X_R(f) = A\tau_p sinc(f\tau_p) \tag{2.24}$$

where:

$$sinc(f) = \frac{sin(\pi f)}{\pi f} \tag{2.25}$$

Combining the last equation into equation (2.16), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P_R^+(f) = \frac{A\tau_p}{\sqrt{2}} sinc\left((f - f_c)\,\tau_p\right) \exp\left(-j\varphi\right) \tag{2.26}$$

For this envelope in particular, from (2.22), the pulse emitted energy expression is given as follows:

$$E_{pR} = \frac{A^2\tau_p}{2Z_L} \tag{2.27}$$

For a BPSK impulse modulation, the power spectral density is proportional to the magnitude squared of $P_R^+(f)$. Regarding the pulse time-domain parameters, the duration τ_p of $p(t)$ can be expressed as function of oscillation frequency f_c as follows:

$$\tau_p = \frac{N}{2f_c} \tag{2.28}$$

where N is the integer number of sinusoidal half-periods of the generated pulse. Moreover, the minimal number of half-periods of the sinusoidal waveform, in relation of the bandwidth BW_{-XdB}, can be written as:

$$N_{\min} = \alpha \frac{f_M}{BW_{-XdB}} \tag{2.29}$$

where α is a coefficient that has either a value of 1.8 for an considered attenuation X_{dB} of 3 dB, a value of 3 for an considered attenuation X_{dB} of 10 dB, or a 10.8 or an considered attenuation X_{dB} of 18 dB. Indeed, for every considered attenuation X_{dB} value, there is a corresponding α coefficient single value. The attenuation values of 3 dB, 10 dB and 18 dB come from the IEEE 802.15.4 standard masks of Figure 8. Combining (2.28) and (2.29), the pulse minimum width can be expressed as function of a bandwidth BW for a certain attenuation X_{dB}:

$$\tau_{p-\min} = \frac{\alpha}{2BW_{-XdB}} \tag{2.30}$$

Table 3 displays all 15 channels addressed in Table 1 pulse bandwidth for a certain attenuation X_{dB} and its corresponding pulse width, calculated from 2.30. Indeed, for pulses targeting the standardized channel 15, to respect a bandwidth of 1355 MHz, a minimal pulse duration required is 0.67 ns. To respect both bandwidth of 1355 MHz and 1757 MHz (Fig. 8d), a minimal pulse duration is 0.85 ns. In order to fit properly into IEEE 802.15.4 mask (Fig. 8d), a minimal pulse duration necessary is 2.50 ns, for a rectangular envelope.

Figures 17, 18 and 19 present an IR-UWB pulses waveform and spectrum, addressing the channel 3 (BW_{-3dB} = 499 MHz) from IEEE 802.15.4 standard, having

a rectangular envelope. The width values of pulses displayed in Figures 17, 18 and 19 come from Table 3. From these Figures, it can be noticed that the only the pulse spectrum of Figure 19 fully fits into IEEE 802.15.4 mask, which means that to respect the IEEE 802.15.4 frequency masks, a minimal pulse duration of 6.75 ns is required for this channel in particular, considering a rectangular envelope. However the pulse bandwidth for an attenuation of 10 dB is not wide enough to be considered as un UWB signal. It can be noticed that many regulations, like the FCC, define that the UWB signal must have either a fractional bandwidth (B_{frac}) of 20% or an absolute bandwidth of 500 MHz.

TABLE 3 – IEEE 802.15.4 Standard Bandwidth and Pulse duration in terms of the Attenuation Levels - Rectangular Envelope

Channel	Attenuation (X)					
	3 dB		10 dB		18 dB	
	BW_{-XdB} (GHz)	T_p (ns)	BW_{-XdB} (GHz)	T_p (ns)	BW_{-XdB} (GHz)	T_p (ns)
15	1.355	0.67	1.755	0.85	2.16	2.50
4,11	1.331	0.68	1.729	0.87	2.128	2.54
7	1.081	0.83	1.404	1.07	1.728	3.13
Others	0.5	1.8	0.65	2.31	0.8	6.75

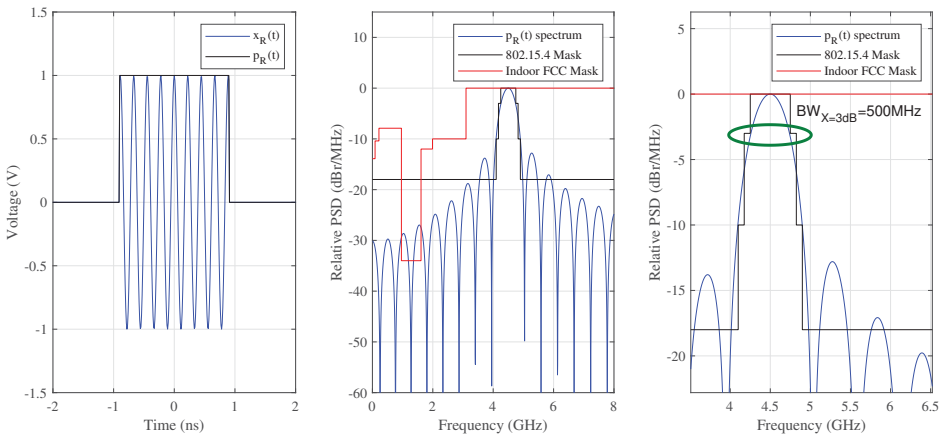


FIGURE 17 – IR-UWB pulses with rectangular envelope target to comply with the channel 3 of IEEE 802.15.4 standard (BW_{-3dB} = 499 MHz and τ_p = 1.8 ns)

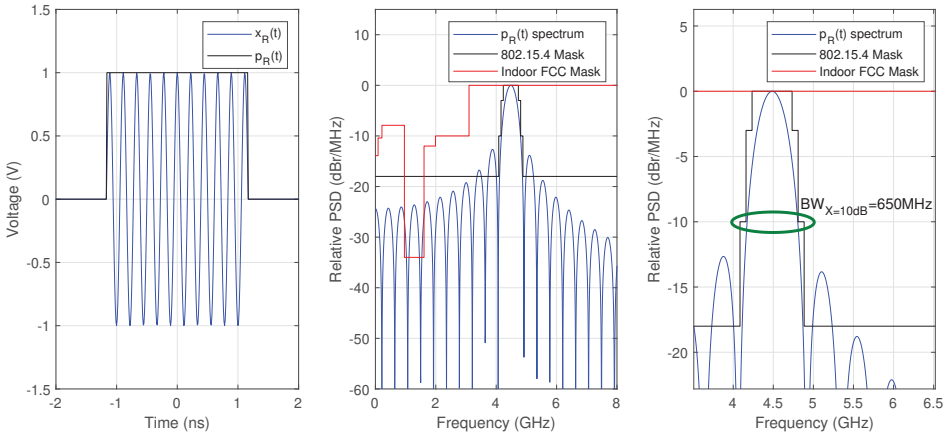


FIGURE 18 – IR-UWB pulses with rectangular envelope target to comply with the channel 3 of IEEE 802.15.4 standard (BW_{-10dB} = 650 MHz and τ_p = 2.31 ns)

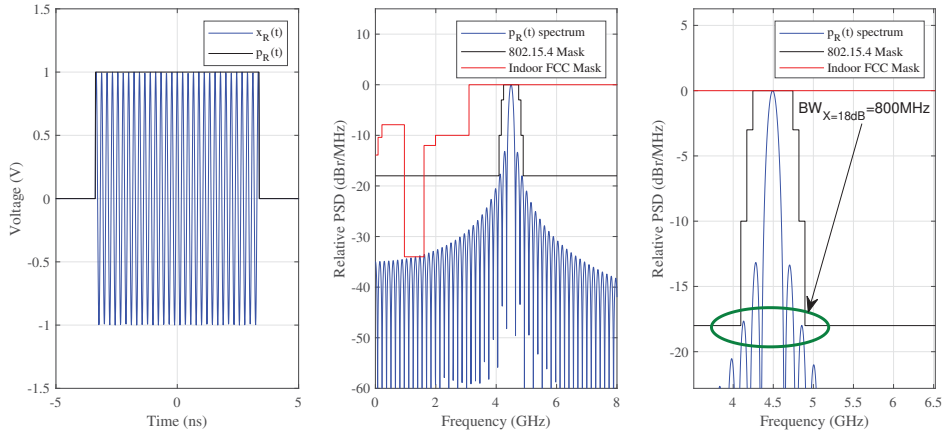


FIGURE 19 – IR-UWB pulses with rectangular envelope target to comply with the channel 3 of IEEE 802.15.4 standard (BW_{-18dB} = 800 MHz and τ_p = 6.75 ns)

2.8.2 Triangular

A second studied envelope in this manuscript is the triangular envelope. It is more complex to generate than the rectangular envelope. The triangular envelope can be defined by the following expression:

$$x_T(t) = \begin{cases} A\left(1 - \frac{2|t|}{\tau_p}\right) & if \quad 0 < |t| < \frac{\tau_p}{2} \\ 0 & if \quad otherwise \end{cases} \tag{2.31}$$

where A is the pulse amplitude, and τ_p the pulse duration. Shifting to frequency domain, the triangular envelope Fourier transform can be computed as:

$$X_T(f) = \frac{A\tau_p}{2} sinc^2\left(f\frac{\tau_p}{2}\right) \tag{2.32}$$

Applying the triangular envelope into (2.20), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P_T^+(f) = \frac{A\tau_p}{2} sinc^2\left[(f - f_M)\frac{\tau_p}{2}\right] \exp(-j\varphi) \tag{2.33}$$

For triangular envelope, from (2.22), the pulse emitted energy expression is given as follows:

$$E_{pT} = \frac{A^2\tau_p}{8Z_L} \tag{2.34}$$

Regarding the pulse time-domain parameters, similarly to rectangular envelope, the pulse minimum width can be expressed as:

$$\tau_{p-\min} = \frac{\alpha_T}{2BW_{-X\text{dB}}} \tag{2.35}$$

where α_T is a coefficient that has either a value of 2.56 for an considered attenuation X_{dB} of 3 dB, a value of 4.448 for an considered attenuation X_{dB} of 10 dB, or 5.68 for a considered attenuation X_{dB} of 18 dB. Despite the rectangular and triangular envelope present the same expression for minimal pulse width, α and α_T coefficients have different values for these two envelopes.

Table 4 displays pulse bandwidth for certain attenuation X_{dB} and its corresponding pulse width, calculated from 2.35. To fully fit into IEEE 802.15.4 mask of Figure 8d, a minimal pulse duration necessary is 3.55 ns, for a triangular envelope.

Figures 20, 21 and 22 display an IR-UWB pulse waveform and spectrum, addressing the channel 3 (BW_{-3dB}= 499 MHz) from IEEE 802.15.4 standard, having a triangular envelope. The width values of pulses displayed in Figures 20, 21 and 22 come from Table 3. From these figures, it can be observed that only the pulse spectrum of Figure 22 fits completely into IEEE 802.15.4 mask, such that a minimal pulse duration of 3.55 is necessary for this standardized channel, considering a triangular envelope. Moreover, from Figure 22, it can be seen that the pulse spectrum presents side-lobes with lower power spectral density than the rectangular envelope. Unlike the rectangular pulse, the triangular envelope has a bandwidth for an attenuation of 10 dB sufficiently large to be considered a UWB signal.

TABLE 4 – IEEE 802.15.4 Standard Bandwidth and Pulse duration in terms of the Attenuation Levels - Triangular Envelope

Channel	Attenuation (X)					
	3 dB		10 dB		18 dB	
	BW (GHz)	T_p (ns)	BW (GHz)	T_p (ns)	BW (GHz)	T_p (ns)
15	1.355	0.94	1.755	1.28	2.16	1.31
4,11	1.331	0.96	1.729	1.3	2.128	1.33
7	1.081	1.19	1.404	1.60	1.728	1.64
Others	0.5	2.56	0.65	3.45	0.8	3.55

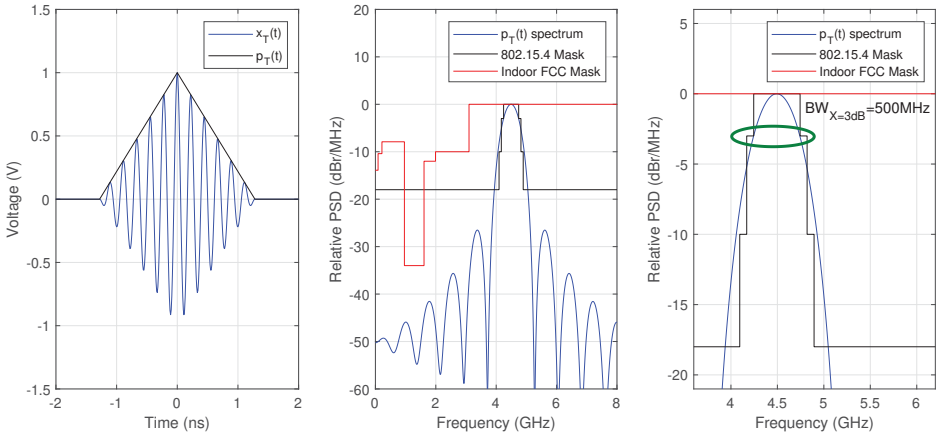


FIGURE 20 – IR-UWB pulse with triangular envelope compliant with the channel 3 of IEEE 802.15.4 standard (BW_{-3dB} = 499 MHz and τ_p = 2.56 ns)

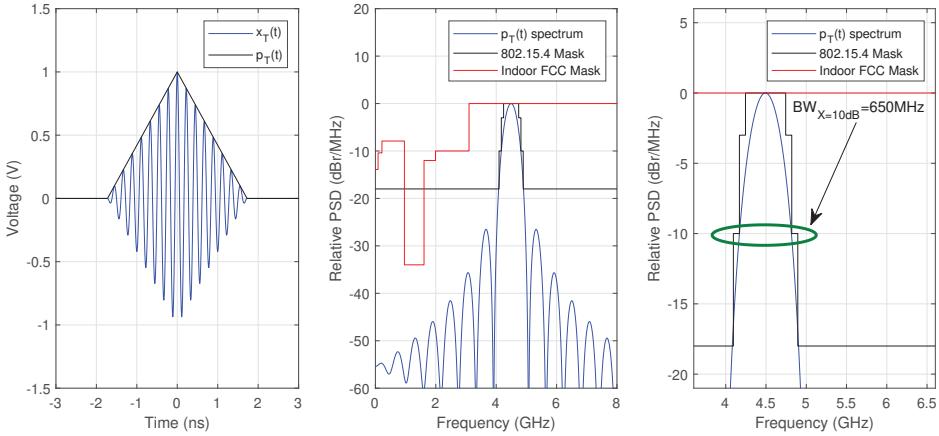


FIGURE 21 – IR-UWB pulse with triangular envelope compliant with the channel 3 of IEEE 802.15.4 standard (BW_{-10dB} = 650 MHz and τ_p = 3.45 ns)

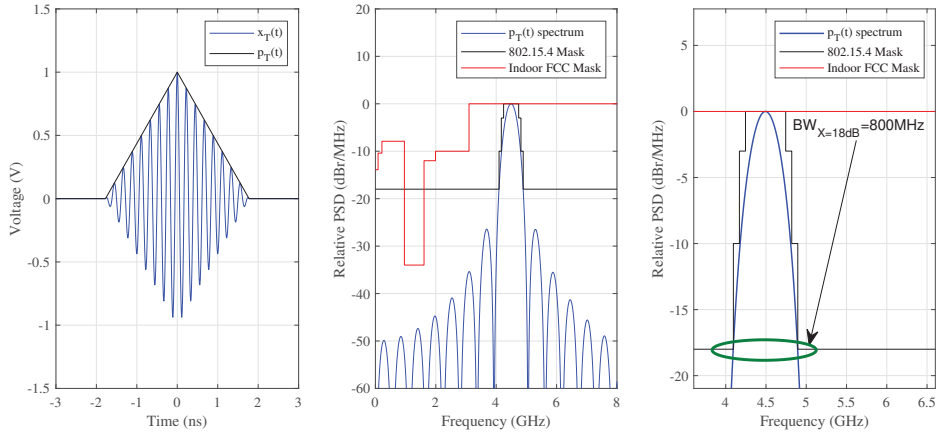


FIGURE 22 – IR-UWB pulse with triangular envelope compliant with the channel 3 of IEEE 802.15.4 standard (BW_{-18dB} = 800 MHz and τ_p = 3.55 ns)

2.8.3 Sample & Hold

In the previous sub-chapter, it has been possible to observe that the generation of IR-UWB pulse with triangular is able to be compliant with the spectral requirements imposed by IEEE 802.15.4 standards. However, these envelopes are difficult to fabricate, requiring a pulse shaping circuit architecture with high complexity.

A digital realization consisting of sample & hold envelope arises as an interesting and less complex alternative despite that an analog realization of pulse shaping circuit presents better tuning performance (ARTEMIO-SCHOULTEN et al., 2020). The sample & hold envelope is a combination of rectangular time-shifted functions, such as:

$$x_S(t) = \sum_{k=0}^{K-1} x_C\left(k\tau_e - \frac{K-1}{2}\tau_e\right) \cdot \Pi_T\left(t - k\tau_e + \frac{K-1}{2}\tau_e\right) \tag{2.36}$$

where τ_e is the duration of a single pulse, K the amount of single pulse, and $x_C(t)$ represents a non-discrete envelope (continuous), like for example the triangular one (Fig. 22). Shifting into the frequency domain, the sample & hold envelope Fourier transform can be computed as:

$$X_S(f) = \exp\left(-j\pi f\tau_e\left(\frac{K-1}{2}\right)\right) sinc^2(f\tau_e) \sum_{k=0}^{K-1} X_C\left(f - \frac{k}{\tau_e}\right) \tag{2.37}$$

Applying the sample & hold envelope into (2.20), the emitted pulse mono-lateral Fourier transform can be computed as:

$$P_s^+(f) = Y_s(f)\, sinc\left([f - f_c]\,\tau_e\right) \sum_{k=-\infty}^{\infty} X\left(f - f_c - \frac{k}{T_e}\right) \tag{2.38}$$

where:

$$Y_s(f) = \frac{\sqrt{2}}{2}\exp(-j\varphi)\exp\left(-j\pi f\tau_e\left[\frac{K-1}{2}\right]\right) \tag{2.39}$$

For the sample & hold envelope, from (2.22), the pulse emitted energy can be estimated as follows:

$$E_{pS} = \frac{\tau_p}{2Z_L} \cdot \sum_{k=0}^{K-1} x_C^2\left(k\tau_e - \frac{K-1}{2}\tau_e\right) \tag{2.40}$$

Figure 23 presents an emitted pulse waveform and spectrum, addressing the channel 3 from IEEE 802.15.4 standard, having a sample $\&$ hold envelope. From Figure 23, it can be noticed that the spectrum from Figure 23 fits into the IEEE 802.15.4 mask, although it presented stronger side-lobes than triangular envelope. It can be noticed that IR-UWB pulse with sample $\&$ hold envelope did not respect the indoor FCC mask

at low frequencies, however this is not a major concern given that the UWB antenna frequency response and its filtering over the IR-UWB pulse. The essential here is that the pulse main and side lobes fit into regulatory masks. Therefore, the sample $\&$ hold envelope is feasible to be implemented in the IR-UWB pulse synthesizer, reducing its complexity design.

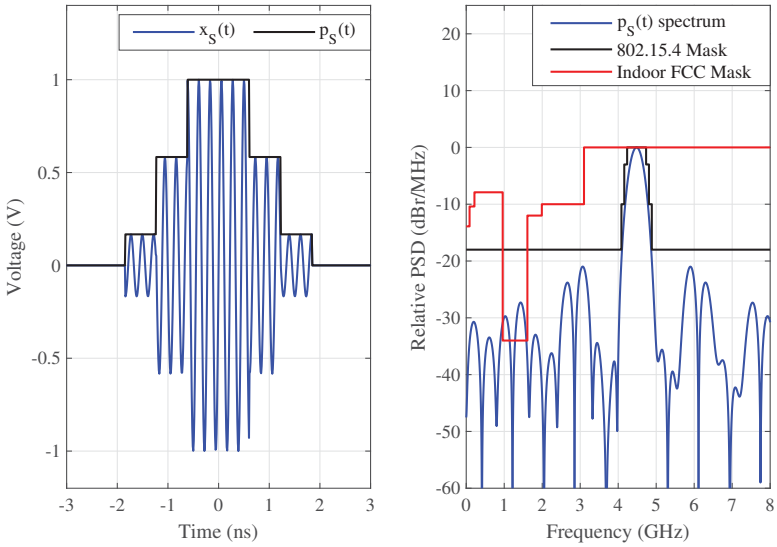


FIGURE 23 – Example of IR-UWB pulse with sampled & hold envelope compliant with the channel 3 of IEEE 802.15.4 standard (K = 6, BW_{-3dB} = 499 MHz and τ_p = 4 ns).

3 STATE OF ART

The previous chapter has described different standards, like the IEEE 802.15.4 and IEEE 802.15.6, and different UWB regulations that imposes spectral masks for the UWB emitted signal. This UWB signal can present a central frequency between 3.1 to 10.6 GHz with a bandwidth of 500 MHz for an attenuation of 10 dB. In the IR-UWB transmitter design, it is essential the design of a pulse generator capable to address a large frequency band, covering entirely the FCC band, and to tune the IR-UWB generated pulse bandwidth in order to address the IEEE standardized channels. Moreover, the IR-UWB pulse envelope shaping is important to ensure that the generated pulse complies with spectral masks established by IEEE standards.

Besides, the main metrics of the UWB transmitters are:

- Pulse synthesis method
- Central frequency (F_c) range
- Spectral Compliance
- IEEE 802.15.4 standard channels addressed
- IEEE 802.15.6 standard channels addressed
- Pulse bandwidth for an attenuation of 10 dB ($BW_{X=10dB}$)
- Pulse maximum magnitude
- Pulse shape
- Modulation
- Static Power
- Dynamic Energy (E_{ac})
- Emitted Energy (E_p)
- Data rate
- Power consumption in relation of data rate

Two pulse synthesis methods are reported in literature: the direct synthesis and synthesis by frequency transposition. In the first method, the pulse is directly synthesized within the target frequency band. Meanwhile, in the other method, a baseband pulse

modulates a voltage-controlled oscillator (VCO). In this chapter, both methods will be approached, reporting several works from literature that have employed those methods into IR-UWB pulse generator design. The method based on direct pulse synthesis employs delay lines. In the other hand, the method based on pulse synthesis based on transposition uses different architectures that are based on mixers, LC-tank oscillators, and ring oscillators. In the end of the chapter, Table 3.1 compares the reported pulse generator performances.

3.1 DIRECT PULSE SYNTHESIS BASED ON DELAY LINES

In relation of the first pulse synthesis method approached in this chapter, the direct pulse synthesis is performed with a circuit composed of delay lines (Fig. 12). The IR-UWB pulse is generated directly on targeted frequency band. To generate this pulse, oscillators are not employed, but voltage controlled delay cells (baseband pulse generator) and a edge combiner (baseband pulse combiner). Indeed, a set of delay cells, whose propagation delay is tuned by voltage, generates time shifted baseband pulses which are combined in a edge combiner circuit. This architecture is capable to generate pulses with arbitrary shape. A larger number of delay cells rise the pulse shaping capability. However, that implies in a higher complexity of the pulse combiner circuit and higher influence from parasitic capacitances, that impacts on central frequency range.

In particular, for this method, most of the reported architectures in the literature are generators based on delay lines and excited filters. In (MIRANDA; MENG, 2010), a UWB pulse transmitter in 65 nm bulk CMOS based on a programmable delay line cell is reported, whose schematic is showed in Figure 24. The transmitter of Figure 24 can program digitally the amplitude and duration of every UWB pulse, which makes feasible a flexible shaping of the pulse spectrum . This UWB transmitter architecture is mainly based on 10 programmable delay cells in cascade, that are capable to generate signals whose bandwidth is greater than 450 MHz. The delay cell (Fig. 25) controls the duration of each cycle of the UWB pulse, where the delays are configurated separately and the total number of cycles are 10. The delay cell of Figure 25 presents a 3-bit programmable delay between input and output, where the delay time value results from MOS capacitor discharge rate control done by three digitally controlled binary weighted parallel branches. Therefore, the MOS capacitor is charged at a fixed rate though the p-channel MOS transistor when the inverter circuit comes back to its initial state. The interesting feature of this delay control mechanism is an approximate linear dependency of frequency on the delay control numbers. This transmitter is capable to generate UWB signal with a central frequency within 3.6-7.5 GHz with an output voltage dynamic of 1 Vpp.

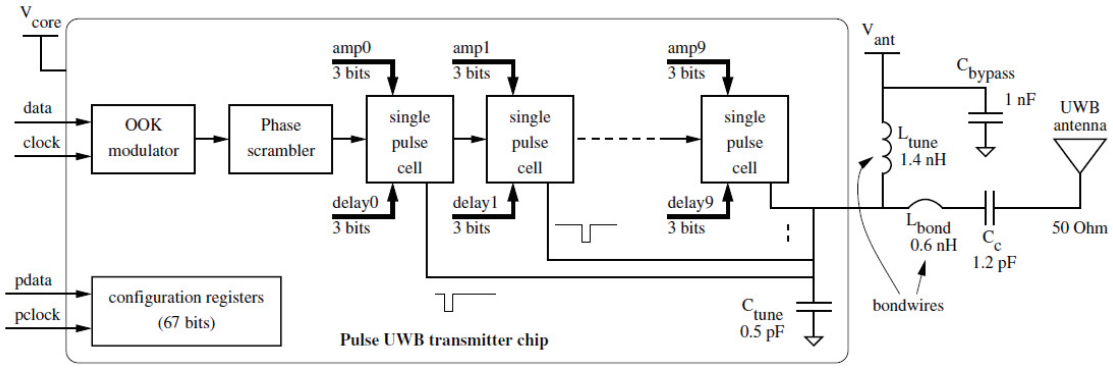


FIGURE 24 – Block diagram of the reported UWB pulse transmitter architecture. From (MIRANDA; MENG, 2010)

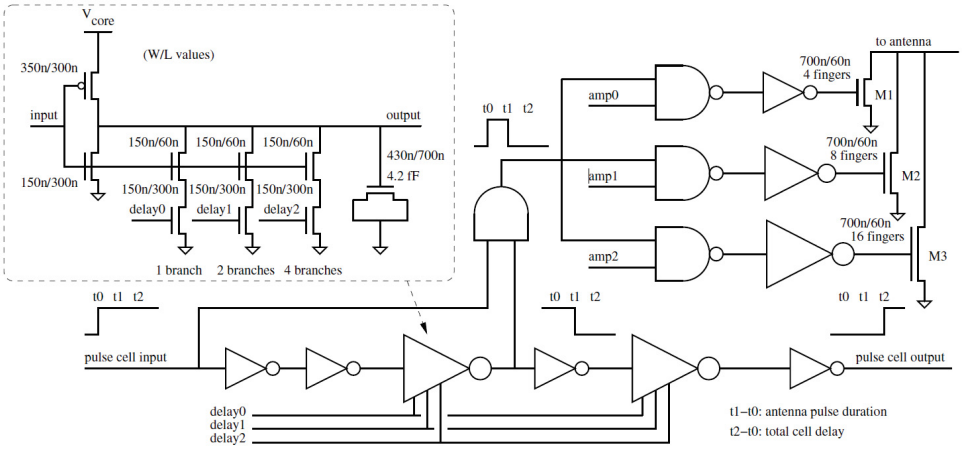


FIGURE 25 – Schematic of the programmable delay line cell. From (MIRANDA; MENG, 2010)

In (VAUCHE; MUHR; FOURQUIN et al., 2017), it is reported an IR-UWB transceiver implemented in a 130 nm bulk CMOS technology for WBAN applications within 3.1-4.9 GHz frequency band. The transmitter design is based on a pulse synthesizer based on delay line and baseband combiner architecture, as displayed in Figure 26. This transmitter is able to tune the amplitude and duration of the generated pulses, and to synthetize the IR-UWB pulse, two circuits of Figure 26 are combined: baseband pulses generator and baseband pulses combiner, whose designed architecture is displayed in Figures 27 and 28 respectively. The baseband pulse generator is composed by two parts, that are a Voltage Controlled Delay Line (VCDL) and a fast logic stage.

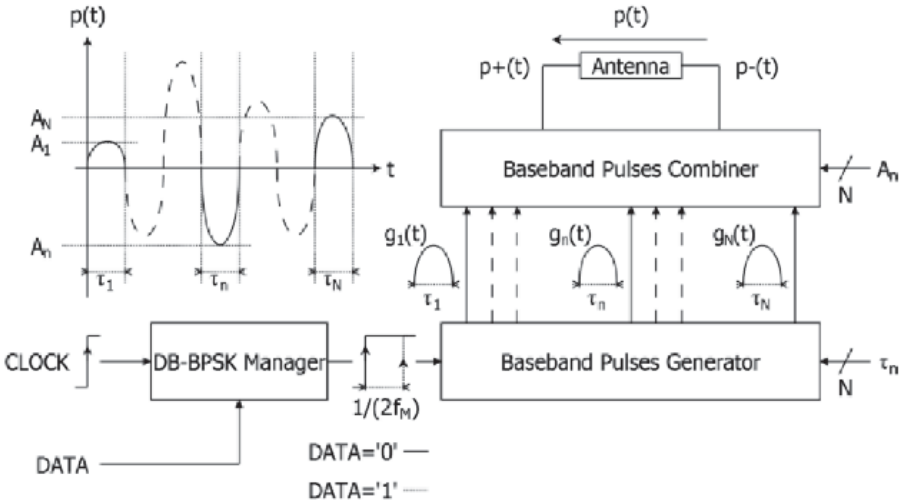


FIGURE 26 – Reported IR-UWB transmitter based on pulse synthesizing technique. From (VAUCHE; MUHR; FOURQUIN et al., 2017)

Concerning the first part of the baseband pulse generator, the VCDL is a delay line where a rising edge signal is propagated through tunable delay cells. These delay cells are composed by two buffered stages whose architecture is based on CMOS logic inverters loaded by a capacitor (D-C1) in series with a n-channel transistor, that implements an analog switch, such that it possible to achieve a wide delay tuning range. Each baseband pulse duration depends mainly on the propagation delay of the different stages of VCDL. The baseband pulse combiner architecture is based on 8 H-bridges paths going into the load (Fig. 28), where each H-bridge path design was done implementing transmission gates (S-M1 and S-M2 of Figure 28). The combined baseband pulse amplitude is controlled via application of different control voltages (Va-n) at each H-bridge path.

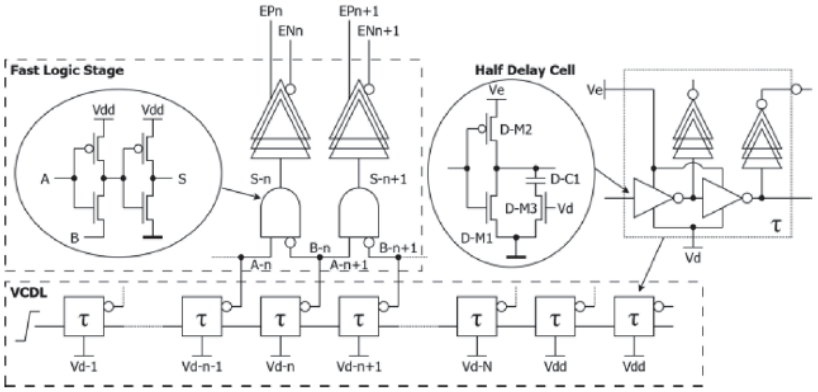


FIGURE 27 – Design of the baseband pulses generator. From (VAUCHE; MUHR; FOURQUIN et al., 2017)

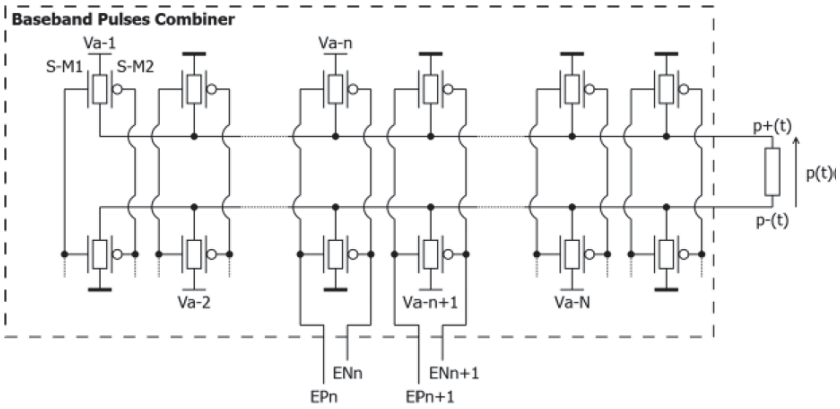


FIGURE 28 – Design of the baseband pulses combiner. From (VAUCHE; MUHR; FOURQUIN et al., 2017)

In (HAAPALA; HALONEN, 2018), it is reported an IR-UWB transmitter front-end, in 65 nm bulk CMOS technology, for energy-harvesting devices, with pulse shaping capabilities and integrated output matching network. This IR-UWB transmitter is capable to generate signals with a central frequency between 6 and 8.5 GHz and its architecture is displayed in Figure 29. The main blocks of the transmitter of Figure 3.6 are delay cells (δ), routers (R), combiners (C), a power amplifier (PA) and a matching network (MN). Figure 3.7 shows the delay cell, router and combiner designs. The delay cells chain, composed by 32 delay cells, generates a pulse that controls the carrier frequency such that:

$$f_c = \frac{1}{t_\Delta} \tag{3.1}$$

Where t_Δ is the propagation delay of a delay unit and is controlled digitally via a 9-bit frequency word. Each delay unit generates an impulse at router input, and the routers propagate an input pulse to up to 4 parallel outputs based on a 4-bit tuning word. The generated pulse from routers are then combined into the combiners, and finally the combined pulses are sent to the PA and the matching network. The architecture of Figure 29 allows to implement only one PA instead of 32 sub-PAs, however the triggering process of combiner rises the power consumption.

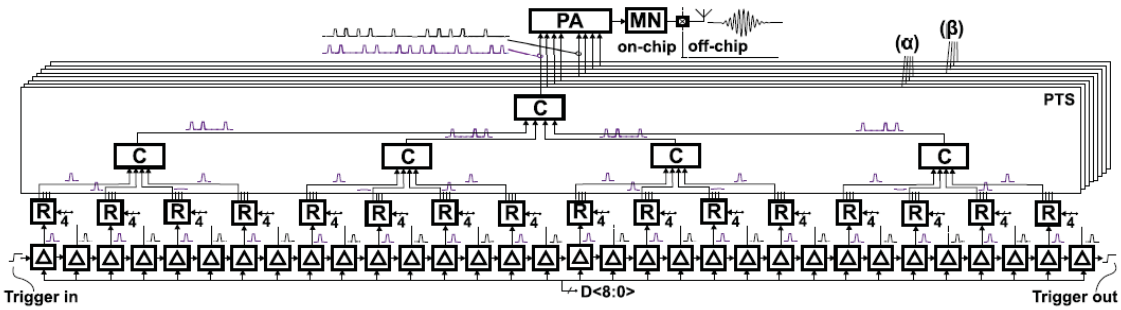


FIGURE 29 – Delay line-based transmitter front-end architecture. From (HAAPALA; HALONEN, 2018)

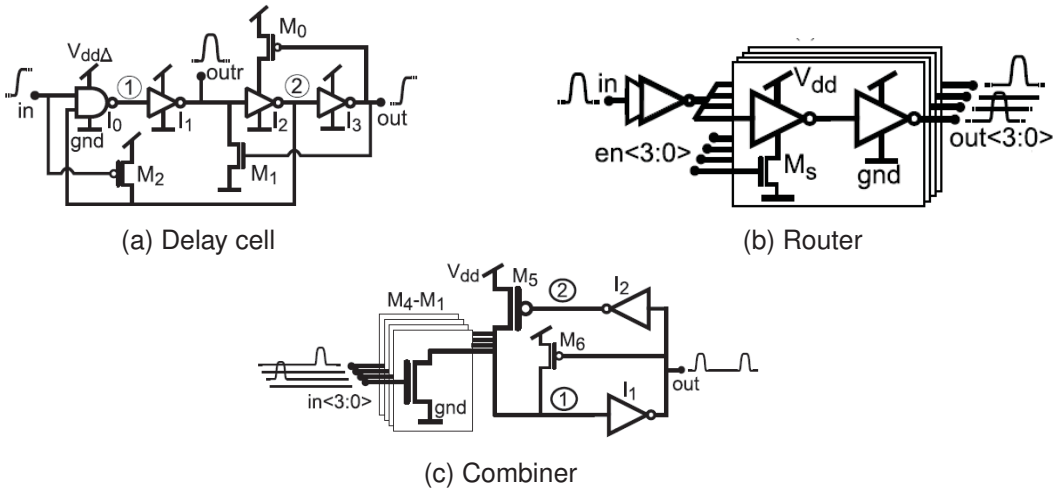


FIGURE 30 – Impulse propagation blocks schematics. From (HAAPALA; HALONEN, 2018)

3.2 PULSE SYNTHESIS BASED ON FREQUENCY TRANSPOSITION

In relation of the second pulse method approached in this chapter, the pulse synthesis based on frequency transposition is realized with circuit composed by a modulated local VCO (Fig. 31). This VCO is modulated by a baseband signal, and it generates a oscillation with the target central frequency. The modulated VCO is able to generate pulse with rectangular shape like the ones of Figures 17, 18 and 19. Nevertheless, for this synthesis technique a pulse shaping circuit should be employed to control the shape of the oscillation generated by the VCO in order generate a UWB pulse compliant to IEEE standards frequency masks and FCC regulations. In this technique, it is feasible to control the oscillator frequency and to turn it on and off with through a baseband signal.

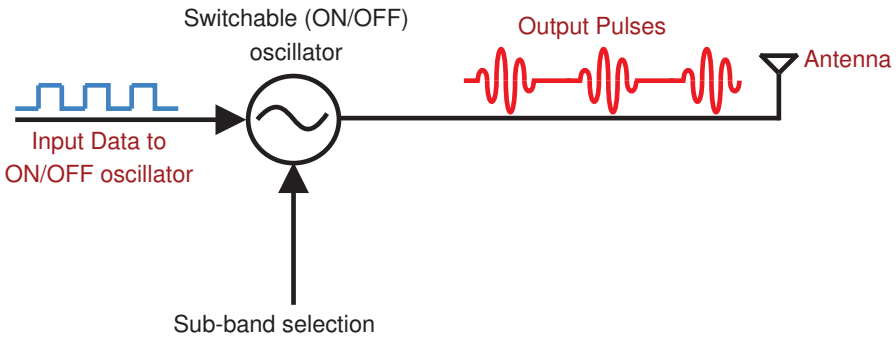


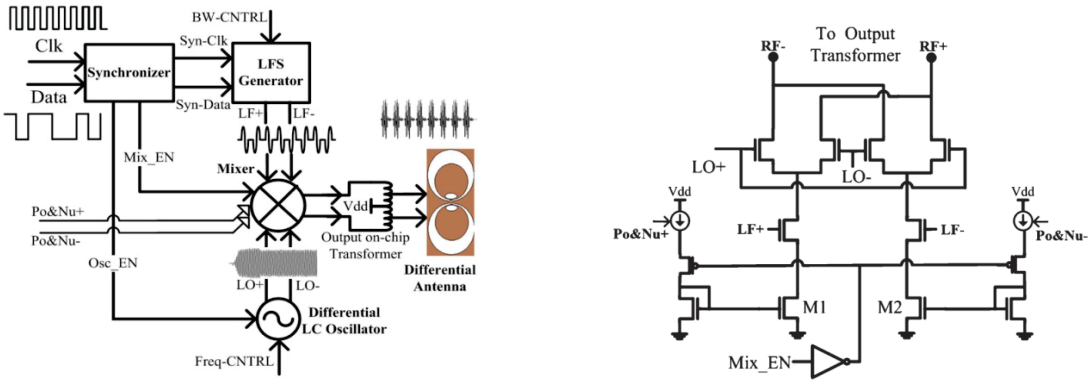
FIGURE 31 – Pulse generator based on gated oscillator schematic principle

Given the fact that a modulated VCO is used, this method is capable to offer better tuning of the pulse frequency bandwidth. To perform a pulse synthesis based on frequency transposition, among the reported strategies, one employs mixers and the other one modulates the VCO through its supply voltage, that are often named gated VCO. In relation of the gated oscillators, their settling time is the critical issue

to cover all the frequency bandwidth of interest, in other words, generate pulses with a duration of order of nanoseconds (IR-UWB pulses). Meanwhile, mixers present a higher power consumption. In this sub-chapter, the addressed pulse generator based on gated oscillator architecture are based on mixers, on LC-tank oscillators and on ring oscillators.

3.2.1 Pulse synthesis based on mixers

In (MIR-MOGHTADAEI et al., 2014), it is reported a gated oscillator modulated by a mixer with fast start-up circuit (Fig. 32a). The circuit of Figure 32a is implemented in 90 nm bulk CMOS technology. The implemented mixer architecture is based on Gilbert cell, that is a type of mixer that produces at its output signals whose levels are proportional to the product of two input signals. Indeed, Gilbert cells are often used for frequency conversion, and they have a interesting feature of having a output current that is a accurate multiplication of differential currents at both inputs. The reported mixer of Figure 32b is capable to isolate the local differential LC oscillator from the differential antenna and matching on-chip transformer. The bias current of Po&Nu+ and Po&Nu- (Fig. 32b) allow to reduce the power leakage of the mixer targeting to compensate the higher power leakage of the LC oscillator of Figure 32a. Moreover, the circuit of Figure 32 is able to perform a BPSK modulation using the pair of monocycle signals LF+ and LF- generated by the low frequency signal (LFS) generator. Therefore, the implemented mixer, the LFS generator and the two control signals (BW-CNTRL and Freq-CNTRL) make feasible to tune the generated IR-UWB pulse frequency response and its waveform shaping. Nevertheless, the major issue of this architecture is the power consumption of the pulse generator, mostly due to mixer power drain.



(a) Gated oscillator modulated by a mixer (b) Mixer composed Gilbert Cell

FIGURE 32 – Pulse generator based on mixer. From (MIR-MOGHTADAEI et al., 2014)

3.2.2 Pulse synthesis based on LC-tank oscillators

Targeting to reduce the oscillator power consumption, one reported strategy is to power up and down directly the oscillator and control the oscillation start through

a power management circuit. Enabling on and off the oscillator during consecutive generated IR-UWB pulses can lead to the oscillator power consumption reduction. In (PHAN et al., 2008), it is reported an oscillator composed by a LC resonator integrated in 180nm CMOS technology (Figs. 33 and 34). The pulse generator of Figure 33 is able to turn on-off the LC oscillator, which allow to generate pulse with particular shapes, like triangular for example that is indicated in Figure 34. To address the target standardized channels, like IEEE 802.15.4, a bank of switched capacitors can be employed to control the oscillations central frequency along with varicap diodes that can be implemented to have a central frequency fine tuning. Nevertheless, the weak points of the pulse generator of Figure 33 are the weak output voltage dynamics (400 mVpp) and the difficulty to generate ultra-short pulses (less than 1 ns), which means that the pulse generate is able only to address channels with bandwidth of 500 MHz. Moreover, LC oscillator has an issue of a of time duration required to have an oscillation amplitude stable.

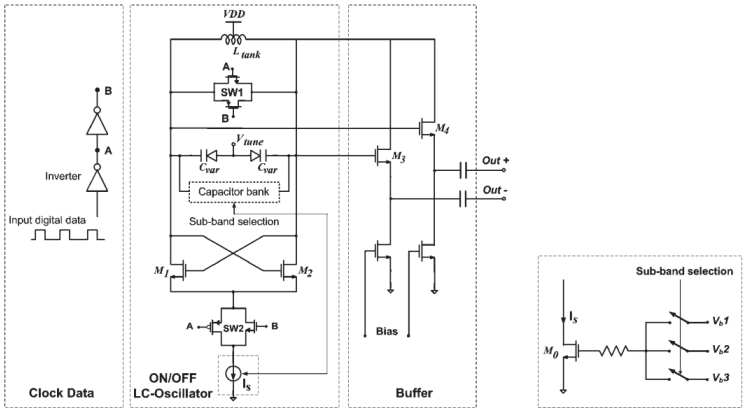


FIGURE 33 – Reported pulse generator based on LC-tank oscillator schematic. From (PHAN et al., 2008)

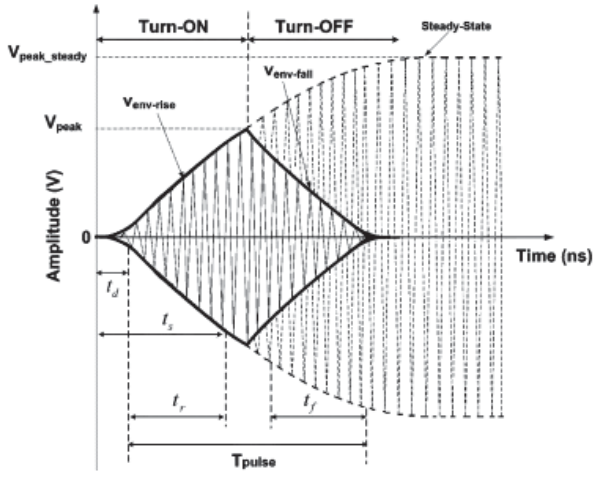


FIGURE 34 – Illustration of oscillator output waveforms. From (PHAN et al., 2008)

In (DOKANIA, R. et al., 2010), it is reported a dual band UWB Impulse Radio transceiver in 90 nm bulk CMOS process for low data rate OOK communications, where

the transmitter architecture reposes on a duty-cycled LC oscillator (Figs. 35 and 36). This LC oscillator can be turned on only when a pulse transmission is requested. The transmitter of Figure 35 generates a pulse with a duration around 2 ns (Fig. 37) and tunable center frequency within 3.3-4.7 GHz frequency band, which means that this system is only able to address the IEEE 802.15.4 and 802.15.6 standards low band channels (Figs. 7 and 9). Given that this transmitter is unable to generate ultra-short pulses (less than 1 ns) mainly due to delay time to oscillation building, it is only able to address standardized channels with a bandwidth of 500 MHz, such this transmitter is not capable to address IEEE 802.15.4 channel 4, despite this circuit is able to generate pulse with a central frequency of 3993.6 MHz, that is central frequency of the IEEE 802.15.4 channel 4. This transmitter was able to generate pulses with a stronger output voltage levels than the oscillator reported in (PHAN et al., 2008), that is between 450 and 600 mV.

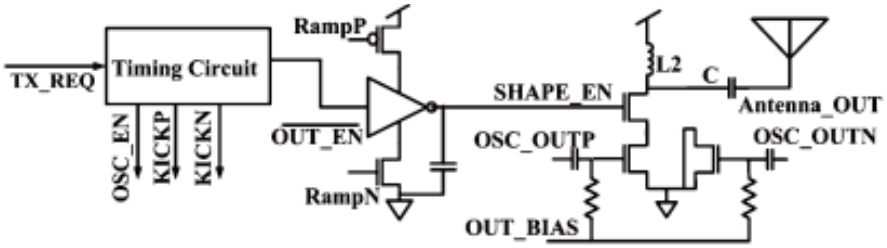


FIGURE 35 – Duty-cycled LC oscillator-based transmitter architecture. From (DOKANIA, R. et al., 2010)

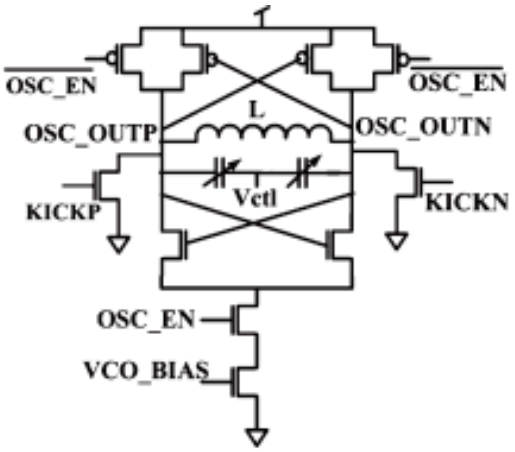


FIGURE 36 – LC oscillator schematic. From (DOKANIA, R. et al., 2010)

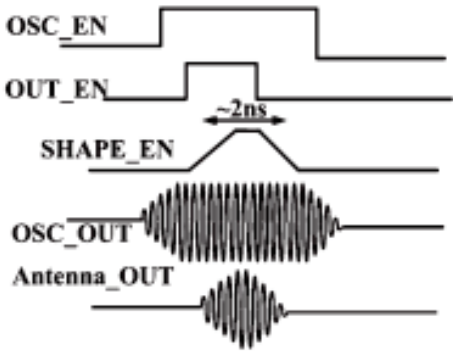


FIGURE 37 – Duty-cycled LC oscillator-based transmitter timing diagram.
From (DOKANIA, R. et al., 2010)

In (SCHMICKL; FASETH; PRETL, 2020), it is reported an IR-UWB transmitter front-end, powered by an RF-energy harvester, in 180 nm CMOS technology (Fig. 38) targeting to comply with European regulations frequency masks (Fig. 5). The transmitter architecture is based on a duty-cycled cross-couple-pair LC oscillator, that generates a single pulse for every rising edge event at V_{trig} signal node. The transmitter of Figure 38 is capable to control the pulses bandwidth, center frequency and amplitude in order to compensate PVT variations. The LC oscillator initializes with an initial voltage on the source-capacitor C_S and it has a time delay around 0.25 ns. The transmitter of Figure 38 generates pulses with center frequency within 5.98-8.80 GHz frequency band using a 6-bit bank of switched capacitors (C). The delay stage has the goal to reshape the input signal V_{TRIG} and to generate two delayed control signals for the n-channel transistors M3 and M4. The pulse duration is determined by the edge-detection circuit formed by the inverters and AND gate. Meanwhile, the transmitter output stage is formed by a programmable current source (bottom part), by a circuit that drives an external output-balun, and by matching control composed mainly by a 6-bit bank capacitor (C_{MP}), that tunes the generated central frequency central, but with lesser influence than 6-bit bank of switched capacitors.

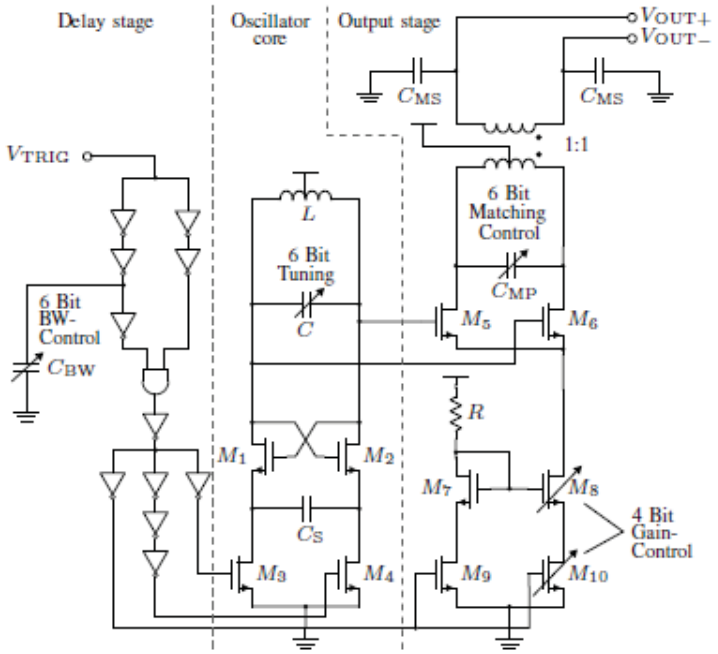


FIGURE 38 – IR-UWB transmitter architecture based on cross-couple-pair LC oscillator. From (SCHMICKL; FASETH; PRETL, 2020)

3.2.3 Pulse synthesis based on ring oscillators

For UWB transmitter design based on gated oscillators, it is also possible to implement ring oscillator, that are capable to boot faster allowing the generation of ultra-short pulses (less than 1 ns) with a good output voltage dynamic. A ring oscillator is composed by odd number of inverter cells, that provides an instability condition to boot the oscillation. Ring oscillator are interesting architecture, since then it does not require neither capacitor nor inductor and is able to provide high frequency oscillations. The frequency oscillation depends on the delay time of the delay cells, such that:

$$f_{osc} = \frac{1}{2N \cdot T_{delay}} \tag{3.2}$$

where N is the number of delay cells within the ring oscillator and T_{delay} the delay time of the delay cell. To control the frequency oscillation, or the inverter time delay, there is the current starving technique that reposes on inverter transistor current control, that influences on delay, rise and fall time of inverters or delay cells. Figure 39 displays an example, where the voltage V_c controls the current that flows into source current that do the inverters transistor biasing. In the other hand, it possible to tune the frequency oscillation in digital manner, where the oscillator is named digital controlled oscillator (DCO). In Figure 40, the oscillation frequency is controlled through a set of tri-state buffer inverters placed in parallel, where the maximal frequency is reached when all inverters are turned on. Since then the boot time of gated ring oscillator is fast, the oscillations present a shape of windowed sinewave of Figure 19. From chapter 2, it is

important to note that signal generated by gated ring oscillations are unable to address IEEE standards masks and are not even considered a UWB signal because its spectrum is not wide enough, such that is necessary a pulse shaping circuit.

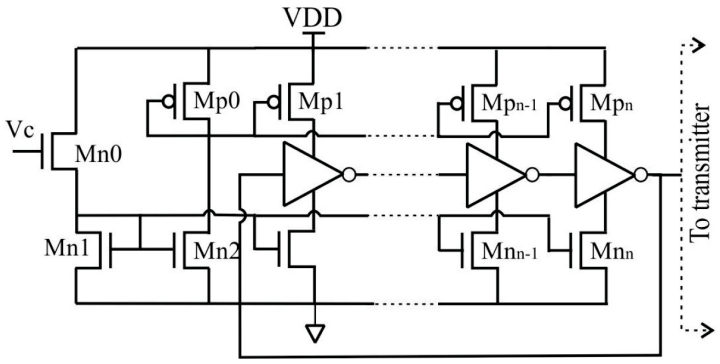


FIGURE 39 – Example of ring oscillator architecture. From (MIRA DA SILVA et al., 2013)

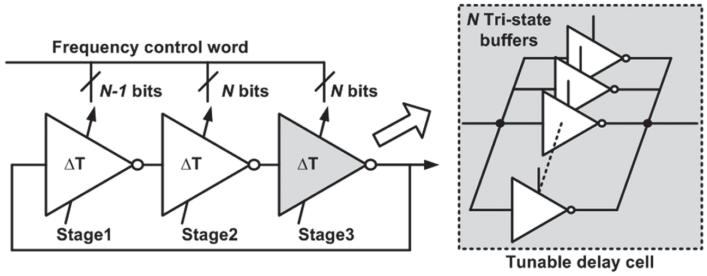


FIGURE 40 – Example of digitally controlled oscillator architecture based on ring oscillator. From (PARK; WENTZLOFF, 2011)

In (ZHAO; LI; WU, 2013), it is reported a UWB transmitter based on on-off voltage-controlled ring oscillator (VCRO) in 180 nm CMOS technology (Fig. 41). The transmitter of Figure 41 is able to generate pulse with a triangular shape of Figure 41, where Figure 42 displays the triangular generator and VCRO schematics. The circuit of Figure 42a is composed by a H bridge (transistors MCa and MCb) and can generate triangular signals, that can be applied into VCRO of Figure 42b through the gate of transistors M8a and M8b. If the transistors M8a and M8b are blocked, the VCRO remains turned off. Otherwise, the VCRO can generate oscillations with a frequency within 3-5 GHz, being able to address the IEEE 802.15.4 and 802.15.6 low band channels. The transmission delay of the VCRO is determined by parasitic capacitances and resistances and by the direct of transistors M10a and M10b. The ring oscillator can achieve a fast-transient response being able then to fabricate an ultra-short pulse.

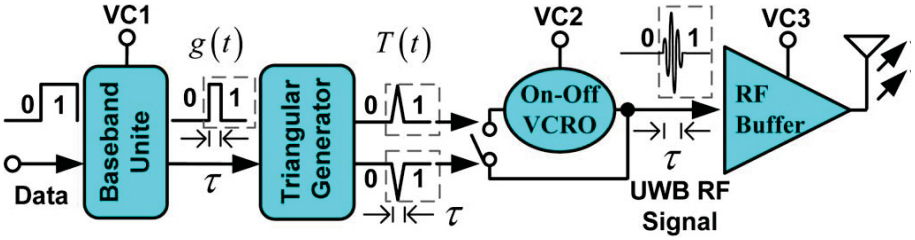
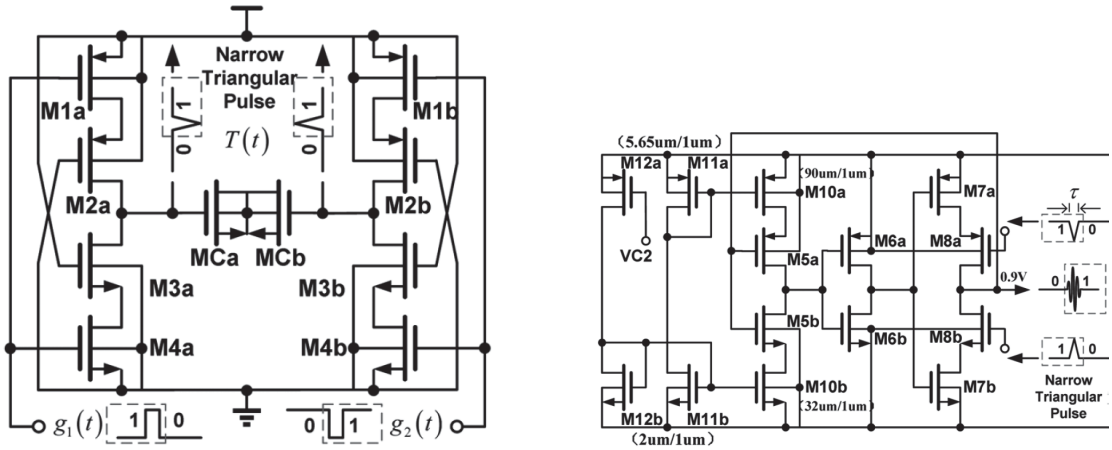


FIGURE 41 – Block diagram of the reported UWB transmitte. From (ZHAO; LI; WU, 2013)



(a) Triangular signal generator (b) VCRO

FIGURE 42 – UWB transmitter main blocks schematics. From (ZHAO; LI; WU, 2013)

In (RYCKAERT et al., 2007), it is proposed an all-digital UWB transmitter architecture, in 90 nm bulk CMOS technology, based on a digitally controlled oscillator (DCO) that produces oscillations between 3 and 10 GHz. The proposed transmitter is able to address the 499 MHz band of IEEE 802.15.4 standard. Figure 43 displays the proposed UWB transmitter general architecture, where is proposed a phase-aligned frequency-locked loop (PA-FLL) for the frequency synthesis for duty-cycled communication. One of the advantages of PA-FLL system is that is possible to turn on the DCO and all dividers only during the burst transmission, hence saving power during two consecutive pulses. Figure 44 displays the DCO of the proposed UWB transmitter, where is proposed 3 methods to control the DCO frequency: coarse-range tuning achieved by a variable current source programmed by a 6-bit code to the biasing, medium-range tuning achieved by a variable capacitor programmed by a 5-bit code to have a short settling time, and finally a fine-range tuning obtained by a variable degeneration resistor programmed by an 8-bit code on the biasing current mirror. Despite the fine tuning of the frequency oscillation, the architecture of Figure 44 is complex to implement due the higher number of bits that control the DCO operation. The burst modulator of Figure 43 combines the signal generated by the DCO and a signal with a frequency of 499 MHz. The transmitter of Figure 43 is able to address the 499 MHz band of the IEEE standard between 3.1 and 10 GHz. Nevertheless, this transmitter is not able to generate

ultra-short pulses that can address IEEE 802.15.4 standard channels with bandwidth greater than 1 GHz (1081 MHz, 1331 MHz and 1355 MHz).

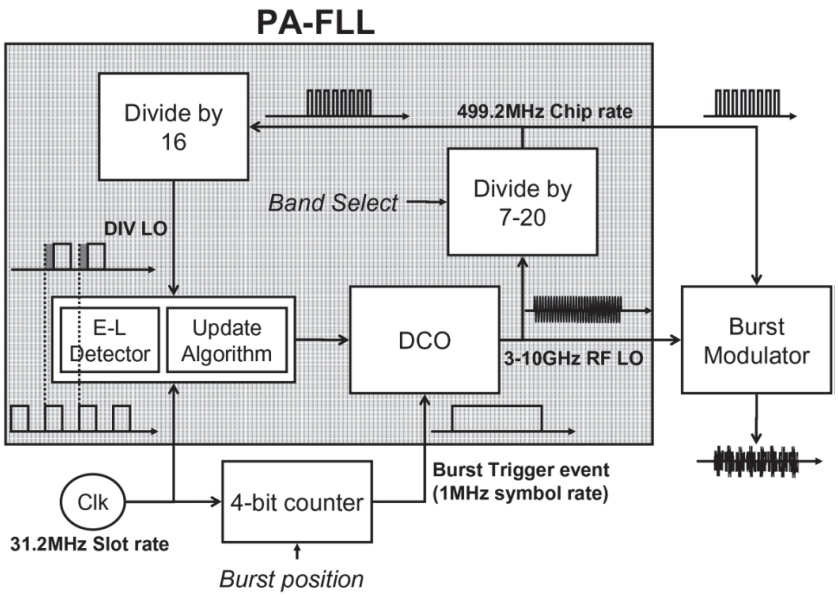


FIGURE 43 – Transmitter general architecture based on PA-FLL. From (RYCKAERT et al., 2007)

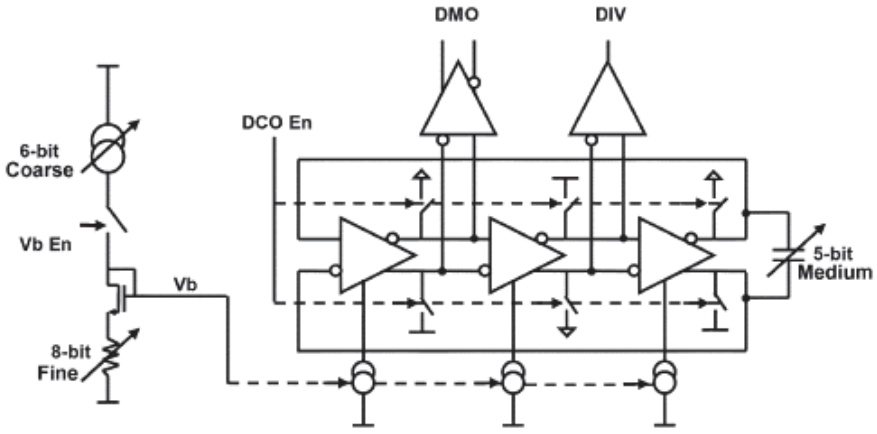


FIGURE 44 – DCO circuit schematic. From (RYCKAERT et al., 2007)

Finally, in (STREEL et al., 2017), it is proposed an IR-UWB transmitter system-on-chip (SoC) in 28 nm FD-SOI CMOS technology with channel selection and digitally programmable pulse shaping. Figure 45 displays the reported transmitter architecture. It exploits a forward back biasing to reduce the MOS transistor threshold voltage, to compensate PVT variations, and to tune the pulse central frequency. The local oscillator is based on ring oscillator of 7 stages (Fig. 46), where the delay of the ring oscillator delay elements is controlled through the forward back biasing instead of current starving technique. The back-bias-controlled oscillator achieves a frequency range between 3.5-4.5 GHz, lower than the circuits reported in (RYCKAERT et al., 2007; VAUCHE; MUHR; TALL et al., 2015). Meanwhile, in terms of power consumption, the transmitter

of Figure 45 presents a energy consumption per pulse of 13.17 pJ, lower than reported circuits based on ring oscillators.

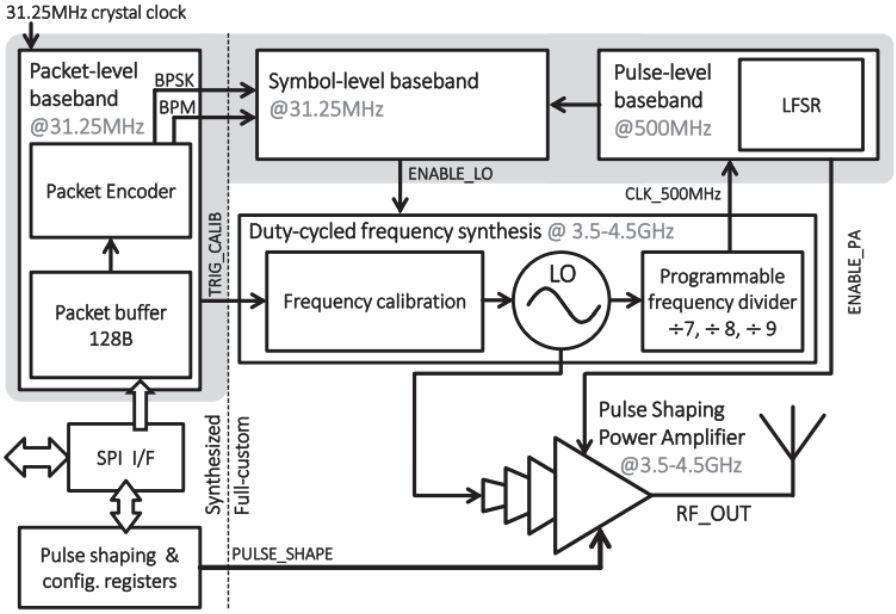


FIGURE 45 – Transmitter architecture. From (STREEL et al., 2017)

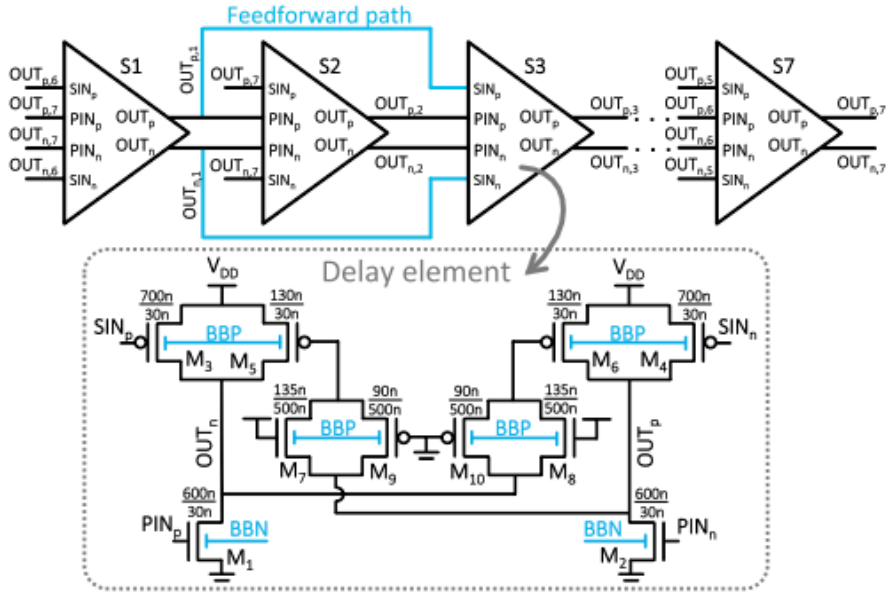


FIGURE 46 – Back-bias controlled ring Oscillator circuit schematic. From (STREEL et al., 2017)

3.3 FD-SOI TECHNOLOGY OVERVIEW

The Fully Depleted Silicon on Insulator (FD-SOI) is a planar process technology capable to exploit the reduced silicon geometries advantages and presents two main attractive features: An ultra-thin layer of insulator, also nominated as buried oxide, placed on the top of the base silicon, and a transistor channel constituted by a very thin silicon,

that is sufficiently thin to not require a doping channel process, therefore characterizing the transistor as fully depleted (Fig. 47) (FEDERSPIEL et al., 2012; WEBER, 2017). This technology is often called as ultra-thin body and buried oxide fully depleted SOI (UTBB-FD-SOI).

Indeed, in order to achieve a better electronic device performance, speed and low power consumption, the transistors are getting smaller. Nevertheless, for the classic bulk CMOS technology, the transistor dimensions sizing down implies in a significant portion of power consumption drained by the leakage current, that is considered undesirable for radiofrequency (RF) CMOS design projects. Meanwhile, the FD-SOI transistor has better electrostatic characteristics and dielectric isolation, that allows it to have improved speed, lower leakage current, better latch-up immunity, fewer noise and greater gain thanks to not-doped channel (ANDRIEU et al., 2010). Besides, the FD-SOI is capable to offer an improved transistor behavior control through the back-gate bias (Fig. 48), similar to the technology bulk body bias, where the back-gate bias could be used to modulate the threshold voltage and then optimize for a targeted application the trade-off between performance and power consumption (PLANES et al., 2012).

In the synthesizer design process, the back-gate terminal of all the transistors is connected to the ground, accordingly the back-gate biasing is not applied in this dissertation.

FIGURE 47 – Bulk CMOS and FD-SOI transistor structures.
From (STMICROELETRONICS, s.d.)

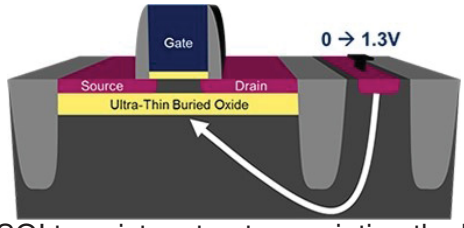


FIGURE 48 – FD-SOI transistor structure pointing the back-gate terminal.
From (STMICROELETRONICS, s.d.)

3.4 PULSE GENERATOR OVERVIEW

Table 5 presents a performance overview of the addressed pulse generators in this chapter. In general, the pulse generator is based either on delay lines or a local oscillator. From Table 5, ring oscillations are more well suited for applications where it is targeted to cover all the 3.1-10.6 GHz and to address the IEEE 802.15.4 and 802.15.6 standardized channels. Moreover, the ring oscillators allow a faster initialization time and an easier frequency tuning. Pulse generator based on mixers or on LC-tank oscillators are not capable to generate ultra-short time, or other words, a pulse with a bandwidth greater than 1 GHz. Meanwhile, pulse generator based on delay lines present a central frequency range around of 4 GHz, being capable to address either the low band or the high band of the IEEE standard. Therefore, for the proposed pulse synthesizer in this dissertation, the local oscillator based architecture with gated ring oscillators is chosen. The essential in this dissertation work is to design a circuit capable to cover the 3.1-10.6 GHz and capable to address IEEE 802.15.4 and 802.15.6 standardized channels. No reported work in Table 5 fully address all IEEE 802.15.4 standardized channels.

TABLE 5 – Comparison with state-of-the-art UWB transmitters

	Miranda 2010	Vauche 2017[±]	Haapala 2020	Moghtadaei 2014	Phan 2008	Dokania 2020	Schmiclk 2020	Zhao 2013	Ryckaert 2007	De Streel 2017
CMOS Tech. (nm)	65 Bulk	130 Bulk	65 Bulk	90 Bulk	180 Bulk	90 Bulk	180 Bulk	180 Bulk	90 Bulk	28 FD-SOI
VDD (V)	1.2	1.2	1.2	1	1.5	1.2	1	1.8	1	1.2
Core Area (mm^2)	0.7	0.11	0.22	0.18	0.30	0.42	0.25	0.08	0.07	0.93
Architecture	DL-based	DL-based	DL-based	LO-based (Mixer)	LO-based (LC)	LO-based (LC)	LO-based (LC)	LO-based (Ring)	LO-based (Ring)	LO-based (Ring)
Spectral compliance	FCC	FCC	ECC	FCC	FCC	FCC	ECC	FCC	FCC	FCC
IEEE 802.15.4 Channel Covered	-	4	5 to 15	-	1 to 3	1 to 3	5, 6, 8, 9	-	All except 4, 7, 11, 15	1 to 3
IEEE 802.15.6 Channel Covered	-	-	3 to 10	0 to 2	0 to 2	0 to 2	-	-	All	0 to 2
Modulation	OOK	OOK + DB-BPSK	OOK	BPSK	OOK	OOK	TR-IR-UWB[†]	OOK	BPSK	2-PPM + BPSK
BW(X=10dB) (GHz)	-	1.8-3.5	0.6	2.4-4.6	0.52[◦]	-	0.5[◦]	1.6	0.5	0.8-1[◦]
F_c range (GHz)	3.6-7.5	3-5	6.5-8.0	5-5.6	3-5	3.5-4.5	6-8.8	3-5	3-10	3.5-4.5
Maximum Magnitude (Vpp)	0.91	0.90	0.46	0.4	0.16	0.49	1	0.26	-	0.7
Impedance Load - Z_L (Ω)	50	100	50	50	50	50	50	50	50	50
Static Power (μW)	13	100	0.38	-	390	5	1.89	-	640	TX: 106[⊗] SoC: 174[*]
Dynamic Energy E_{ac} (pJ/pulse)	8.5	146	63	14.4	16.8	1	6.2	20	40	TX: 10.4[⊗] SoC: 13.2[*]
Emitted Energy - E_p (pJ/pulse)	2.4	0.48	0.83	0.78	0.11	0.84	4.38	0.07	-	0.24
Efficiency - E_p/E_{ac} (pJ/pulse)	15.3	0.32	1.28	2.6	0.63	1.68	4.73	0.35	-	2.33
P_c(PRF = 1 MHz) (μW)[*]	21.50	246	63.38	-	406.80	6	8.09	-	680	TX: 116.4 SoC: 187.2
P_c(PRF = 3.90 MHz) (μW)[*]	46.15	669.4	246	-	455	8.9	26.1	-	796	TX: 146.6 SoC: 225.4
P_c(PRF = 15.6 MHz) (μW)[*]	145.6	2377.6	983.2	-	652	20.6	98.6	-	1264	TX: 268.2 SoC: 379.9
P_c(PRF = 62.4 MHz) (μW)[*]	543.4	9210	3931	-	1438	67.40	388.8	-	3136	TX: 755 SoC: 995.8
Simulation/Mesure	Mesure	Mesure	Mesure	Post-layout	Mesure	Mesure	Mesure	Mesure	Mesure	Mesure

[*] Estimated power consumption.
[±] Paper also includes a receiver.
[◦] Estimated from the reported pulse waveform.
[⊗] Estimated from the paper available data (TX)
[*] Estimated from the paper available data (SoC)
[†] Double Pulse Transmit-Reference

4 CIRCUIT DESIGN

This chapter addresses the proposed IR-UWB pulse synthesizer design targeting to cover 3.1-10.6 GHz bandwidth and to address IEEE 802.15.4 standardized channels. Among the pulse generation techniques and UWB transmitter presented in previous chapter, for the proposed pulse synthesizer, the technique chosen is the one based on frequency transposition, where is employed a fast local oscillator. The oscillator architecture chosen in this dissertation work is the ring controlled oscillator, given that from Table 5, it was observed that this architecture allows to generate pulses with a larger central frequency range, that is sufficiently large to cover the targeted band, and capable to address more IEEE 802.15.4 standardized channels.

The proposed circuit specifications are given as follows:

- Full-custom project
- Cover the 3.1-10.6 GHz band
- Generate pulse with envelope sample & hold
- Have capabilities to tune discrete amplitude pulse duration
- Have capabilities to tune discrete amplitude pulse central frequency
- Have capabilities to shape the pulse by tuning the single pulse amplitude and controlling the amount of single pulses
- Comply with FCC spectral regulations
- Comply with IEEE 802.15.4 standard
- Address IEEE 802.15.4 standards channels (Except channel 0)
- Address IEEE 802.15.6 standards channels

Firstly, a system overview and the deployed technology are presented. Secondly, the circuit main blocks design and their specifications are described and detailed. The technology employed in the circuit is the 28 nm Fully Depleted Silicon on Insulator (FD-SOI) CMOS developed by STMicroletronics. This technology has been chosen because it potentially allows to design a UWB transmitter fully capable to cover the 3.1-10.6 GHz having a low power consumption. Indeed, the FD-SOI technology allows to achieve lesser power leakage.

All the simulations were done in Cadence Virtuoso with the latest design kit version. Moreover, in the circuit design process, it has been considered possible parasitic capacitances in order to perform more realistic simulations. In this chapter, the circuit design blocks and schematics are presented without the parasitic capacitances. The design blocks and schematics that include the parasitic capacitances are addressed in Appendix B.

4.1 SYSTEM OVERVIEW

The proposed IR-UWB pulse synthesizer design is done in this dissertation targeting to comply mainly the FCC regulations and the IEEE 802.15.4 standard spectral masks. In order to be fully capable to address several standardized channels, the proposed circuit in this dissertation must have programmable capabilities such as tuning of generated pulse discrete amplitude, width, and central frequency. The synthesizer design seeks to achieve the least power leakage and the least energy per pulse consumption. The pulse generator architecture is based on frequency transposition technique employing a ring controlled oscillator that targets to generate oscillations whose frequency covers entirely the 3.1-10.6 GHz. From previous chapter, reported oscillators based on ring architecture are more suitable to applications that require a larger frequency band range, if compared with LC oscillators.

The proposed circuit has an architecture based on carrier generation and on envelope shaping circuit (Fig. 49). There are 6 main blocks: VCO Control Module (a), Carrier generation (b), digitally controlled amplifier (DCA) (c), the envelope shaping circuit (d), the dual-band digitally voltage-controlled oscillator (DB-DCO) (e) and a slow memory (f). The blocks (a), (e) and (f) have been done in CMOS logic, whereas the blocks (b) and (c) have been done in CML logic, that is a differential logic family, commonly used in high-date rate integrated systems, that has an advantage to be less susceptible to noise. In relation of the envelope shaping circuit, both architectures done in CMOS and CML logics are studied.

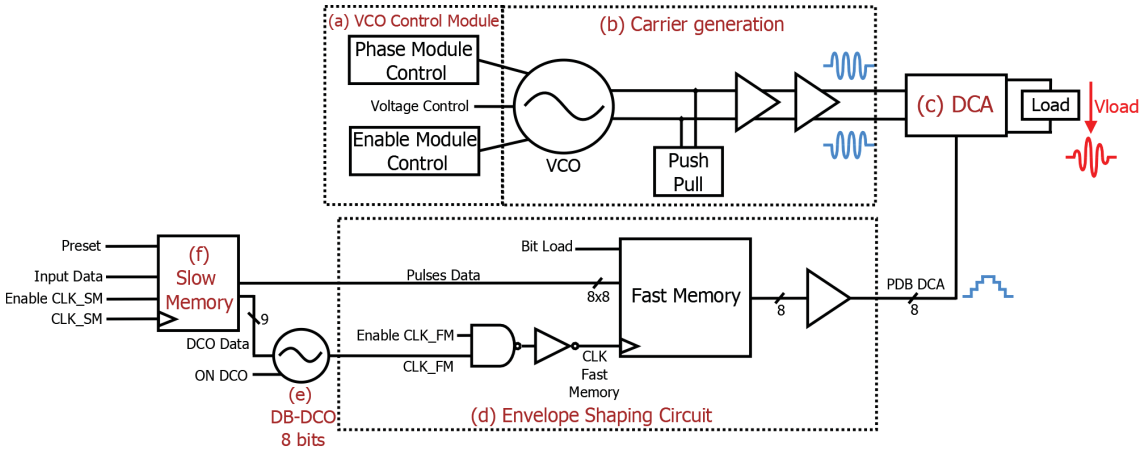


FIGURE 49 – Proposed IR-UWB synthesizer architecture

The carrier generation block (b) is mainly composed by a gated voltage-controlled oscillator (VCO) followed by a buffer stage. The envelope shaping circuit (d) is mainly composed by a fast memory and a buffer stage. There are two memory blocks in this system, the slow and the fast. The slow one works with frequencies of order of 10 MHz and provides at its output signals that address the envelope shaping circuit and the DB-DCO (e), that generate the clock signal for the block (d). Meanwhile, the fast memory is the core of the envelope shaping circuit and works with frequencies of order of few GHz (1-4.5 GHz). The block (c), the DCA, performs a pulse amplitude modulation (PAM) on the carrier signal using the 8-bit bus data from the envelope shaping circuit. The modulated signal is the IR-UWB signal, that presents a sample & hold envelope and a discrete amplitude. Besides, in the proposed architecture, it is possible to turn off the synthesizer when no pulse is transmitted, allowing to save power.

4.2 VCO MODULE CONTROL

The VCO module control, done in CMOS logic, has a goal to control the gated voltage-controlled oscillator (VCO) frequency and phase, and to enable the VCO when necessary. The VCO phase control is based on a BPSK modulation, whereas the VCO drive control on an OOK modulation. The enable and phase control design has been performed using the same transistor architecture (Fig. 50), that is 3 cascaded inverters, generating signals in phase opposition addressing the differential VCO of carrier generation block. In Table 6, the transistors dimensions are displayed. For a single inverter, the width of p-channel transistor is the double of the n-channel transistor in order to have a logic gate with rise and fall time with same values or very closed.

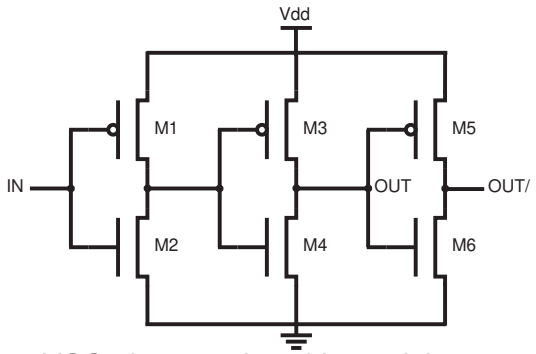


FIGURE 50 – VCO phase and enable module control schematic

TABLE 6 – VCO control modules transistors dimensions

Circuit	Transistor Width (μm)					
	M1	M2	M3	M4	M5	M6
Enable Module Control	4	2	8	4	8	4
Phase Module Control	1	0.5	2	1	2	1

4.3 CARRIER GENERATION

The carrier generation block, done in CML logic, is an analog circuit that has been designed to generated carrier signals, addressing the DCA, with a frequency oscillation within 3.1 – 10.6 GHz. The carrier generation block is composed by a gated VCO, a push-pull and a buffer stage.

4.3.1 Voltage Controlled Oscillator

The gated voltage-controlled oscillator is the carrier generation main block circuit. Its design is based on a ring oscillator architecture whose principle is to propagate a signal on a close loop chain of an odd number of inverters, as indicated in Figures 51 and 52. The odd number of cascaded delay cells, where the minimal is three, provides an instability condition required to the oscillation start. Indeed, a ring with one delay cell is not feasible because the transistor will be self-biased, presenting only a DC component current. As can be noticed in Figure 51, instead of inverters, NAND gates are used as delay cells, which allow to quickly start and stop the oscillations. When one of two inputs of the NAND gate have high logic level, it behaves as a classic CMOS inverter. Besides, the buffer (XOR gate) performs the oscillation phase control, permuting the signal phase in 180 degrees, provides better signal integrity of the oscillator output signal, minimizing the effect of frequency instantaneous variation within the delay cells close loop.

The ring oscillation architecture is interesting given that neither capacitor nor inductor are required, being easier to design, and it can provide high frequency oscillations and multi-phase output.

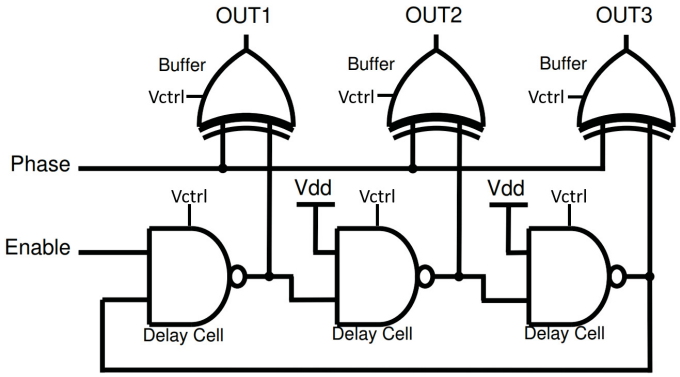


FIGURE 51 – Proposed VCO topology

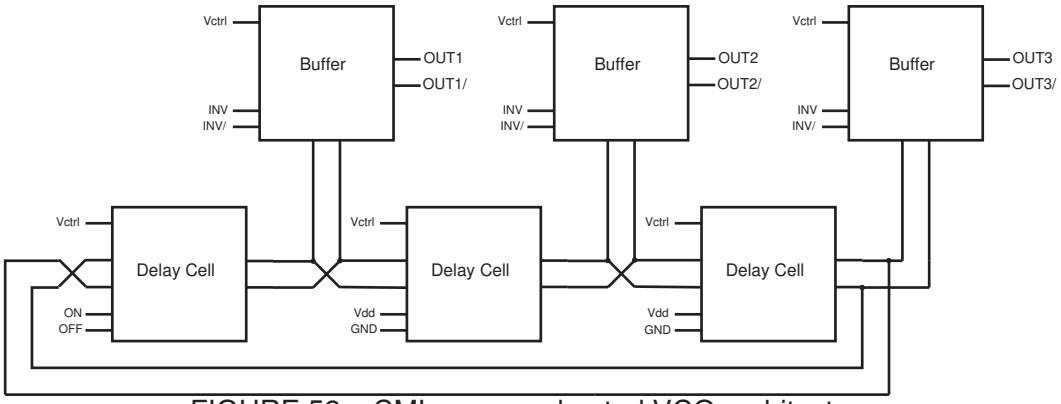


FIGURE 52 – CML proposed gated VCO architecture

The delay cell and buffer cell schematics are addressed in Figure 53. The $Vctrl$ is the voltage control signal. The ON and OFF signals are the output signal of the VCO enable module control, that allow a VCO start-stop command. The INV and $INV/$ signals are the output signals of the VCO phase module control, that allow a BPSK modulation on the signal generated by the VCO. A truth table of the delay cell and buffer cell are displayed in Tables 7a and 7b respectively. The delay cell and buffer cell transistor sizing are indicated in Table 8.

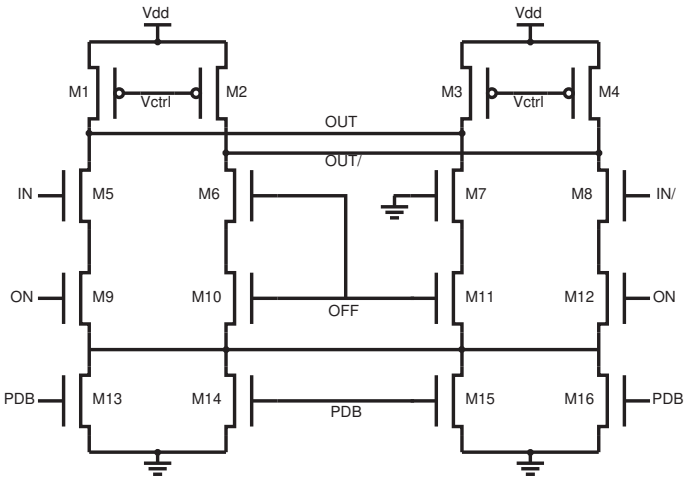
TABLE 7 – VCO main cells truth tables

(a) Delay Cell

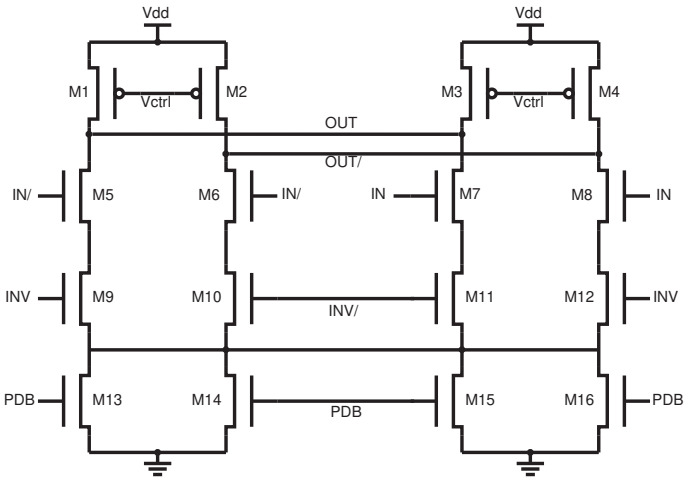
IN	INV	OUT
0	0	0
0	1	1
1	0	1
1	1	0

(b) Delay Cell

IN	ON	OUT
0	0	0
0	1	0
1	0	0
1	1	1



(a) Delay Cell



(b) Buffer cell

FIGURE 53 – Proposed VCO schematics

TABLE 8 – VCO control modules transistors dimensions

Circuit	Transistor Width (μm)			
	M1 to M4	M5 to M8	M9 to M12	M13 to M16
Delay Cell	4	16	32	16
Buffer	1.5	6	12	6

4.3.2 Buffer Stage

The voltage buffer, often named voltage follower, is employed to transfer properly a voltage from a circuit to the following one and to isolate the output signal from one circuit from the input signal of the following circuit, where the buffer has a high output impedance level. In the carrier generation block, two cascaded CML buffers are implemented between the gated VCO and the DCA. Figure 54 presents the buffer CML schematics and Table 9 both buffers transistor sizing. The PD signal means power down, whereas the PDB signal means power up. In the circuit of Figure 54, the p-channel transistors (M1 and M2) and also the n-channel transistor M5 are responsible to execute a power management.

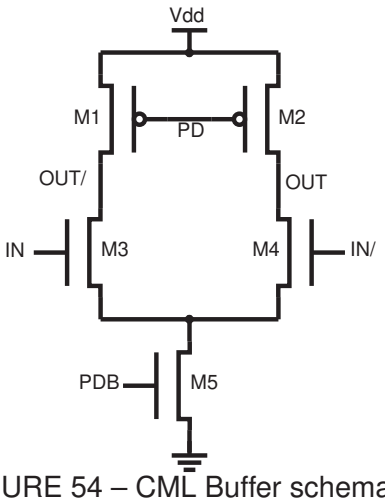


FIGURE 54 – CML Buffer schematics

TABLE 9 – VCO control modules transistors dimensions

Circuit	Transistor Width (μm)				
	M1	M2	M3	M4	M5
First buffer	5	5	10	10	10
Second buffer	10	10	20	20	20

4.3.3 Push-pull

The push-pull, placed between the gated VCO and the buffer stage (Fig. 49), has the goal to amplify the VCO output current, thereby providing an improved signal dynamics and driving capability. The push-pull schematic design is addressed in Figure 55, where the transistors M1 and M2 have a width of 400 nm, whereas the M3, M4 and M5 a width of 800 nm. As same for CML buffer, the signal PD (power down) and PDB (power up) execute the power management of the circuit in Figure 55.

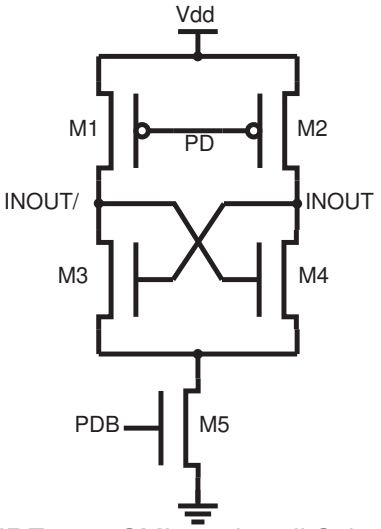


FIGURE 55 – CML push-pull Schematic

4.4 DIGITALLY CONTROLLED AMPLIFIER

A digitally controlled amplifier (DCA) is a circuit that amplifies an analog signal where the gain is defined by a binary bus data. In the IR-UWB pulse synthesizer, it is implemented an 8-bit digitally controlled amplifier in CML logic (Fig. 56). Here, the DCA amplifies the signal generated from the carrier generation block and the discrete gain are set by the 8-bit data bus displayed at the envelope shaping circuit output. In other words, the DCA performs a PAM modulation over the oscillation signal. Thereby, the DCA generates an IR-UWB pulse with discrete amplitude. Since the DCA has 8 bits, there are 256 different discrete amplitude levels for the generated pulse.

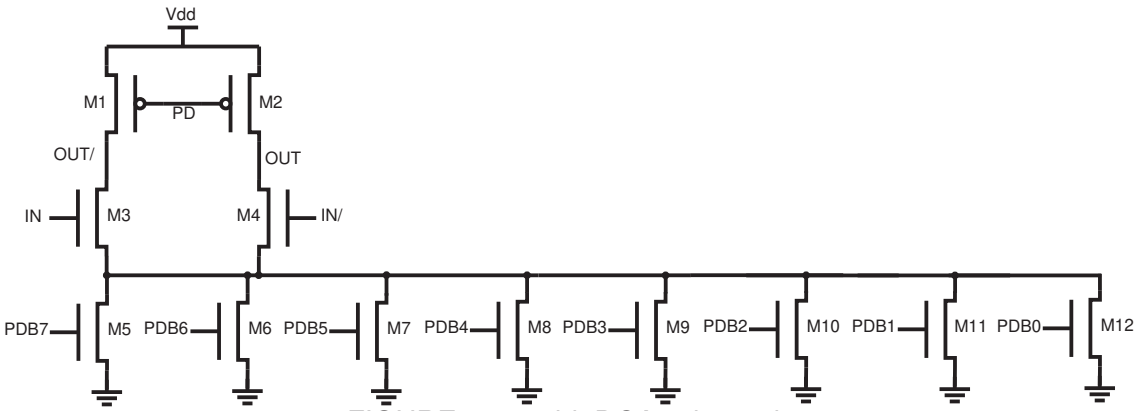


FIGURE 56 – 8-bit DCA schematic

In Figure 56, the signals IN and $IN/$ correspond to the differential signals from the carrier generation block, that is the gated VCO output buffered signal. The signals PDB0 to PDB7 correspond to the 8 bit-data bus from the envelope shaping circuit. Moreover, the signal PD corresponds to power down, that performs a power management of the circuit of Figure 56. Table 10 addresses the DCA transistor sizing.

TABLE 10 – 8-bit digital to analog converter transistor sizing

Transistor width (μm)									
M1 and M2	M3 and M4	M5	M6	M7	M8	M9	M10	M11	M12
48	96	48	24	12	6	3	1.5	0.75	0.325

The amplifier digital gain is tuned through the transistors M5 to M12, that are current sources, and their gate terminal is connected to the 8-bit bus data from the envelope shaping circuit (PDB0 to PDB7). PDB0 is the least significant bit, whereas PDB7 is the most significant bit. From the transistor M5 to M12, the values of their width follow a finite geometric progression with a common ratio of 0.5, where the transistor drain current contribution is proportional to the transistor width length ratio (W/L), where all these transistors have the same length (30 nm). Moreover, the transistors M5 to M12 are equivalent to one transistor with a width of 96 μm. Merging the transistors M5 to M12 into one single transistor, a circuit of Figure 54 is implemented.

To generate an IR-UWB pulse with rectangular envelope shape, one current source transistor is only required, due the fact that 2 discrete amplitudes are enough to achieve this envelope shape. The circuit of Figure 54 can be applied to generate an IR-UWB pulse with rectangular envelope shape. Nevertheless, for envelopes with a more complex shape, like the sample & hold, that are applied in the proposed circuit, require a DCA with higher resolution, hence more current source transistors. A DCA of 8 bits is implemented targeting to generate pulses that fits properly within IEEE 802.15.4 standardized spectral masks (Fig. 8). A higher resolution allows to reprogram more precisely the pulse shaping given the process, voltage, and temperature (PVT) variations.

4.5 ENVELOPE SHAPING CIRCUIT

In this dissertation, the envelope shaping circuit is digital circuit whose output is an 8-bit data bus, that addressed the 8-bit DCA, tuning the IR-UWB pulse amplitude level. The envelope shaping is performed via a 64-bit memory composed by parallel shift registers with parallel loading. Figure 49 displays the main elements of the envelope shaping circuit block: an AND logic gate (NAND Gate followed by an inverter), a fast memory, and a buffer stage. The fast memory works a frequency of order of few GHz.

Among the envelope shaping circuit input signals, the pulses data is a 64-bit data bus, or 8-byte data bus provided from the slow memory, where each byte corresponds to one sampled pulse amplitude levels. Other input signal is the clock signal generated by the DB-DCO, and another one is the load bit pulse, that defines when the fast memory loads the 8-byte data bus from the slow memory. Figure 57 displays the chronograms of the envelope shaping circuit, where D0 to D7 corresponds to sampled pulses amplitude level codified in 8 bits.

When no pulse is transmitted, the PDB 8-bit bus has null value. The NAND Gate followed by an inverter control if the signal clock arrives at the fast memory. If the signal EnableCLK has a low logic level, the fast memory clock signal has a low logic level, otherwise, is has the same logic level of the external clock signal. As seen in Figure 57, the enable clock signal has a high logic level for 8 clock cycles. The load bit pulses signal and enable clock signal should not have high logic level at same time to ensure that the pulse shaping process is done properly.

Besides, the clock signal, generated by the DB-DCO, has a period corresponding to one sample pulse duration. Table 11 displays sample & hold envelope pulses parameters that are considered on envelope shaping circuit and DB-DCO design process. Indeed, the sampling frequency values influences on DB-DCO design, while the number of pulses on envelope shaping circuit, mostly on fast memory design. A number of samples of 6 is enough to achieve a pulse shaping capable to have a pulse spectrum

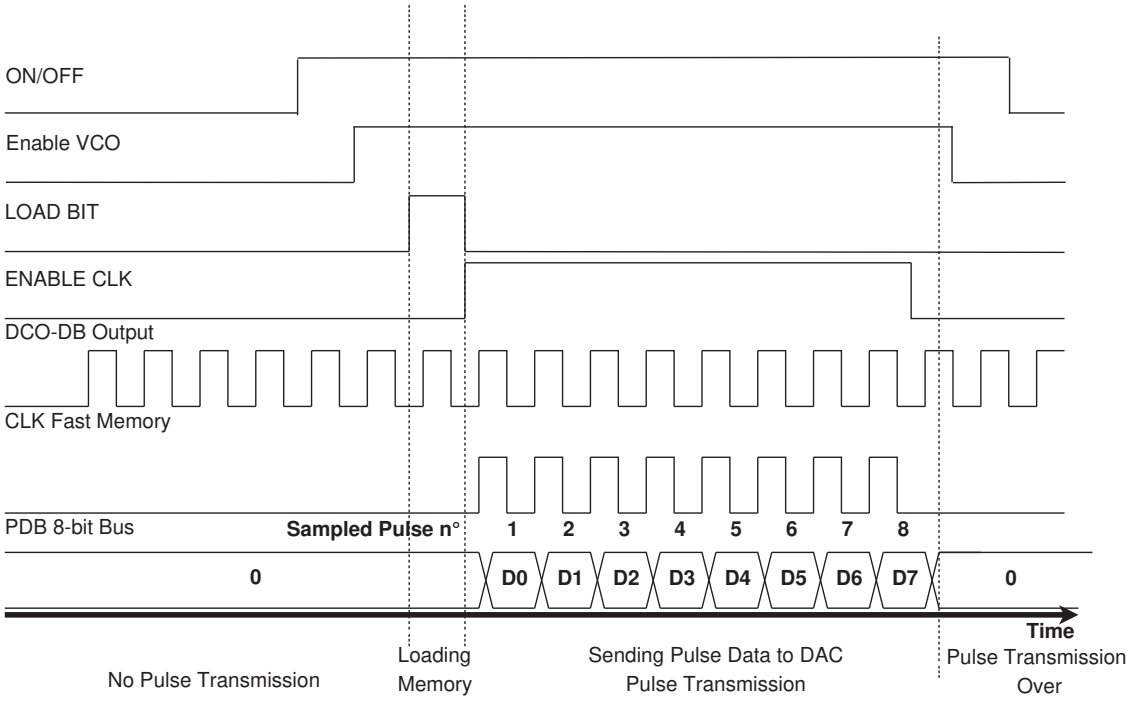


FIGURE 57 – Chronograms of the envelope shaping circuit

fitting into IEEE 802.15.4 and 802.15.6 masks.

Figure 58 displays the sampling frequency of the sample & hold envelope pulses, that correspond to clock frequency of the envelope shaping circuit. Given the pulse parameters of Table 11, the envelope shaping circuit design targets a good performance until 4.5 GHz of clock frequency (at least period of 222 ps).

TABLE 11 – Sample & hold pulse parameters

$BW_{X=3dB}$	T_{sample} (ps)	Number of samples	T_{pulse} (ps)	Sampling Frequency (GHz)
499	626	6	3756	1.60
1081	235	6	1404	3.37
1331	297	6	1410	4.27
1355	231	6	1386	4.33

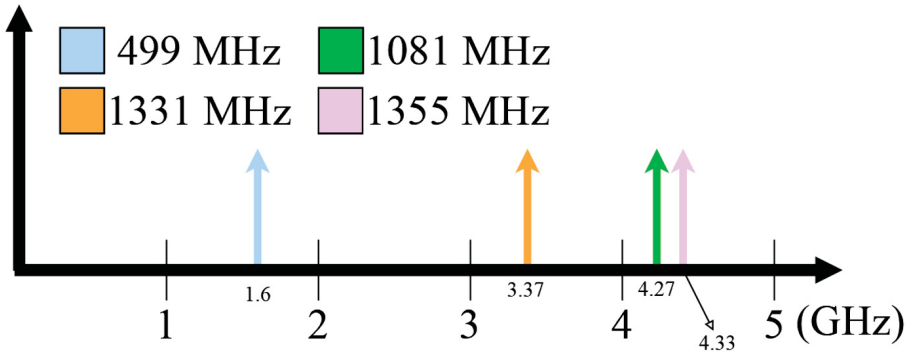


FIGURE 58 – Sample & hold envelope sampling frequency plan

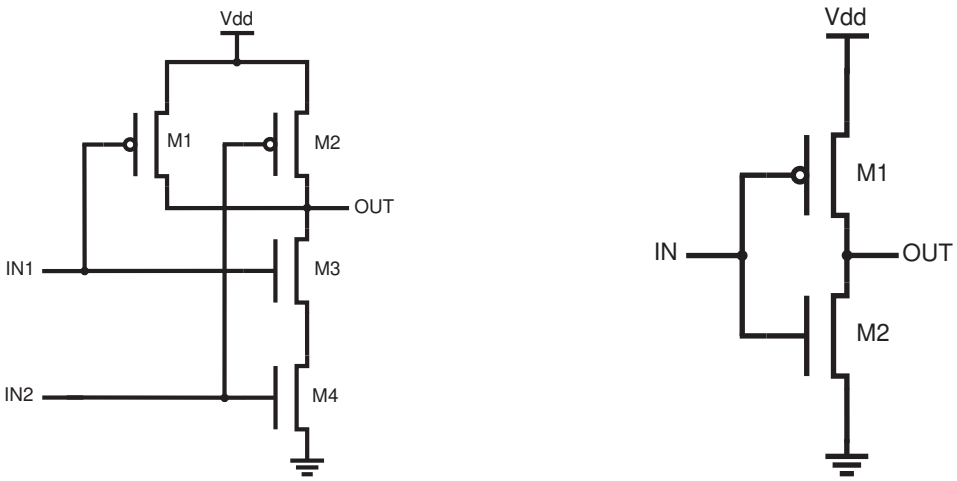
In this dissertation, several architectures of the fast memory that is the core block of the envelope shaping circuit are approached and studied. These are based

either on CMOS flip-flops or on CML flip-flops. The aim here is to find the architecture that achieves the lowest power leakage and the lowest power consumption.

The logic gates displayed inside the envelope shaping circuit in Figure 49 are a NAND gate followed by a logic inverter, whose schematics are displayed in Figure 59. All the transistors of the NAND gate (Fig. 59a) have a width of 8 μ. Regarding the inverter (Fig. 59b), the M1 and M2 transistors have a width of 11 μm and 5 μm respectively. The transistor sizing has been done targeting to equilibrate transistors, such that the rise time and fall time of the logic gate output signal present close values. Indeed, to equilibrate the transistors of logic circuit, it is necessary to find to parameter β that allows to achieve approximate rise and fall time, where the parameter β is given below:

$$\beta = \frac{W_p/L_p}{W_n/L_n} \tag{4.1}$$

where W_p and L_p are the equivalent width and length of p-channel transistors respectively, and W_n and L_n are the equivalent width and length of n-channel transistors respectively. For the NAND gate of Figure 59a, given there are two n-channel transistors in series (M3 and M4), the L_n has the double value if compared with L_p. The value of factor β that allows to equilibrate the MOS transistors for given logic circuit is found often in the interval between 2 and 3. The factor β chosen for circuits from Figures 59a and 59b are respectively 2 and 2.2.



(a) NAND (b) Inverter

FIGURE 59 – Logic gates schematics

4.5.1 Fast Memory

The fast memory is the core of the envelope shaping circuit and works with a clock signal with a frequency between 1 GHz and 4.5 GHz. This circuit loads the 8-byte data bus from the slow memory, responsible for the storage of the pulses data,

and provides at its output a 1-byte data bus that addresses the DCA. The fast memory design is based in 8 parallel shift registers (Fig. 60), where the bit load and clock signals address all the 8 shift registers, that are loaded in a parallel manner, when the bit load signal has a high logic level. Concerning the 8-byte input data bus, the bit of each byte addresses one shift register, the bit the following shift register, successively until the bit 7 that addresses the last shift register.

The shift register is mainly composed by D flip-flops. The first sampled pulse data load the last flip-flop, whereas the last sampled pulse data the first flip-flop. For example, considering that BitLoad signal has a high logic level, if dataP7 signal has a high logic level, the first flip-flop will be set, hence its output signal will have a high logic level. However, if the dataP7 has a low logic level, the flip-flop will not be set. After the shift register load, the pulse amplitude data will propagate though the D flip-flops. After 8 clock cycles, all flip-flops will have an output signal with a low logic level.

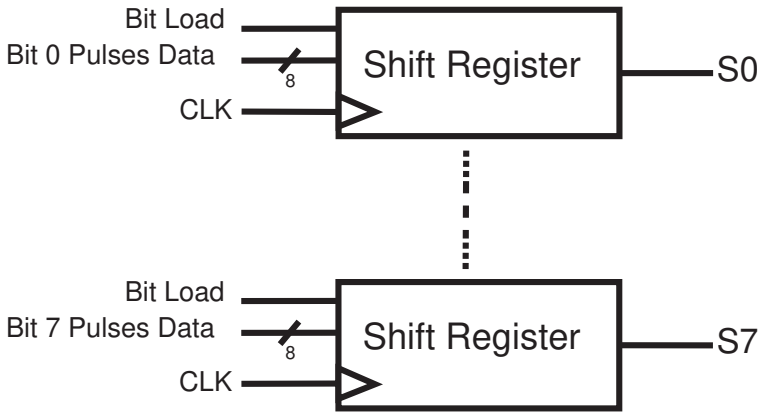


FIGURE 60 – Fast Memory Design

Several architectures of fast memory are approached and studied, where the difference between them is the D flip-flop architecture. The flip-flop addressed architecture in this dissertation are either based on CMOS flip-flops or CML flip-flops. The goal here is to observe which of them presents better power efficiency, mostly in terms of leakage power.

4.5.1.1 Based on CMOS flip-flops

In this sub-chapter, CMOS D flip-flops are addressed. The shift register, indicated in Figure 61, are composed by cascaded 8 CMOS flip-flops, and logic gates as buffer, inverter, and NAND gate. The shift register of Figure 61 is edge triggered and has active high asynchronous preset and reset. The input of the first flip-flop is connected to the ground, which means after the shift register loading process and the 8 clock cycles all the flip-flops will display at their output a low logic level signal. The NAND gate and inverter from Figure 61 are responsible to generate the signal that will

set these 8 flip-flops, or other words, load the shift register and therefore load the fast memory. Therefore, the circuit from Figure 61 is a shift register with parallel input and serial output (parallel-in, serial-out), where only the output of the last flip-flop is used in a following circuit, that is the envelope shaping buffer stage.

The AND gate and inverter schematics are the same of Figure 59. Moreover, the buffer circuit (Fig. 62) from Figure 61 is implemented to improve the circuit fan out and provide a better clock signal integrity. Table 12 displays the transistor sizing of the NAND gate, inverter, and buffer of Figure 61. Indeed, the transistors sizing has done aiming to have equilibrated transistors with a factor β of 2.

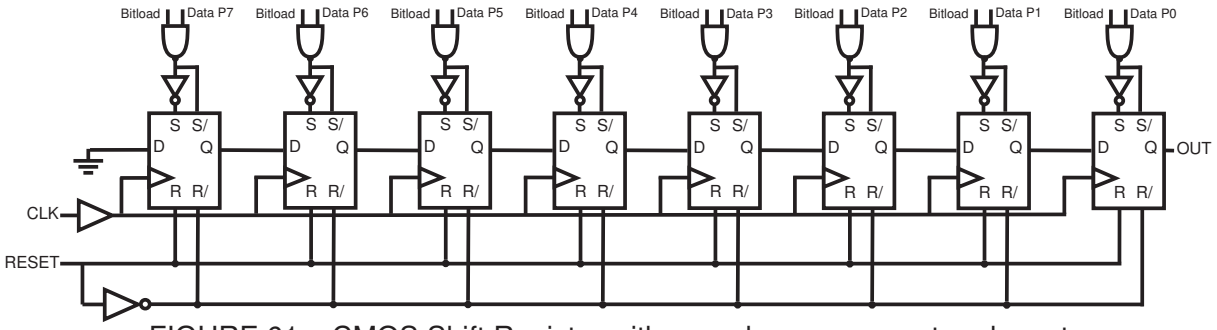


FIGURE 61 – CMOS Shift Register with asynchronous preset and reset

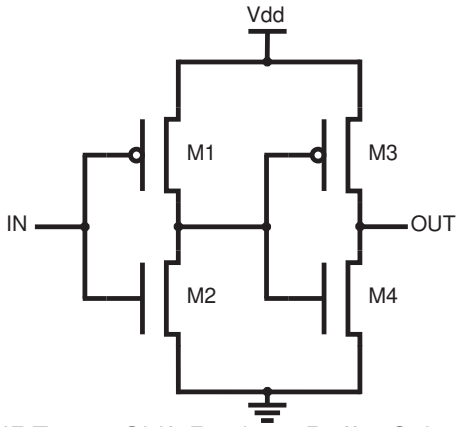


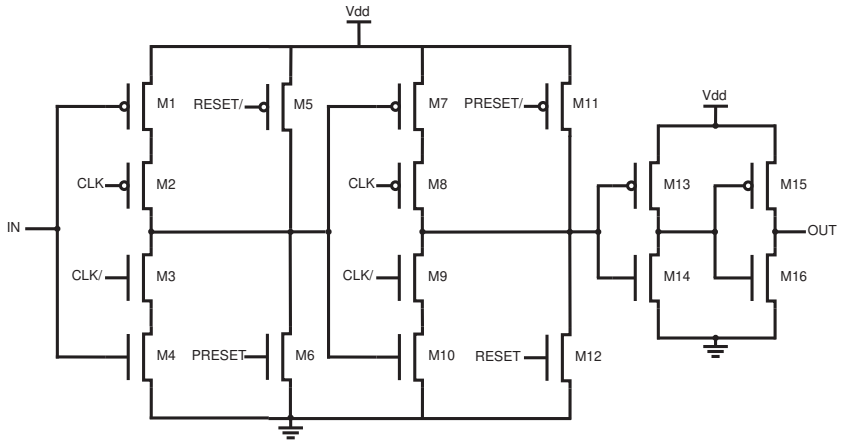
FIGURE 62 – Shift Register Buffer Schematic

TABLE 12 – Buffer, inverter, and NAND gate transistor sizing

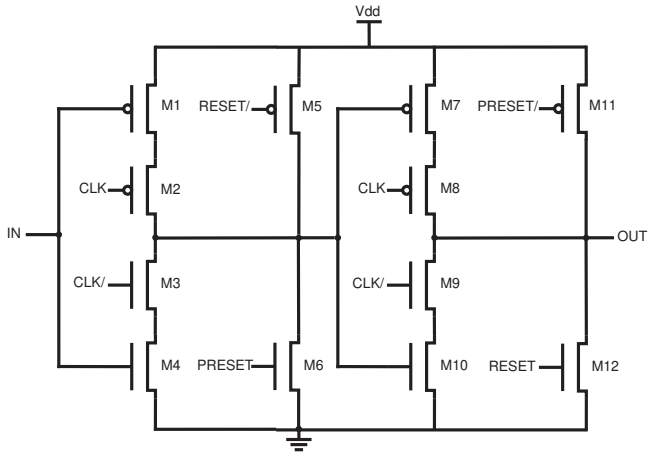
	Transistor width (μm)			
Buffer	M1	M2	M3	M4
	9	4	14	7
NAND gate	M1	M2	M3	M4
	4	4	4	4
Inverter	M1		M2	
	2		1	

Concerning the D flip-flops, the main circuit of the shift register of Figure 61, they are based on CMOS logic, activated by positive rising clock edge, and has active

high asynchronous preset and reset. Their proposed schematics are displayed in Figure 63. The flip-flop preset has logic high level when the occurs the fast memory loading process, or when bit load signal goes to high logic level. Meanwhile, the flip-flop reset has high logic level when no pulse is transmitted. The transistors (M5 and M12) are responsible to reset the flip-flops of Figure 63 are implemented because without them, there are fluctuant nodes at flip-flop output, which may rise the power consumption, despite the pulse generator is turned off. The flip-flop of Figure 63a presents a buffering stage, whose goal is to improve the flip-flop output signal integrity, reducing the signal oscillations. However, the inconvenient of the buffering stage is the fact that it rises the power leakage of the flip-flop. Table 13 addresses the transistor sizing of the circuit from Figure 63.



(a) With buffering stage



(b) Without buffering stage

FIGURE 63 – CMOS high asynchronous reset and preset flip-flop schematic

TABLE 13 – CMOS high asynchronous reset and preset flip-flop transistor sizing

Transistor width (μm)							
M1,M2,M7,M8	M3,M4,M9,M10	M5,M11	M6,M12	M13	M14	M15	M16
2	1	1	0.5	4	2	8	4

Figure 64 shows another CMOS flip-flop, but implemented with 2 latches master

and slave, that are composed by NAND gates of 2 and 3 inputs. Figure 65 displays the latch schematic and Figure 66 the 3 input NAND gate schematic. The schematic of 2 input NAND gate from Figure 65 is the same from Figure 59a and of inverter from Figure 65 is the same from Figure 59b. Table 14 addresses the transistor sizing of the circuit from Figure 65 and 66. Note that to equilibrate the transistors of the logic circuits from Figure 65, a parameter β calculated is 2.4.

The flip-flop of Figure 64 is activated by positive rising clock edge and has active high asynchronous preset. This flip-flop does not present asynchronous reset like the flip-flop from Figure 63, because the architecture of the latch from Figure 65 does not have the issue of fluctuant node. In Figure 65, the 3 input NAND gate are responsible to preset the latch, accordingly, preset the flip-flop from Figure 64.

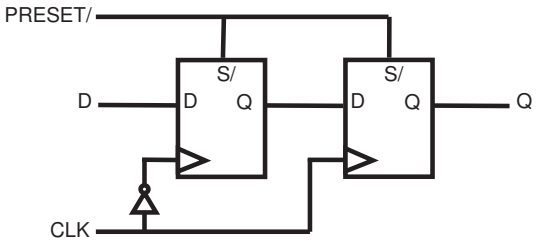


FIGURE 64 – CMOS high asynchronous preset flip-flop schematic

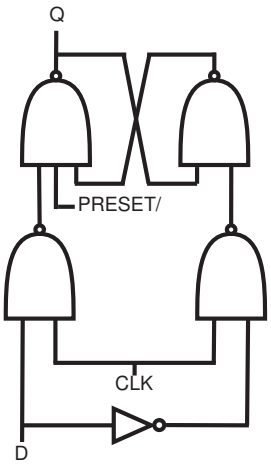


FIGURE 65 – CMOS high asynchronous preset latch schematic

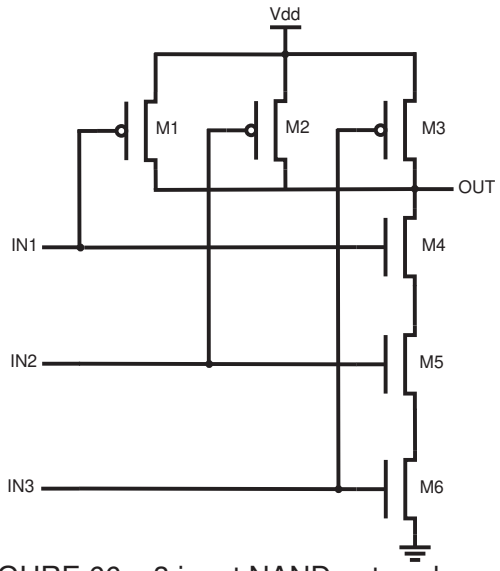


FIGURE 66 – 3 input NAND gate schematic

TABLE 14 – CMOS high asynchronous preset latch schematic transistor sizing

	Transistor width (μm)					
2-input NAND	M1	M2	M3	M4		
	4.8	4.8	4	4		
3-input NAND	M1	M2	M3	M4	M5	M6
	4.8	4.8	4.8	3	3	3
Inverter	M1		M2			
	2		0.840			

The CMOS flip-flop of Figure 64 are implemented in the 8-bit shift register, whose schematic is displayed in Figure 67, that is version of the circuit from Figure 61 without the asynchronous reset.

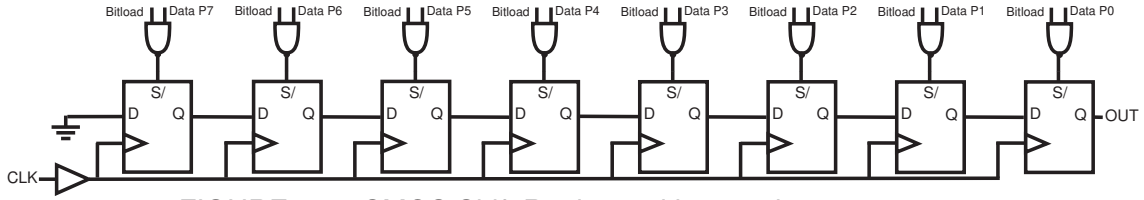


FIGURE 67 – CMOS Shift Register with asynchronous preset

4.5.1.2 Based on CML flip-flops

In this sub-chapter, D flip-flops done in current mode logic (CML) are addressed. As well for CMOS logic, the shift register is composed by 8 cascaded CML flip-flops, and logic gates done in CMOS logic as buffer, inverter, and NAND gate. Figure 68 displays the shift register done with CML flip-flops. The differences between the shift register done with CMOS flip-flops (Figs. 61 and 67) and the one from Figure 68 are the flip-flops architecture and transistor sizing, and the presence of node power down

(PD) that performs the circuit power management. The buffer, 2 input NAND gate and inverter displayed in Figures 64, 67 and 68 present the same architecture and transistor sizing (Table 12). The goal here is to observe which flip-flop architecture, among the approached ones in this dissertation, is capable to achieve the better performance in terms of power drain.

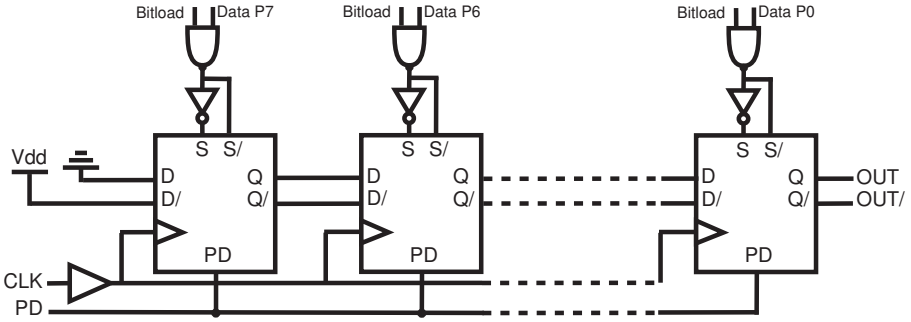


FIGURE 68 – CML Shift Register with asynchronous preset

The flip-flops from figure 68 are implemented with 2 latches master and slave. Figure 69 shows the CML flip-flop schematic and Figure 70 CML latch schematic. The flip-flop from Figure 69 presents the node PD (power down) that does the circuit power management, and differential input, output, and preset signals. The p-channel transistors M1 and M2 of Figure 70, whose gate is connected to power down, performs the power management of the latch of Figure 70. When power down signal goes to high logic level, the latch is turned off. To avoid short circuit in this CML latch, when preset signal goes to high logic level, the PD signal should have high logic level signal. In particular, if power down signal and preset signal have high logic level, the transistors M1 and M9 of Figure 70 allow a short circuit between voltage supply node and ground. Table 15 address the transistor sizing of circuit of Figure 70.

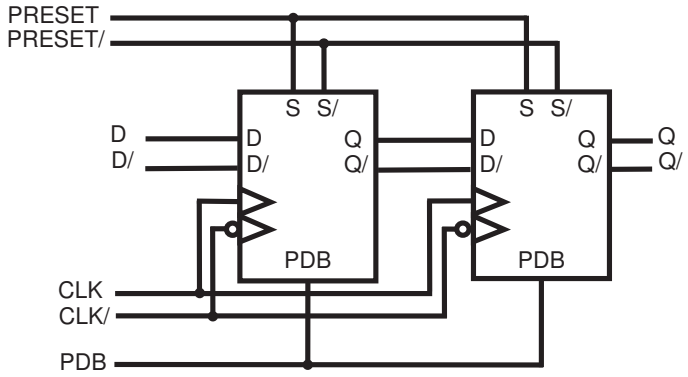


FIGURE 69 – CML high asynchronous preset flip-flop schematic

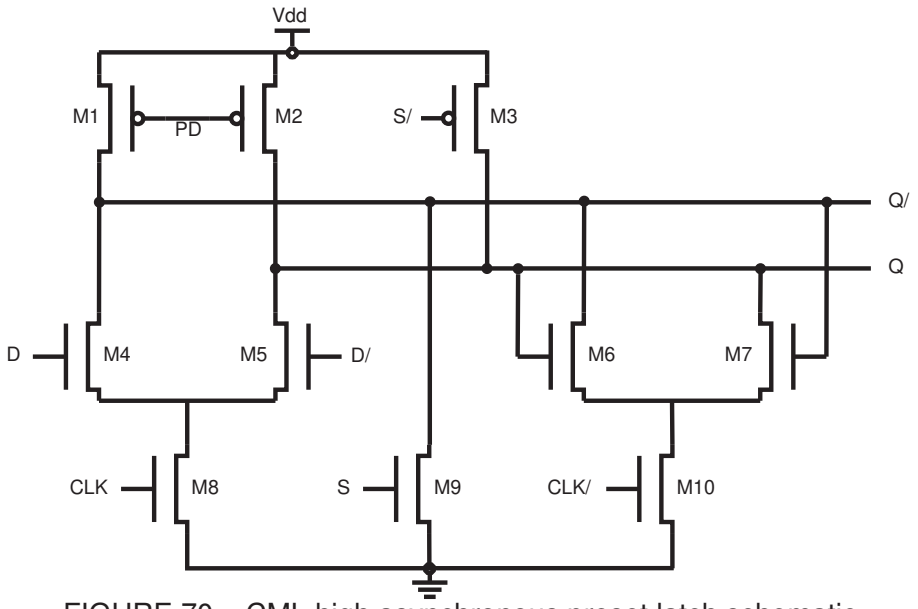


FIGURE 70 – CML high asynchronous preset latch schematic

TABLE 15 – CML high asynchronous preset latch schematic transistor sizing

Transistor width (μm)		
M1,M2,M3	M4,M5,M6,M7	M8,M9,M10
4	2	1

Figure 71 displays a transient simulation of the circuit of Figure 70, where the input signal and clock frequency are 1 GHz and 250 MHz respectively. In Figure 71, it possible to notice that latch output voltage dynamic is between 200 mV and 1V (supply voltage). This dynamic of the latch output voltage leads to higher power consumption, given that when the synthesizer is not generating an IR-UWB pulse, all CML flip-flops output signals will be in low logic level, which means they present a voltage level of 200 mV. A logic circuit with asymmetric supply consumes more power when its input signal is closer to half value of the voltage supply. For example, a classic CMOS inverter presents a higher power drain when its inputs value is half value of the supply voltage.

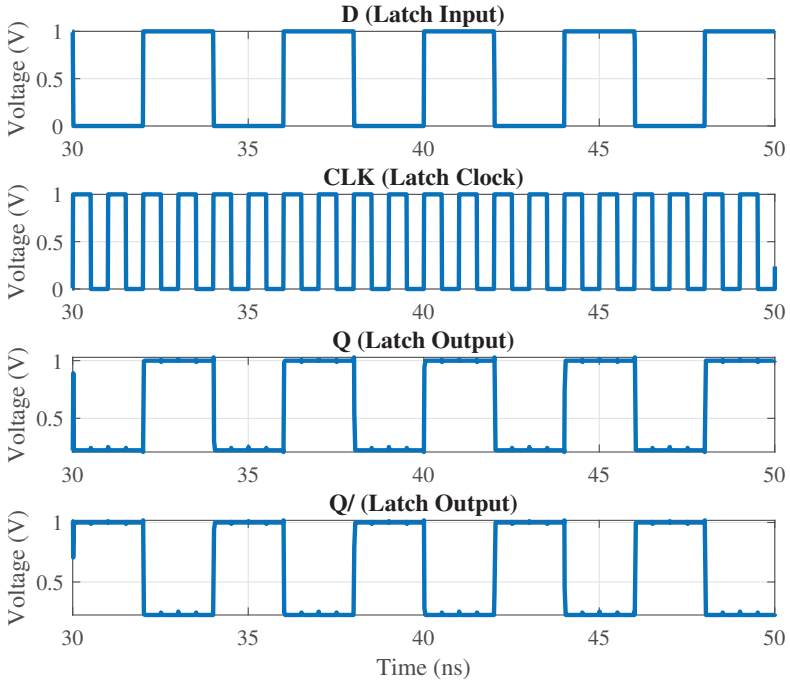


FIGURE 71 – Transient simulation of CML high asynchronous preset latch

A feasible solution to solve this issue is proposed in circuits of Figures 72 and 73. The circuit of Figure 73 is a version of the latch of Figure 70 modified, where the architecture was flipped and n-channel transistors were swapped by p-channel, and p-channel transistors were swapped by n-channel. In this dissertation, the latch of figure 70 will be named CML-N and the latch of Figure 73 CML-P. For the power management of the flip-flop of Figure 72 is done with the PDB node (Power up) instead of PD (Power down). Table 16 address the transistor sizing of circuit of Figure 73.

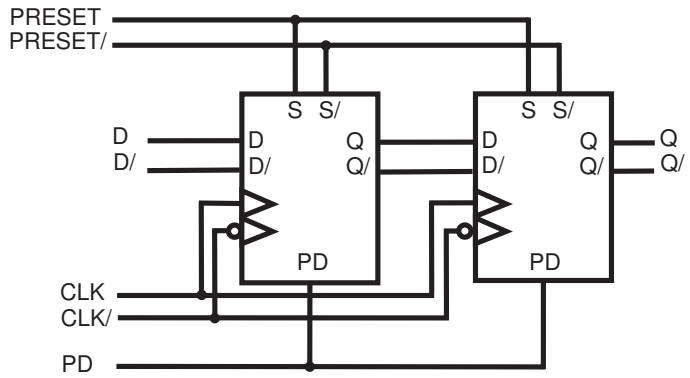


FIGURE 72 – Modified CML (CML-P) high asynchronous preset flip-flop schematic

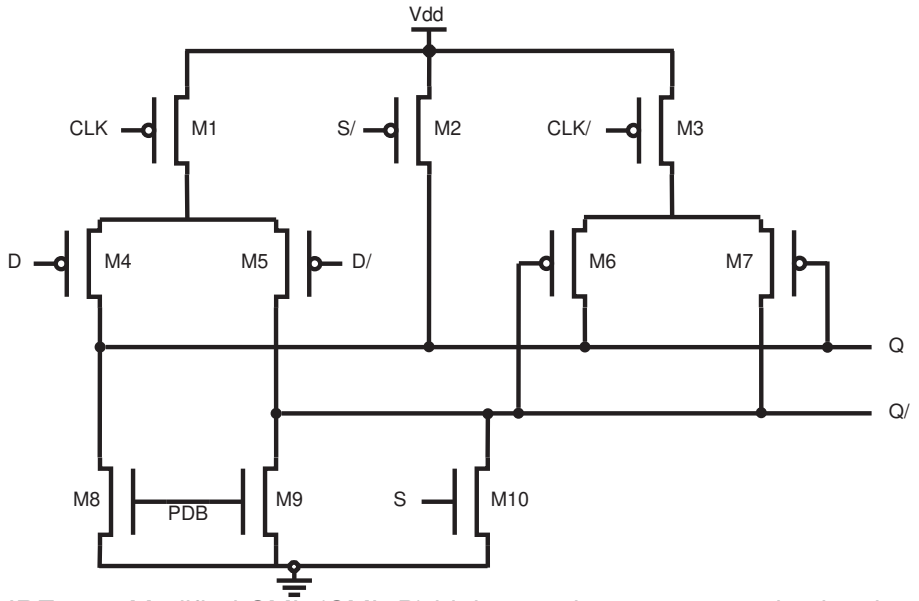


FIGURE 73 – Modified CML (CML-P) high asynchronous preset latch schematic

TABLE 16 – Modified CML (CML-P) high asynchronous preset latch schematic transistor sizing

Transistor width (μm)				
M1,M3	M2	M4,M5,M6,M7	M8,M9	M10
32	6	32	1	3

Figure 74 shows a transient simulation of the circuit of Figure 73, where the input signal and clock frequency are 1 GHz and 250 MHz respectively. In figure 74, it may be noticed that the modified (CML-P) latch presents an output voltage dynamic between 0 and 940 mV, that is different from the latch of Figure 71. When the pulse synthesizer is not transmitting IR-UWB pulses, all CML-P flip output signals will be in low logic level, which means they present a voltage level of 0 V, such that the CML-P latch does not present the issue of higher power consumption coming from a higher displayed voltage level at flip-flop output. Nevertheless, from tables 15 and 16, CML-P latch architecture has bigger transistors than CML-N latch architecture. Indeed, it was necessary to rise the width of transistors of CML-P latch to ensure that it works properly with a frequency until 4.5 GHz, however this may lead to a higher power leakage.

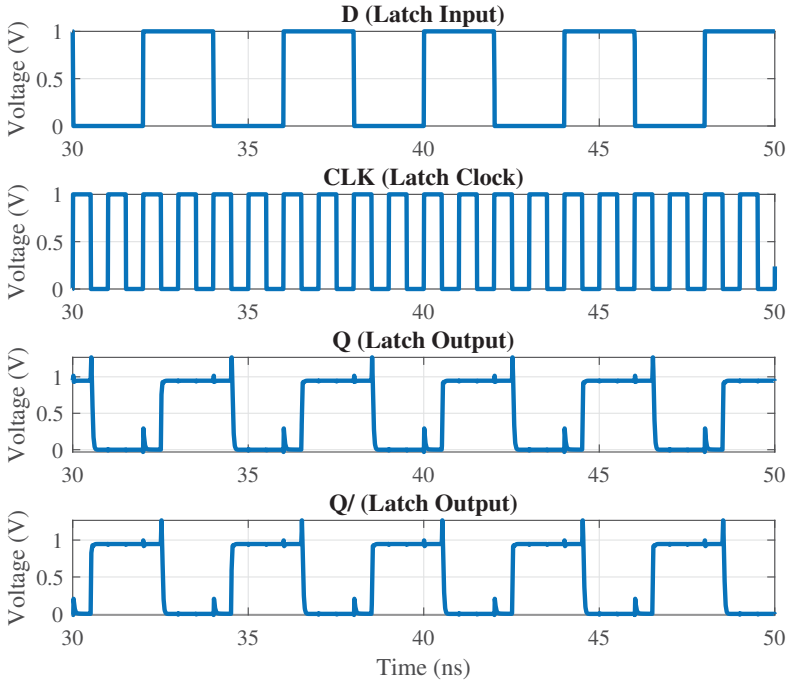


FIGURE 74 – Transient simulation of CML-P high asynchronous preset latch

In relation of the all addressed fast memory architectures in this chapter, Figures 75 and 76 presents the fast memory block mean power consumption in relation of fast memory the clock frequency, for a PRF of 10 MHz, and in relation of PRF, for a clock frequency of 1 GHz respectively. In the simulations of Figure 75 and 76, only the envelope shaping circuit was simulated, and this generates at its output an 8-bit data bus to address the IEEE 802.15.4 channel 3.

From Figure 75, it can be noticed that fast memories based on CMOS flip-flops presents lower power consumption than ones based on CML flip-flops in terms of the simulated clock frequency. The flip-flop architecture of Figure 63b presented the lowest power consumption for a frequencies higher than 1.7 GHz. Meanwhile, the flip-flop architecture of Figure 72 presented the highest power consumption for all simulated range of clock frequency. The power consumption of the flip-flop of Figure 64 presents a slight variation in terms of simulated clock frequency, that can be explained by the fact the flip-flop composed by NAND gates and logic inverters power consumption depends more on the number of logic transitions rather than the circuit speed. Indeed, the number of logic transitions are the same for all clock frequencies simulated.

From Figure 76, it can be seen that, in terms of PRF, fast memories based on CMOS flip-flops presents lower power consumption than ones based on CML flip-flops. The flip-flop architecture of Figure 63b presented the lowest power consumption for all range of simulated PRF, while the flip-flop architecture of Figure 72 presented the highest power consumption for all simulated range of PRF. Among the CMOS flip-flops

architectures, the one of Figure 64 consumes more power.

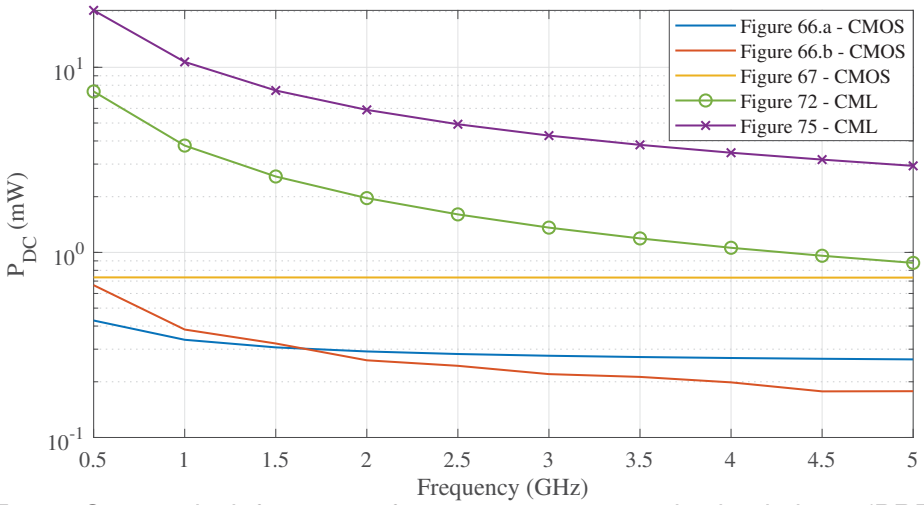


FIGURE 75 – Sweep clock frequency fast memory parametric simulations. (PRF = 10 MHz, IEEE 802.15.4 standard channel 3 addressed)

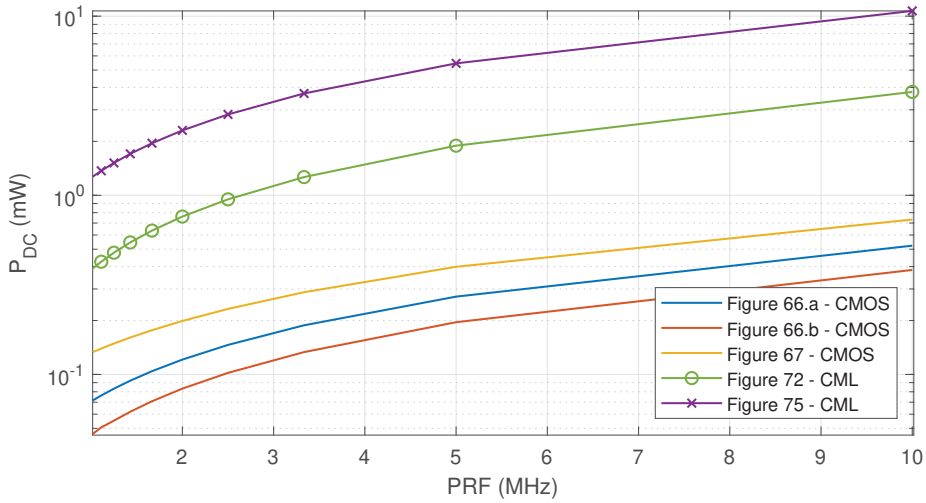


FIGURE 76 – Sweep pulse repletion frequency fast memory parametric simulations. (Frequency clock of 1 GHz, IEEE 802.15.4 standard channel 3 addressed)

Finally, Table 17 addresses the approached fast memory architectures power leakage, mainly flip-flop and shift register power leakage. From Table 17, it can be observed that the flip-flop from Figure 63b presents the lowest power leakage. The CML flip-flops of Figure 69 and 72 present a higher power leakage than CMOS flip-flops of 63a and 64, where the latter has the highest power leakage. The flip-flop of Figure 63b presents the lowest power leakage and the lowest power consumption in terms of PRF since then it has smaller transistors than other addressed flip-flops. Therefore, in the IR-UWB pulse synthesizer design, the envelope shaping circuit will be based on fast memory composed by the flip-flops of Figure 63b.

TABLE 17 – Addressed fast memory architectures static power

Architecture	Power Leakage	
	Flip-flop (nW)	Shift Register (nW)
Figure 63a - CMOS	235.39	2446
Figure 63b - CMOS	39.12	931.74
Figure 64 - CMOS	942	8175
Figure 69 - CML	108.82	1489
Figure 72 - CML	95.79	1867

4.5.2 Buffer Stage

Placed between the fast memory and the digitally controlled amplifier (DCA), the buffer stage of envelope shaping circuit has the target of improve the fast memory output signals integrity and to drive them to the DCA. The envelope shaping circuit buffer stage design is composed by 8 CMOS parallel buffers (Fig. 77). The buffer schematic is displayed in Figure 62. Table 18 addresses the 8 CMOS buffers transistor sizing, where the buffer B7 is composed by bigger transistor because its output is connected to bigger current source transistor of DCA. Again, the transistor sizing has been done targeting to achieve equilibrated transistors.

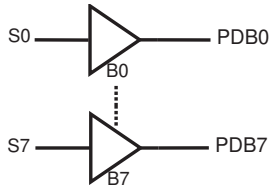


FIGURE 77 – CMOS Buffer stage proposed design

TABLE 18 – Buffer stage transistor sizing

	Transistor width (μm)			
Buffer	M1	M2	M3	M4
B0 to B5	4	2	8	4
B6	4	2	12	6
B7	6	3	24	12

4.6 DUAL-BAND DIGITALLY CONTROLLED OSCILLATOR

The dual-band digitally controlled oscillator (DB-DCO) is the circuit block of the IR-UWB pulse synthesizer responsible to generate the clock signal for the envelope shaping circuit. The DB-DCO generates oscillations with a frequency between 1-2 GHz and 3-4.5 GHz. These frequency bands cover the width of the singles pulses that addresses the IEEE standardized channels, especially IEEE 802.15.4 and IEEE 802.15.6. The DB-DCO design, as well as for carrier generation VCO, resides in a ring oscillator architecture, that is consisted of 3 cascaded delay cells connected in a close loop chain. The DB-DCO and VCO present a few differences: the DB-DCO is done in CMOS logic, does not have a BPSK modulation, and has a voltage control discrete tuning through a 9-bit data bus, where 8-bits control an oscillation frequency for a chosen frequency band and one bit selects the frequency band, that is either 1-2 GHz or 3-4.5 GHz. Concerning the DB-DCO design process, it is divided in 3 steps: single

band voltage-controlled oscillator, single band digitally controlled oscillator, and finally dual-band digitally controlled oscillator (Fig. 78).

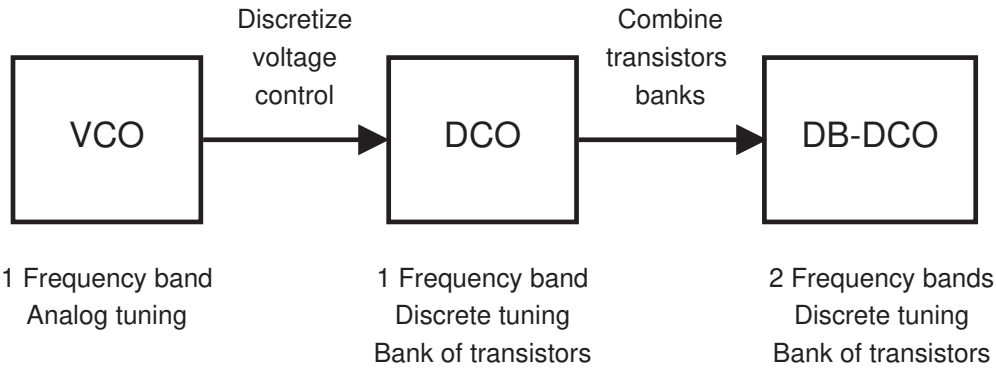


FIGURE 78 – DB-DCO design process overview

Concerning the DB-DCO design first step, Figure 79 displays the single band VCO. The circuit of Figure 79 is composed by a ring oscillator of 3 delay cells (2 input NAND gate and 2 inverters), and 3 buffer cells (CMOS buffer). The 2 input NAND gate schematic is displayed in Figure 59a, the inverter schematic in Figure 59b, and buffer cell schematic in Figure 62. Table 19 address the transistor sizing of 2 input NAND gate, inverter, and buffer from Figure 79.

To tune the VCO oscillation frequency, the current starving technique is applied. Indeed, the n-channel and p-channel transistors outside the ring oscillator loop chain (M1 to M4) control the delay cell propagation time via control of the current that flows through ground and supply nodes of ring oscillator delay cells. The control of this current is done through the gate voltage control of transistors M1 to M4. In the design of the oscillator of Figure 79, the transistors M1 and M3 are designed to offer the minimal frequency oscillation desired, that are either 1 GHz or 3 GHz, where their gate voltage level is keep fixed. The transistors M2 and M4, whose gate voltage is analog tuned (Vctrl and Vctrl/), are designed to tune the oscillation frequency targeting the frequency band of interest (1-2 GHz or 3-4.5 GHz).

In other words, the transistors M1 and M3 establish the least oscillation frequency and transistors M2 and M4 the greatest oscillation frequency. The node ON allows to turn on-off the oscillator of Figure 79, similarly to the VCO of Figure 51. Table 20 address the transistor sizing of the remaining 4 transistors of the circuit of Figure 79. Only one output (OUT1) is connected to other part of synthesizer. Despite two buffer outputs are not connected to other block of the proposed synthesizer, three buffers were implemented in order to isolate all delay cell outputs.

TABLE 19 – Single band VCO CMOS logic cells transistor sizing

	Transistor width (μm)			
Buffer	M1	M2	M3	M4
	4	2	8	4
NAND gate	M1	M2	M3	M4
	9	9	6	6
Inverter	M1		M2	
	9		3	

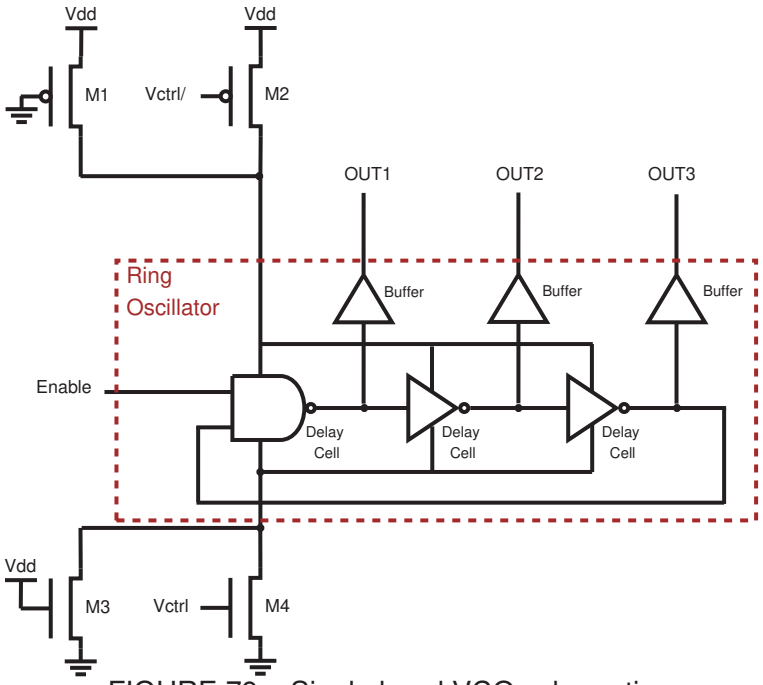


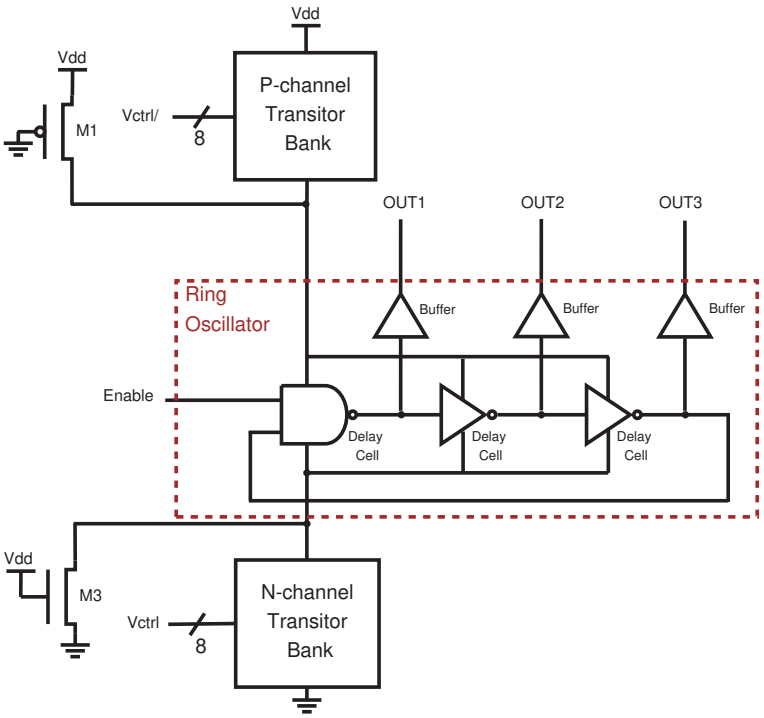
FIGURE 79 – Single band VCO schematic

TABLE 20 – Single band VCO CMOS transistor sizing

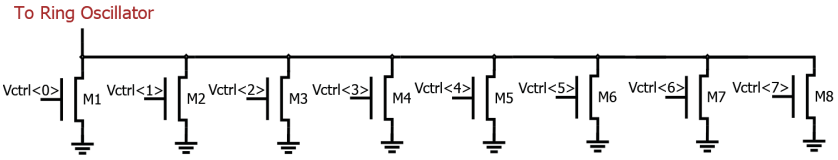
	Transistor	M1	M2	M3	M4
1-2 GHz Band	Width (μm)	0.570	61.2	0.190	20.4
	Length (nm)	30	7320	30	7320
	Transistor	M1	M2	M3	M4
3-4.5 GHz Band	Width (μm)	2.52	61.2	0.840	20.4
	Length (nm)	30	1950	30	1950

Concerning the DB-DCO design second step, Figure 80a display the single band digitally controlled oscillator schematic design, where the oscillation frequency is controlled through digital tuning instead of analog tuning. To achieve the circuit of Figure 80 from the one of Figure 79, the transistor M2 and M4 are partitioned into N parallel transistors that composes a transistor bank (Figs. 80b and 80c), where N is the number of bits of the DCO. Note that the length of transistors remains the same. The transistor bank does the frequency digital tuning of the DCO. The N parallel transistors width follows a geometric progression of ratio of 2, like that was done in DCA design. Tables

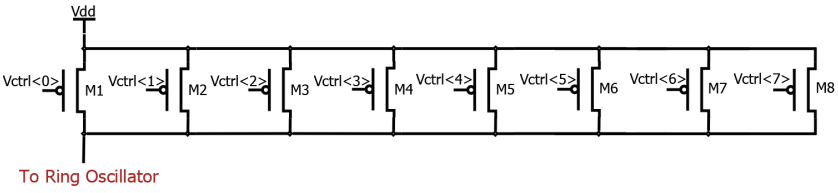
21 and 22 address the n-channel and p-channel transistor banks of DCO. Targeting a frequency resolution of 5 MHz, it has been chosen a N of 8, therefore the circuit of Figure 80 is the 8-bit DCO.



(a) DCO general schematic



(b) N-channel transistor bank schematic



(c) P-channel transistor bank schematic

FIGURE 80 – DCO schematics

TABLE 21 – DCO n-channel transistor banks transistor sizing

1-2 GHz Band	Transistor	M1	M2	M3	M4	M5	M6	M7	M8
	Width (μm)	0.080	0.160	0.320	0.640	1.28	2.56	5.12	10.24
	Length (nm)				7320				
3-4.5 GHz Band	Transistor	M1	M2	M3	M4	M5	M6	M7	M8
	Width (μm)	0.080	0.160	0.320	0.640	1.28	2.56	5.12	10.24
	Length (nm)				1950				

TABLE 22 – DCO p-channel transistor banks transistor sizing

1-2 GHz Band	Transistor	M1	M2	M3	M4	M5	M6	M7	M8
	Width (μm)	0.240	0.480	0.960	1.92	3.84	7.68	15.36	30.72
	Length (nm)	7320							
3-4.5 GHz Band	Transistor	M1	M2	M3	M4	M5	M6	M7	M8
	Width (μm)	0.240	0.480	0.960	1.92	3.84	7.68	15.36	30.72
	Length (nm)	1950							

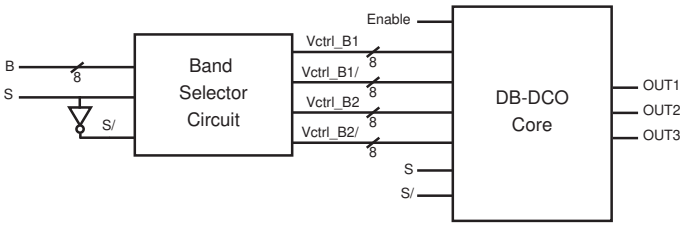
Concerning the DB-DCO last step, Figure 81a displays the dual-band digitally controlled oscillator final schematic design. In this last step, both DCO targeting 1-2 GHz and 3-4.5 GHz frequency band are combined in one controlled oscillator, where the frequency band is selected via a digital signal (S). Figure 81b displays the DB-DCO core design and Figure 81c the frequency band selector circuit design, where this circuit generates signal that address the n-channel and p-channel transistors banks. The frequency tuning of DB-DCO is done with 9 bits, where one bit, the most significant, selects either 1-2 GHz or 3-4.5 GHz frequency band. The 2 input NAND and inverter schematics are displayed in Figure 59. Table 23 addresses the 2 input NAND and inverter transistor sizing.

TABLE 23 – Frequency band selector transistor sizing

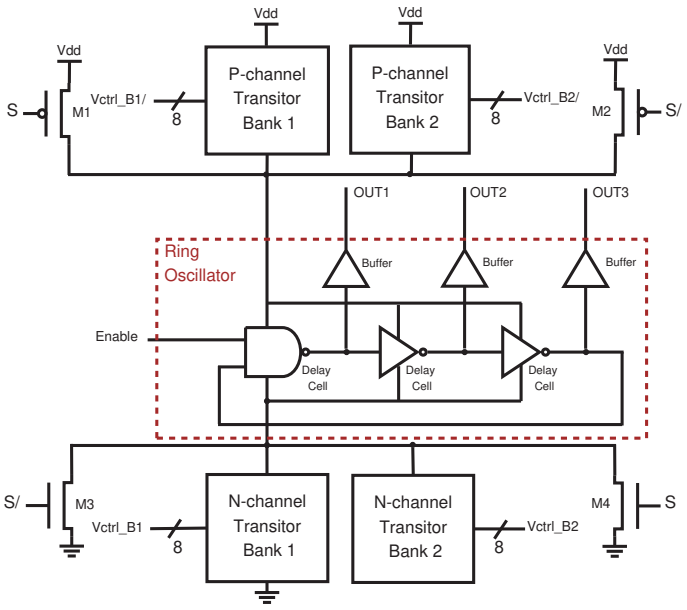
	Transistor width (μm)			
2-input NAND	M1	M2	M3	M4
A1.1 to A1.6	0.3	0.3	0.2	0.2
A1.7	0.45	0.45	0.3	0.3
A1.8	0.9	0.9	0.6	0.6
A2.1 to A2.8	0.3	0.3	0.2	0.2
Inverter	M1		M2	
B1.1 to B1.6	0.3		0.1	
B1.7	0.45		0.15	
B1.8	0.9		0.3	
B2.1 to B2.8	0.3		0.1	

4.7 SLOW MEMORY

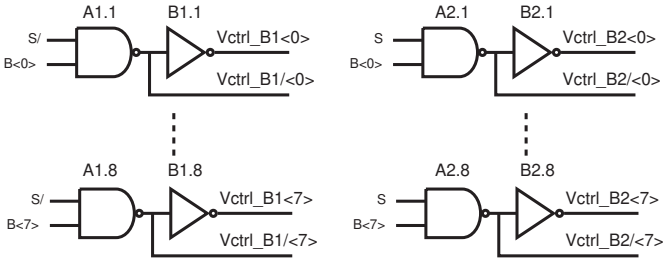
The slow memory is the last synthesizer circuit block approached in this dissertation. The slow memory target is to generate and to provide the 8 bytes that will address the envelope shaping circuit and the 9 bits that will address the DB-DCO. This memory loads a 10-byte data bus from external interface and works with a frequency around few MHz. It should be loaded before the first pulse transmission. The slow memory design is based in 10-byte shift register (Fig. 82) with serial input and parallel output (serial-in, parallel-out) (Fig. 83), composed of 10 1-byte cascaded shift registers. Moreover, the NAND gate followed by an inverter of Figure 82 performs the slow memory



(a) DB-DCO general architecture



(b) DB-DCO core schematic



(c) Frequency band selector schematic

FIGURE 81 – DB-DCO design schematics

shift register enable control, and the two transmission gates are implemented to mitigate the interference from external interfaces. The 2-input NAND gate and inverter design are displayed in Figure 59. The transmission gate design is displayed in Figure 84. Table 24 addresses the NAND gate, inverter, and transmission gate transistor sizing.

Given that the circuit of Figure 82 works in frequency of MHz, all transistors of this circuit have a length (L) of 100 nm targeting a lower leakage power.

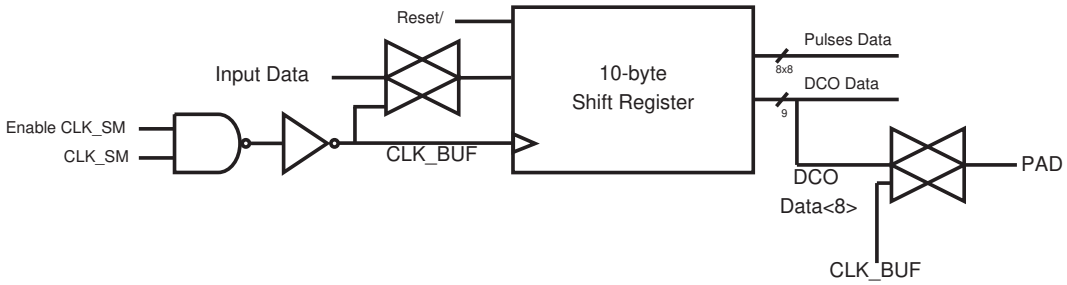


FIGURE 82 – Slow Memory Design

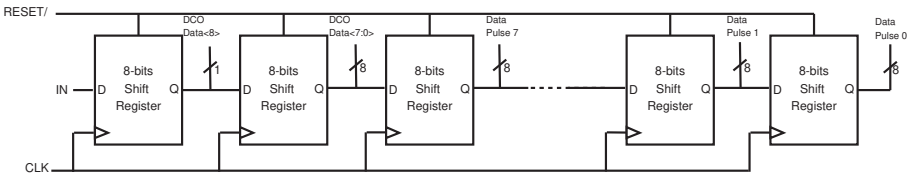


FIGURE 83 – 10-byte serial-in, parallel-out shift register Design

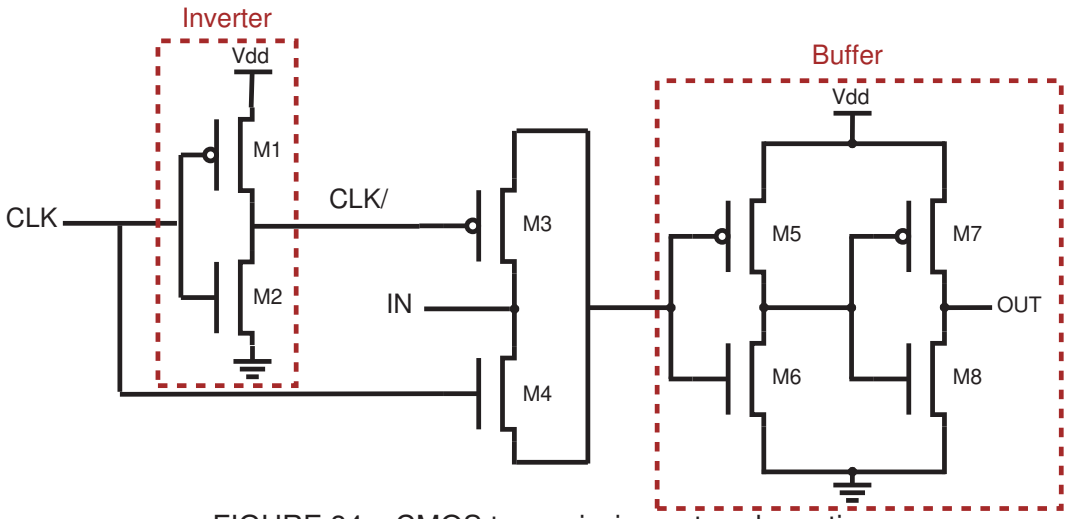


FIGURE 84 – CMOS transmission gate schematic

TABLE 24 – Slow Memory Transistor sizing

	Transistor (μm)							
Transmission Gate	M1	M2	M3	M4	M5	M6	M7	M8
	412	206	412	206	412	206	824	412
2-input NAND	M1	M2	M3	M4				
	412	412	412	412				
Inverter	M1	M2						
	412	206						

Concerning the circuit of Figure 83, the signal reset is implemented to clear the memory. Figure 85 displays the 1-byte shift register design. This shift register is composed of 8 flip-flops whose design is displayed in Figure 86. The CMOS flip-flop architectures discussed in fast memory section (Figs. 63 and 64) can be applied to slow

memory design. The architecture of Figure 63 is not interesting since then it presents node voltage fluctuations, such that it may change undesirably the information that should be sent to DB-DCO and envelope shaping circuit, interfering with IR-UWB pulse shape. In the latch of fast memory, the solution to prevent node voltage fluctuations is to reset the fast memory when no pulse is emitted. However, this solution is not feasible to slow memory because this is loaded slowly (around few microseconds) one time, before the pulse's transmission, unlike the fast memory that is loaded before each transmitted pulse. Meanwhile, the flip-flop architecture of Figure 64 is interesting given that it does not present node voltage fluctuation issues. However, for the slow memory it is implemented a flip-flop activated by positive rising clock edge and has active low asynchronous reset (Fig.86). The flip-flop of Figure 86 is implemented with 2 latches master and slave, that are composed by NAND gates of 2 and 3 inputs. Figure 87 displays the latch schematic. Note that the place where 3-bit NAND of latch of Figure 87 is different from the latch of Figure 65 because this latch is asynchronous preset and that one is asynchronous reset. The 2-bit NAND gate, 3-bit NAND gate and inverter design is displayed in Figs 59a, 66 and 59b respectively. Table 25 addresses the transistor sizing of the circuit from Figure 87. Note that to equilibrate the transistors of the logic circuits from Figure 87, it was applied a parameter β of 2.

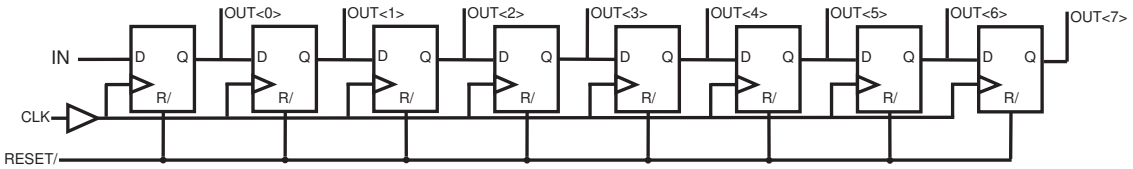


FIGURE 85 – 1-byte serial-in and parallel-out shift register Design

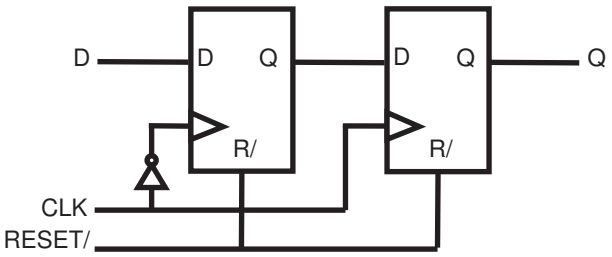


FIGURE 86 – CMOS low asynchronous reset flip-flop schematic

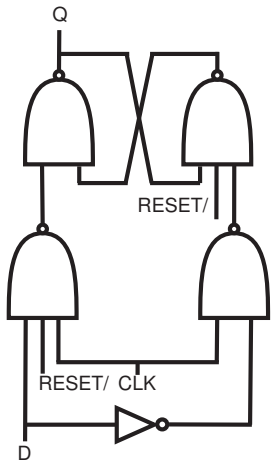


FIGURE 87 – CMOS low asynchronous reset latch schematic

TABLE 25 – CMOS low asynchronous reset latch transistor sizing

	Transistor (μm)					
3-input NAND	M1 206	M2 206	M3 206	M4 309	M5 309	M6 309
2-input NAND	M1 206	M2 206	M3 206	M4 206		
Inverter	M1 412	M2 206				

5 CIRCUIT LEVEL SIMULATIONS

This chapter addresses IR-UWB pulse synthesizer final design simulations. Concerning the envelope shaping circuit, the flip flop chosen architecture is the one of Figure 63b. First, parametric simulations of each pulse generator blocks are addressed. In relation of the VCO and DB-DCO, the voltage control is swept. In relation of DCA, the VCO voltage control and 8-bit data bus generated by envelope shaping circuit are swept. In relation of slow memory, the clock frequency is swept. Finally, IR-UWB pulse generation study cases are addressed, where time domain waveform and frequency domain simulation results are presented for several IEEE standardized channels, in particular the IEEE 802.15.4. Concerning the parasitic capacitances, only the parametric simulations presents circuit results both with and without parasitic capacitances. The IR-UWB pulse transmission study cases present only results with parasitic capacitances. Nevertheless, they are not post layout simulation.

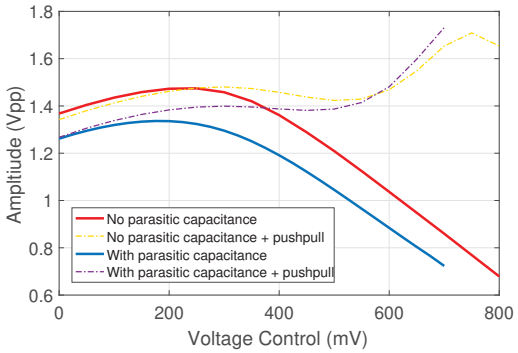
5.1 PARAMETRIC SIMULATIONS

In this sub-chapter, parametric simulations are presented. Firstly, gated VCO parametric simulations are addressed, sweeping the VCO voltage control. Secondly, 8-bit DCA parametric simulations are addressed, sweeping the VCO frequency and 8-bit data bus from envelope shaping circuit. Thirdly, DB-DCO parametric simulations are addressed, sweeping the discrete voltage control. Finally, slow memory parametric simulations are addressed, sweeping the clock frequency.

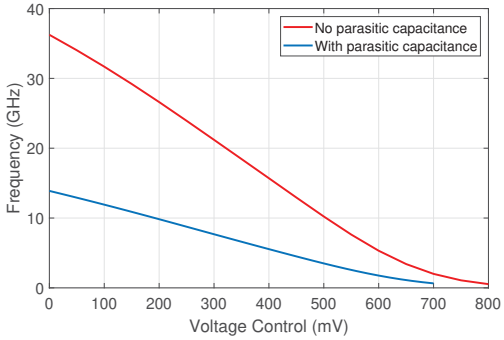
5.1.1 Gated Voltage Controlled Oscillator

In relation of the gated voltage-controlled oscillator parametric simulations, Figure 88a presents the gated VCO output amplitude level, Figure 88b the gated VCO frequency and Figure 88c DC power in function of the VCO voltage control (Vctrlb). From Figure 88a, it can be noticed that the push-pull was able to improve the VCO output signal, mostly for voltage control greater than 300 mV, and the parasitic capacitor reduced the VCO output amplitude levels. The push-pull is important and necessary in the pulse generation design because that allows that VCO output signal drives properly the carrier generation buffering stage chain and the DCA. From Figure 88b, it can be observed that the parasitic capacitances lower significantly the VCO oscillation frequency, where the maximum frequency is 36 GHz without parasitic capacitance, and 14 GHz with parasitic capacitance. From Figure 88c, it can be noticed that the parasitic capacitances lightly increase the DC power, where the maximum power is around 20

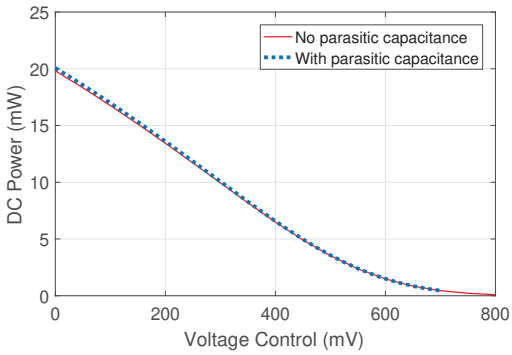
mW. Moreover, the VCO frequency and DC power present linear behavior in relation of the input voltage control, for values up to 500 mV.



(a) (VCO output amplitude



(b) VCO frequency

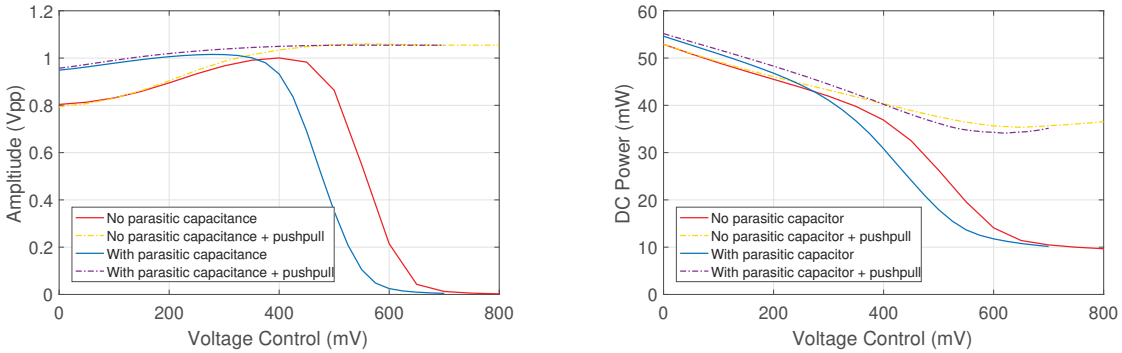


(c) VCO DC power

FIGURE 88 – Sweep voltage control VCO parametric simulations

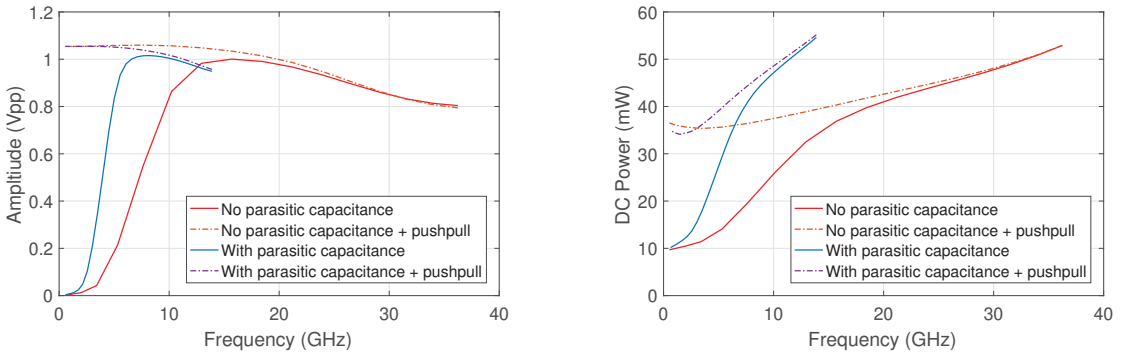
5.1.2 Digitally Controlled Amplifier

In relation of digitally controlled amplifier of 8 bits, Figure 89a presents the IR-UWB pulse output amplitude level, Figure 89b the carrier generation block and DCA DC power in function of the gated VCO voltage control. Figure 90a presents the IR-UWB pulse output amplitude level, and Figure 90b the carrier generation block and DCA DC power in function of the gated VCO frequency. It is important to note that for the DC power measured from simulations, it is only included the carrier generation block and DCA from Figure 49. From Figure 89, it can be seen that without the push-pull circuit, the DCA output amplitude are weak for VCO voltage control greater than 500 mV or for low carrier frequencies, that can be explained by the fact that gated VCO is unable to drive the carrier generation buffer chain and DCA because the gated VCO presents weak output voltage levels. Figure 90b points that the parasitic capacitance insertion arises the DC power for low gated VCO frequencies.



(a) DCA output amplitude levels (b) Carrier generation and DCA DC power

FIGURE 89 – DCA parametric simulation sweeping the gated VCO voltage control

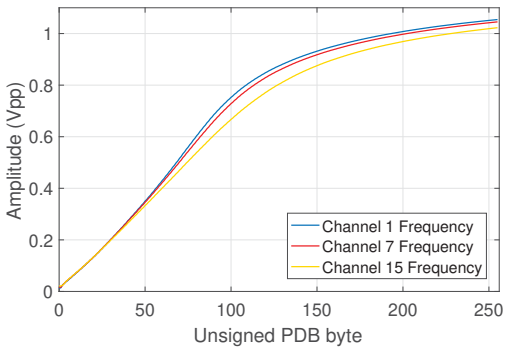


(a) Pulse synthesizer amplitude (b) Pulse synthesize DC power

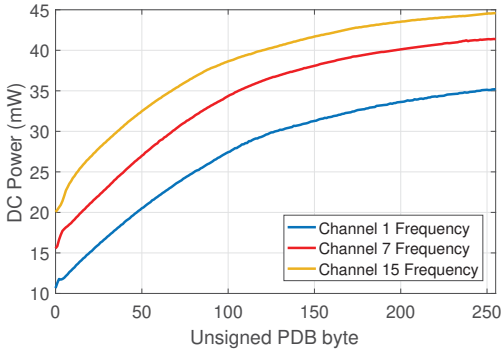
FIGURE 90 – Pulse synthesizer parametric simulation sweeping the VCO frequency

Figure 91a addresses the IR-UWB pulse output amplitude level, Figure 91b the DC power and Figure 91c the DCA power efficiency in function of the 8-bit data bus unsigned value generated by the envelope shaping circuit (PDB-DCA). In particular, this simulation includes only the carrier generation block and DCA. The 8-bit data bus was set in the simulation. Three VCO frequencies values are addressed, where they are specified in terms of the standardized channel of Table 1 (IEEE 802.15.4). The parametric simulation of Figure 91 considers the circuit with parasitic capacitance and push-pull.

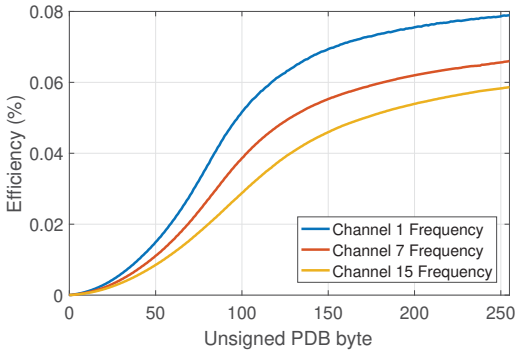
From Figure 91, it can be observed that higher carrier frequency implies in higher IR-UWB pulse amplitude level and DC power consumption, and that greater values of the 8-bit data bus (PDB-DCA) rises the IR-UWB pulse amplitude level and DC power consumption, presenting curves with a non-linear behavior, which is not an issue because the IR-UWB pulse synthesizer (Fig. 49) has programming capabilities. The IEEE 802.15.4 standardized channel 15 presents the lowest IR-UWB pulse amplitude level because the parasitic capacitances have major effects for higher frequency operations. Besides, for this channel frequency, the DC power consumption is higher given the higher VCO operation speed.



(a) Pulse synthesizer amplitude



(b) Pulse synthesizer DC power

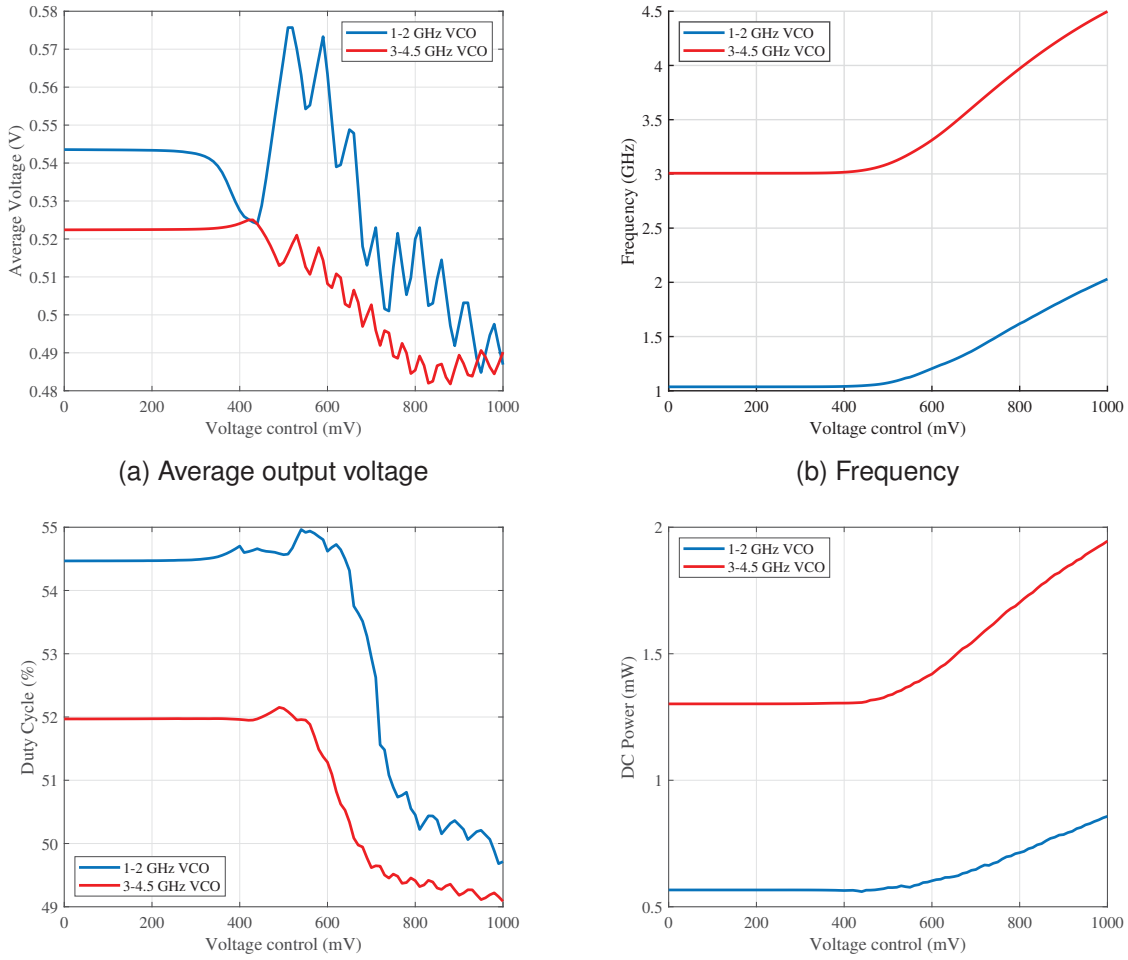


(c) Pulse synthesizer efficiency

FIGURE 91 – Pulse synthesizer parametric simulation sweeping the PDB 8-bit bus data unsigned value

5.1.3 Dual-band Digitally Controlled Oscillator

In relation of the dual-band digitally controlled oscillator parametric simulations, Figure 92a presents the single band voltage-controlled oscillator, from Figure 79, average output voltage level, figure 92b the VCO frequency, Figure 92c duty cycle and Figure 92d DC power in function of the VCO voltage control. The parametric simulation of Figure 92 considers the circuit with parasitic capacitance. From Figure 92, it can be noticed that below 300 mV, both designed VCO for 1-2 GHz and 3-4.5 GHz present the minimal frequency oscillation where the values of average output voltage, mean power and duty cycle are constant. From Figure 92, it can be observed that, for voltage control greater than 500 mV, the VCO frequency and mean power rise, while the average output voltage and duty cycle decrease for both VCOs. The 1-2 GHz presents a higher power consumption, and a lower average output voltage and duty cycle than the 3-4.5 GHz. Moreover, Figures 92b and 92d points for an input voltage superior than 600 mV a linear behavior of the VCO frequency and mean power. Therefore, as well the VCO of the carrier generation block, the VCO from Figure 79 presents a linear behavior in relation of the input voltage control. For a voltage control greater than 500 mV, the 1-2 GHz and 3-4.5 GHz VCO mean gain are 1.91 GHz/V and 2.81 GHz/V respectively.



(a) Average output voltage

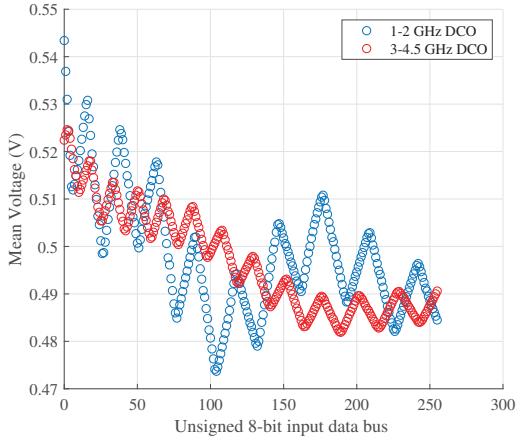
(b) Frequency

(c) Duty cycle

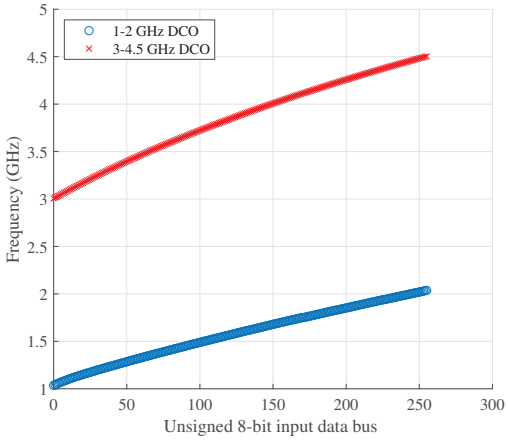
(d) DC Power

FIGURE 92 – VCO parametric simulation sweeping the voltage control

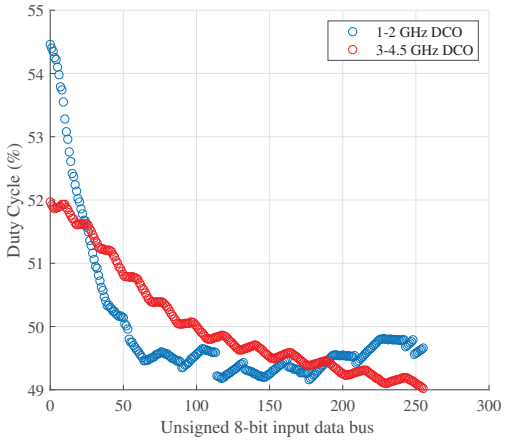
Figure 93a presents the single band digitally controlled oscillator, from Figure 80, average output voltage level, figure 93b the VCO frequency, Figure 93c duty cycle and Figure 93d DC power in function of the DCO 8-bit input data. From Figure 93, it can be observed a predominant linear behavior for DCO frequency and mean power, where higher values of 8-bit input data implies in a higher frequency and mean power, and lower duty cycle. The curves of Figure 93b and 93d present a stronger linear behavior than the ones of Figures 92b and 92b. However, the DCO does not present a fine tuning like the gated VCO. The 1-2 GHz and 3-4.5 GHz DCO mean resolution are 3.88 MHz/bit and 5.79 MHz/bit respectively.



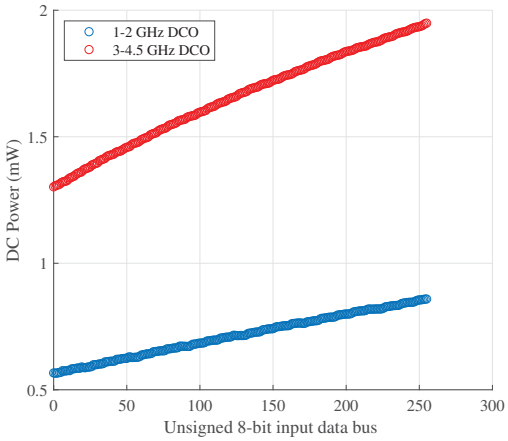
(a) Average output voltage



(b) Frequency



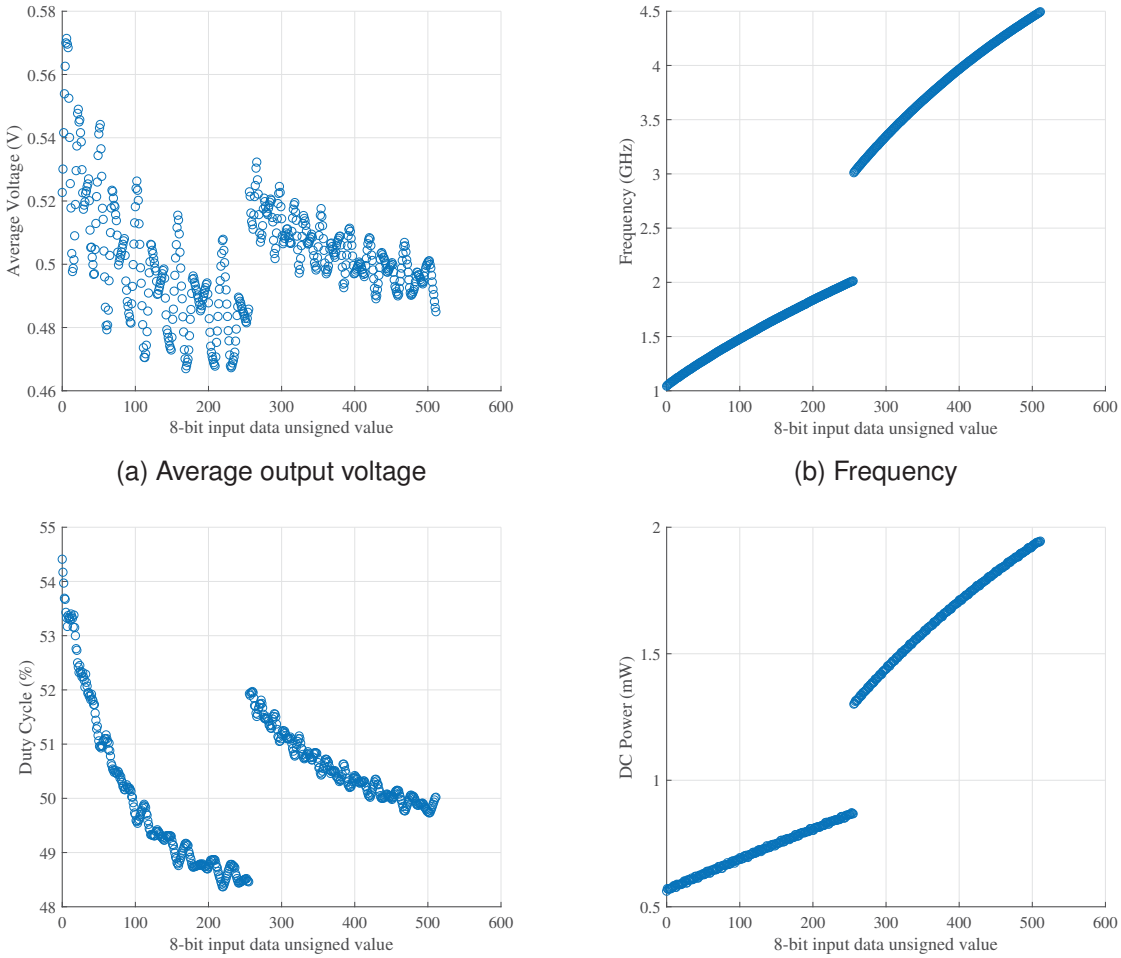
(c) Duty cycle



(d) DC Power

FIGURE 93 – DCO parametric simulation sweeping the voltage control

Figure 94a presents the dual-band digitally controlled oscillator, from Figure 81, average output voltage level, Figure 94b the VCO frequency, Figure 94c duty cycle and Figure 94d DC power in function of the DB-DCO 9-bit input data. From Figure 94a, it can be seen that the curves presented in this figure are the combined version of the curves of both 1-2 GHz and 3-4.5 GHz DCO addressed in Figure 5.6. For an 9-bit input data bus value lower than 255, the DB-DCO behaves as 1-2 GHz DCO, otherwise, the DB-DCO behaves as 3-4.5 GHz.



(a) Average output voltage

(b) Frequency

(c) Duty cycle

(d) DC Power

FIGURE 94 – DB-DCO parametric simulation sweeping the voltage control

5.1.4 Slow Memory

In relation of the slow memory, that generates 10-byte data bus that address that DB-DCO and the envelope shaping circuit, Figure 95 presents the power consumption of the 1-byte serial-in and parallel-out shift register of Figure 85. From Figure 95, it can be observed that the circuit of Figure 85 consumes power of order of microwatts. For a clock frequency of a few MHz, the circuit of Figure 85 consumes a few microwatt (7.60 μW for a clock frequency of 10 MHz).

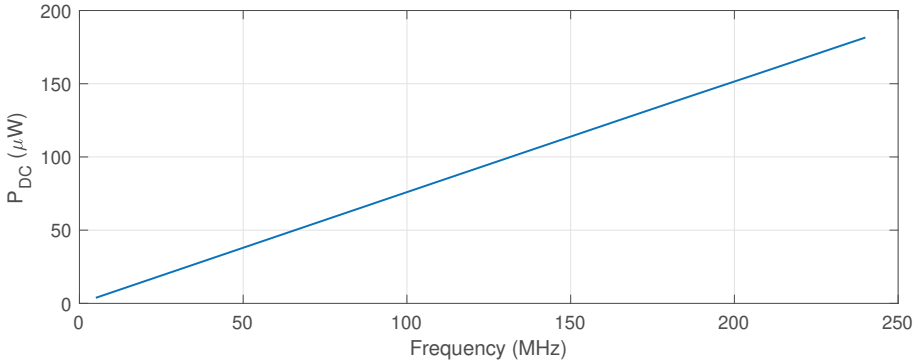


FIGURE 95 – 1-byte serial-in and parallel-out shift register parametric simulation sweeping the clock frequency

5.2 IR-UWB PULSE TRANSMISSION STUDY CASES

In this sub-chapter, transient simulations of the IR-UWB pulse synthesizer of Figure 49 are addressed. The main focus here is to observe the generated IR-UWB pulse waveform and spectrum, principally if the pulse fits in the IEEE 802.15.4 standard and FCC regulations masks. All the generated pulses have an envelope sampled & hold (Fig.23) from a triangular continuous envelope (Fig.22). The targeted envelope presents a symmetric shape and is composed by 6 sampled & hold pulses, where each single pulse has a particular amplitude level, defined by the 8-bit data bus generated by the envelope shaping circuit.

In this case study, three IEEE 802.15.4 standardized channels are targeted: channels 1, 14 and 15. Table 26 addresses generated IR-UWB pulses parameters for every addressed standardized channel. There are two types of generated IR-UWB pulse, the ideal and the non-ideal. In this dissertation, only the non-ideal pulses are addressed. The ideal and non-ideal pulses have different time parameters, mainly the pulse duration, where the non-ideal single pulse duration is the ideal single pulse duration rounded up to nearest VCO half-period value (Fig.96), hence reducing the generated IR-UWB pulse bandwidth (Fig.97). Therefore, the non-ideal single pulse duration is integer number of VCO half-periods, which allow to achieve a better synchronization between the carrier signal and the envelope shaping circuit.

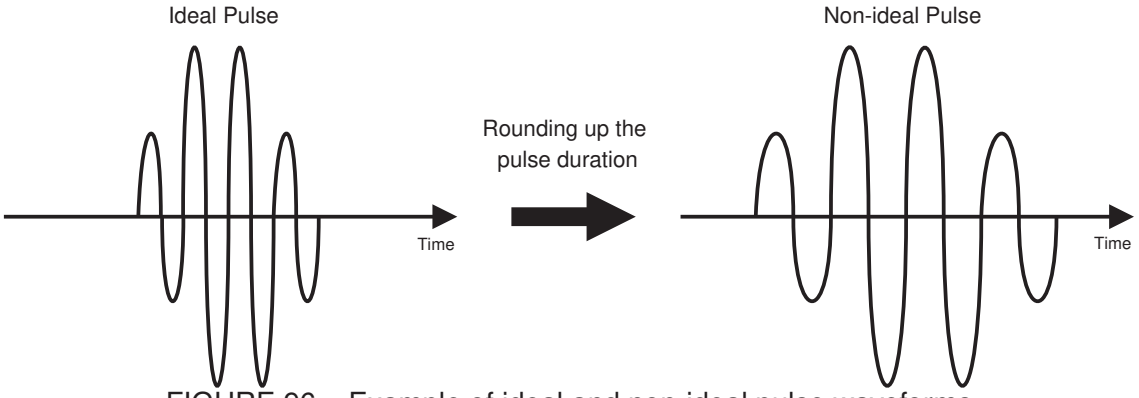


FIGURE 96 – Example of ideal and non-ideal pulse waveforms

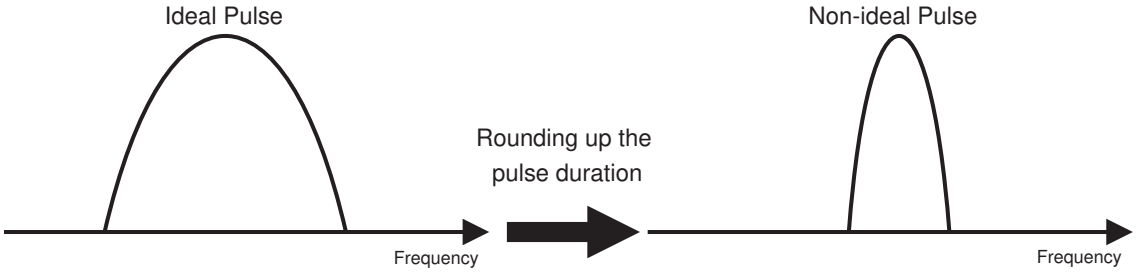


FIGURE 97 – Example of ideal and non-ideal pulse spectrum

TABLE 26 – IR-UWB pulse parameters

Channel	1		14		15	
Type of IR-UWB pulse	Ideal	Non-ideal	Ideal	Non-ideal	Ideal	Non-ideal
VCO voltage control (mV)	492.19		173.02		197.54	
Carrier frequency (MHz)	3494		9984		9484.8	
Maximum allowed bandwidth X = 3 dB (MHz)	499		499		1355	
Maximum allowed bandwidth X = 10 dB (MHz)	650		650		1757	
Maximum allowed bandwidth X = 18 dB (MHz)	800		800		2162	
DB-DCO 9-bit input unsigned value	133	79	133	119	474	390
DB-DCO frequency (GHz)	1.60	1.40	1.60	1.54	4.33	3.91
Sampled pulse duration (ps)	626	716	626	651	231	256
Total pulse duration (ps)	3756	4296	3756	3906	1386	1536

Table 27 addresses the 8-bit data bus unsigned value generated by the envelope shaping circuit that address the 8-bit DCA. Despite the pulse targeting IEEE 802.15.4 standardized channels 1 and 14 have similar timing parameters, the values displayed in Table 27 are different for these channels because the generated IR-UWB pulse amplitude vary as function of the carrier frequency, as showed in Figure 91a.

TABLE 27 – 8-bit bus data unsigned values from the envelope control module

Sampled pulse	Channel 1	Channel 14	Channel 15
0	0	0	0
1	26	25	20
2	81	90	86
3	255	255	255
4	255	255	255
5	81	90	86
6	26	25	20
7	0	0	0

Figures 98, 99 and 100 display IR-UWB pulses time domain waveform and normalized power spectral density (PSD) addressing IEEE 802.15.4 standardized channels 1, 14 and 15 respectively. In the frequency domain figures, the indoor FCC and IEEE 802.15.14 standard masks are also indicated.

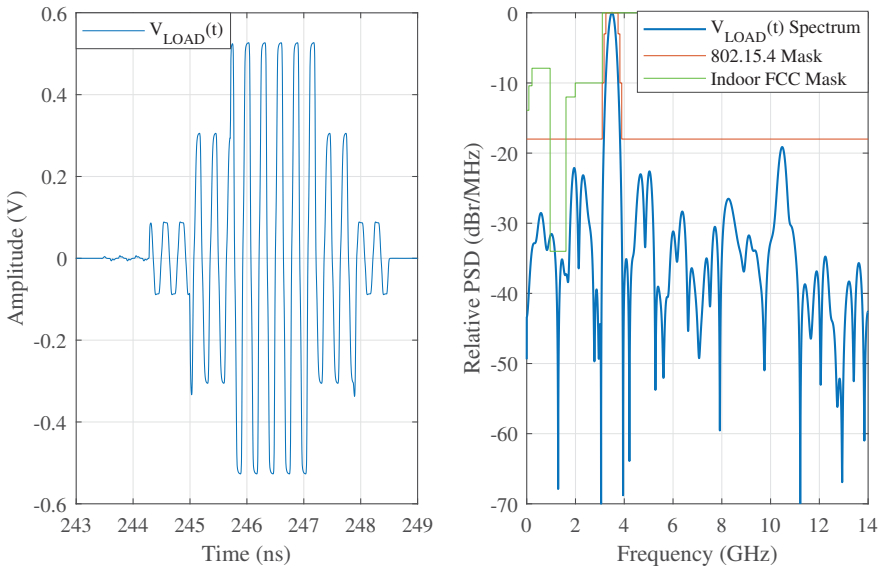


FIGURE 98 – IR-UWB pulse for the channel 1 of the IEEE 802.15.4 Standard

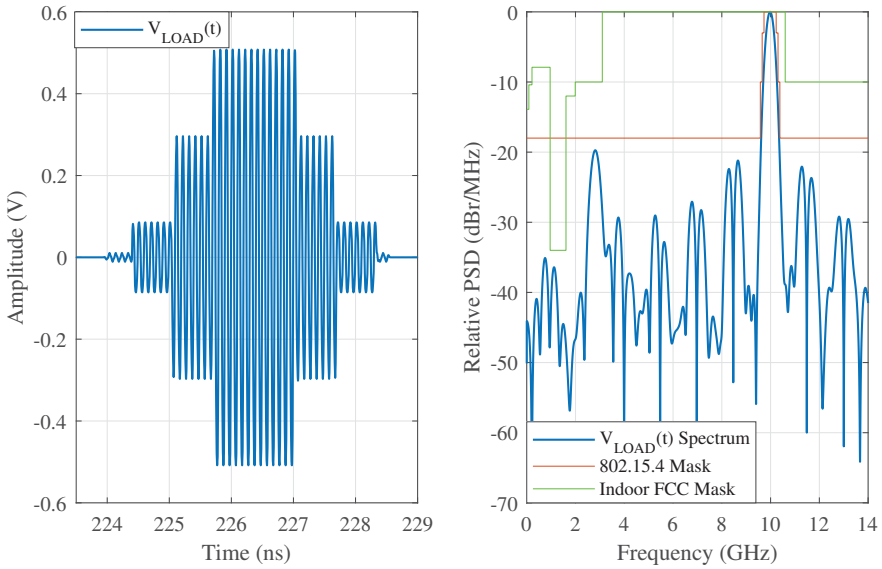


FIGURE 99 – IR-UWB pulse for the channel 14 of the IEEE 802.15.4 Standard

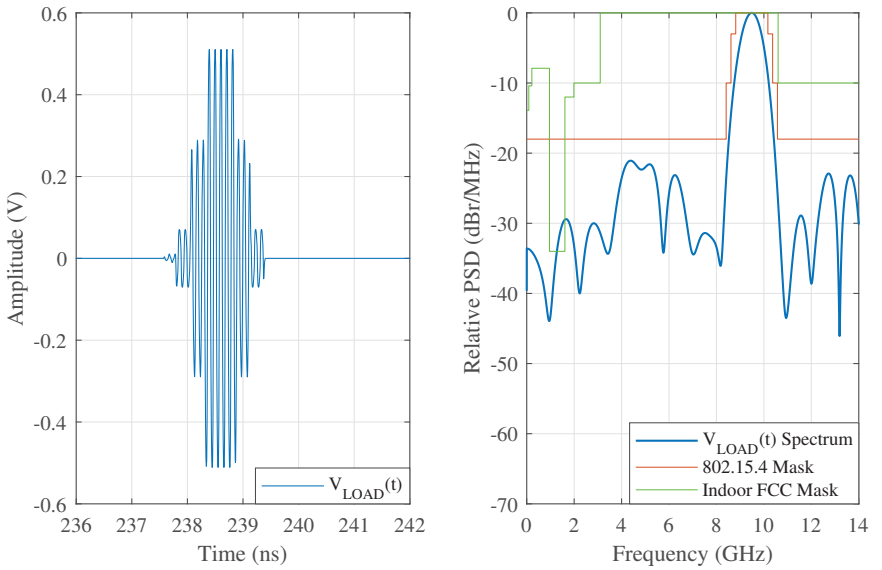


FIGURE 100 – IR-UWB pulse for the channel 15 of the IEEE 802.15.4 Standard

Table 28 shows the single pulses amplitudes levels for the IEEE 802.15.4 addressed channels and Table 29 the generated IR-UWB pulses frequency bandwidth for particular attenuation levels (3 dB, 10 dB and 18 dB). In Figures 98, 99 and 100, it can be noticed that all generated IR-UWB pulses fits in IEEE 802.15.4 standard mask, where Table 29 indicates that IR-UWB pulses bandwidth for an attenuation of 3 dB, 10 dB and 18 dB are lower than the maximum bandwidth allowed by the IEEE 802.15.4 standard (Table 26). Despite IR-UWB pulses of Figure 98 and 100 transgressed the FCC indoor mask, in particular for 0.5-2 GHz frequency band, this does not represent a major issue because the UWB antenna filters the signal within this frequency band. From the generated IR-UWB pulse waveforms, it can be observed that the less distorted

is the one that addresses the IEEE 802.15.4 standardized channel 14, that can be explained by the higher ratio between pulse duration and carrier signal period.

TABLE 28 – Sampled IR-UWB pulse amplitude levels in mV

Sampled pulse	Channel 1	Channel 14	Channel 15
0	0	0	0
1	173.8	165.1	134.0
2	611.2	595.0	579.4
3	1054.2	1017.3	1022.6
4	1054.2	1017.3	1022.6
5	611.2	595.0	579.4
6	173.8	165.1	134.0
7	0	0	0

TABLE 29 – Simulated IR-UWB pulse bandwidths

Channel	sampled pulse duration (ps)	$BW_{X=3dB}$	$BW_{X=10dB}$	$BW_{X=18dB}$
1	716	300	524	676
14	651	330	588	748
15	256	812	1446	1894

Finally, Table 30 addresses the UWB system DC power consumption, for the addressed channels of IEEE 802.15.4 standard, for two different values of pulse repetition frequency (PRF) that are 1 MHz and 10 MHz. The (2.8) assumes a linear behavior between the DC power consumption (P_{dc}) and PRF, where the energy consumpted per pulse (E_{ac}) and power leakage (P_{0Hz}) can be calculated through (2.8) and (2.9). To calculate these two power parameters, the DC power consumption values of simulated IR-UWB pulse with PRF of 1 MHz and 10 MHz were used. Therefore, Table 31 addresses the enegy per pulse for addressed channels of IEEE 802.15.4.

TABLE 30 – IR-UWB pulse synthesizer mean power consumption (μW)

Channel	1		14		15	
PRF (MHz)	1	10	1	10	1	10
VCO	48.42	458.32	162.71	1601.2	62.90	603.12
DCA	67.87	673.83	62.19	616.83	24.24	237.41
Envelope Shaping Circuit	30.88	217.21	30.97	217.58	31.19	220.21
DB-DCO	18.72	179.69	20.27	194.75	33.70	329.97
Carrier generation buffer chain $\&$ slow memory	62.09	530.95	56.69	477.52	30.64	210.97
Total	227.98	2060	332.83	3107.88	182.67	1601.68

TABLE 31 – IR-UWB pulse synthesizer energy per pulse consumption (pJ)

Channel	1	14	15
VCO	45.54	159.83	60.20
DCA	67.33	61.63	23.69
Envelope Shaping Circuit	20.70	20.73	21.00
DB-DCO	17.89	19.39	32.92
Carrier generation buffer chain $\&$ slow memory	52.10	46.76	20.03
Total	203.56	308.34	157.67

From Tables 30 and 31, it is noticed that IR-UWB pulse that targets the IEEE 802.15.4 standardized channel 14 consumes the most energy per pulse, given that this pulse the highest carrier frequency and a longer pulse duration than IR-UWB pulse addressing IEEE 802.15.4 standardized channel 15. This IR-UWB pulse consumes less energy per pulse than the IR-UWB pulse addressing IEEE 802.15.4 standardized channel 1, despite the higher carrier frequency, because it is a shorter pulse. In general, larger pulses with higher carrier frequency consumes more energy per pulse. In particular, from Table 31, the IR-UWB pulse central frequency has major impact on VCO energy per pulse consumption, and the IR-UWB pulse duration on DCA and carrier generation buffer chain energy per pulse consumption. Moreover, shorter IR-UWB pulses rise the DCO power consumption, given that to generate shorter IR-UWB pulses, the DCO frequency must be higher. Meanwhile, the enveloppe pulse shaping circuit energy per pulse consumption is not influenced neither by the IR-UWB pulse duration nor by carrier generation frequency. The reason is that the envelope shaping circuit energy consumption is mainly determined by the number of logical operations done by the fast memory of envelope shaping circuit.

5.3 PERFORMANCE OVERVIEW

Table 32 addresses the IR-UWB pulse synthesizer static power (P_{0Hz}). Despite the envelope pulse shaping circuit consume less energy per pulse than the VCO, the DCA and the DB-DCO, it presents a greater leakage power, that can be explained by the fact that the envelope pulse shaping circuit core circuit, the fast memory, is composed by 8 shift registers of 8 bits, that implies on a greater number of transistors. Despite the slow memory has more flip-flops than the fast memory, it presents a lower power leakage because its transistors has a transistor width of order of nanometers and a larger transistor length (100 nm).

TABLE 32 – IR-UWB pulse synthesizer static power (μW).

VCO	Carrier Generation Buffer Chain	DCA	Envelope Pulse Shaping Circuit	DB-DCO	Slow Memory	Total
2.52	0.32	0.98	9.354	0.832	0.039	14.045

Table 33 presents a performance comparison of the proposed IR-UWB pulse synthesizer with UWB transmitters reported in Chapter 3. In relation of the reported UWB transmitters, the system addressed in this work is the only one that covers the 3.1-10.6 GHz and addresses the IEEE 802.15.4 and 802.15.6 standard channels, while only the circuit reported in (RYCKAERT et al., 2007) was able have a central frequency range wide enough to cover the 3.1-10.6 GHz, however this circuit is only able to address channels with bandwidth of 500 MHz. An oscillator based on ring oscillator architecture and implemented in 28 nm FD-SOI CMOS technology allow to the proposed system to generate pulses with a sufficiently large central frequency range. Indeed, the 28 nm FD-SOI CMOS design kit were critical to achieve this frequency range, given that similar oscillator architectures, done in 65 nm bulk CMOS like the one reported in (VAUCHE; MUHR; TALL et al., 2015) was not fully able to cover the FCC band.

TABLE 33 – Comparison with state-of-the-art UWB transmitters

	Miranda 2010	Vauche 2017[±]	Haapala 2020	Moghtadaei 2014	Phan 2008	Dokania 2020	Schmiclk 2020	Zhao 2013	Ryckaert 2007	De Streel 2017	My work
CMOS Tech. (nm)	65 Bulk	130 Bulk	65 Bulk	90 Bulk	180 Bulk	90 Bulk	180 Bulk	180 Bulk	90 Bulk	28 FD-SOI	28 FD-SOI
VDD (V)	1.2	1.2	1.2	1	1.5	1.2	1	1.8	1	1.2	1
Core Area (mm^2)	0.7	0.11	0.22	0.18	0.30	0.42	0.25	0.08	0.07	0.93	-
Architecture	DL-based	DL-based	DL-based	LO-based (Mixer)	LO-based (LC)	LO-based (LC)	LO-based (LC)	LO-based (Ring)	LO-based (Ring)	LO-based (Ring)	LO-based (Ring)
Spectral compliance	FCC	FCC	ECC	FCC	FCC	FCC	ECC	FCC	FCC	FCC	FCC
IEEE 802.15.4 Channel Covered	-	4	5 to 15	-	1 to 3	1 to 3	5, 6, 8, 9	-	All except 4, 7, 11, 15	1 to 3	All
IEEE 802.15.6 Channel Covered	-	-	3 to 10	0 to 2	0 to 2	0 to 2	-	-	All	0 to 2	All
Modulation	OOK	OOK + DB-BPSK	OOK	BPSK	OOK	OOK	TR-IR-UWB[†]	OOK	BPSK	2-PPM + BPSK	OOK + BPSK
BW(X=10dB) (GHz)	-	1.8-3.5	0.6	2.4-4.6	0.52[◇]	-	0.5[◇]	1.6	0.5	0.8-1[◇]	0.5-1.3
F_c range (GHz)	3.6-7.5	3-5	6.5-8.0	5-5.6	3-5	3.5-4.5	6-8.8	3-5	3-10	3.5-4.5	0.5-12
Maximum Magnitude (Vpp)	0.91	0.90	0.46	0.4	0.16	0.49	1	0.26	-	0.7	1.06
Impedance Load - Z_L (Ω)	50	100	50	50	50	50	50	50	50	50	100
Static Power (μW)	13	100	0.38	-	390	5	1.89	-	640	TX: 106[⊗] SoC: 174[⋆]	14.05
Dynamic Energy E_{ac} (pJ/pulse)	8.5	146	63	14.4	16.8	1	6.2	20	40	TX: 10.4[⊗] SoC: 13.2[⋆]	158
Emitted Energy - E_p (pJ/pulse)	2.4	0.48	0.83	0.78	0.11	0.84	4.38	0.07	-	0.24	2.31
Efficiency - E_p/E_{ac} (pJ/pulse)	15.3	0.32	1.28	2.6	0.63	1.68	4.73	0.35	-	2.33	
P_c(PRF = 1 MHz) (μW)[⋆]	21.50	246	63.38	-	406.80	6	8.09	-	680	TX: 116.4 SoC: 187.2	172
P_c(PRF = 3.90 MHz) (μW)[⋆]	46.15	669.4	246	-	455	8.9	26.1	-	796	TX: 146.6 SoC: 225.4	630
P_c(PRF = 15.6 MHz) (μW)[⋆]	145.6	2377.6	983.2	-	652	20.6	98.6	-	1264	TX: 268.2 SoC: 379.9	2478
P_c(PRF = 62.4 MHz) (μW)[⋆]	543.4	9210	3931	-	1438	67.40	388.8	-	3136	TX: 755 SoC: 995.8	9873
Simulation/Mesure	Mesure	Mesure	Mesure	Post-layout	Mesure	Mesure	Mesure	Mesure	Mesure	Mesure	Simulation

[⋆] Estimated power consumption.
[±] Paper also includes a receiver.
[◇] Estimated from the reported pulse waveform.
[⊗] Estimated from the paper available data (TX)
[⋆] Estimated from the paper available data (SoC)
[†] Double Pulse Transmit-Reference

6 CONCLUSION

This dissertation work presented the study and design of a pulse radio UWB synthesizer targeting the 3.1-10.6 GHz frequency band using the 28 nm CMOS FD-SOI technology. The FD-SOI technology was introduced and UWB communications principles were approached. The proposed IR-UWB synthesizer design and simulation are presented. The general architecture is based on pulse generator composed by a gated ring-controlled voltage oscillator, on an envelope shaping circuit and a digitally controlled amplifier. The designed system includes circuits done with both CMOS and CML logics.

Several reported works have already pointed that the IR-UWB transmitter is capable to perform a pulse transmission with high data rate and low power for small and medium area coverage, therefore being well suited of Internet of Things (IoT) and biomedical applications. UWB transmitters based on frequency transposition pulse synthesis technique are more capable to cover a larger frequency band, mainly the ones composed by ring oscillators that can be enabled and disabled. However, a pulse shaping circuit is necessary to ensure that the generated pulses fit into the spectral masks defined by IEEE 802.15.4 and 802.15.6 standards.

In the study case, it was performed transient simulations of the proposed IR-UWB pulse synthesizer addressing several IEEE standardized channels, where the main goal is to observe if the generated pulse respects American regulations (FCC) and IEEE standard spectral restrictions, mostly the IEEE 802.15.4. The parametric simulations showed that IR-UWB pulse amplitude and power consumption are susceptible to the pulse central frequency, mostly for higher frequencies, where the parasitic capacitances present major effects. In relation of the design of the envelope shaping circuit, the architecture based on CMOS flip-flops presented the lowest power consumption and power leakage. Besides, the transient simulations of the proposed system showed that it is fully capable to address all of IEEE 802.15.4 and 802.15.6 standardized channels, with a power leakage of 14 uW and maximal energy per pulse consumption of 308 pJ. Using the 28 nm CMOS FD-SOI technology, it was possible to implement a pulse synthesizer capable to cover the 3.1-10.6 GHz band, that is the frequency band of interest for UWB applications.

6.1 PERSPECTIVES FOR FUTURE WORK

Perspectives for future work are:

- To design a synchronization circuit
- To layout the IR-UWB pulse synthesizer
- To extract the layout parasites of the proposed circuit
- To optimize the transistor sizing using the values of the parasitic capacitances extracted
- To perform post-layout simulations
- To perform post-layout Monte Carlo simulations
- To study the exploitation of forward back gate biasing to achieve fine tuning
- To study other pulse envelopes shapes

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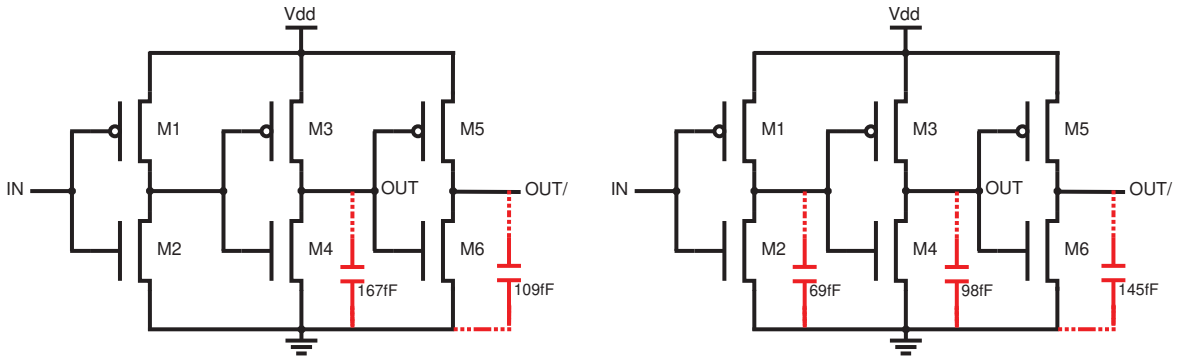
- SCHOULTEN, F. A.; MARIANO, A. A. ; VAUCHE, R. ; BOURDEL, S. ; GAUBERT, J. ; DEHAESE, N. ; BARTHELEMY, H. . IR-UWB Pulse Synthesizer Based on a Sample & Hold Envelope Shaping Circuit. In: 36th South Symposium on Microeletronics, 2021. Proceedings of the 36th South Symposium on Microeletronics, 2021.
- SCHOULTEN, F. A.; MARIANO, A. A. ; VAUCHE, R. ; BOURDEL, S. ; MUHR, E. ; GAUBERT, J. ; DEHAESE, N. ; BARTHELEMY, H. . Low Power Ultra-Wide Band Pulse Generator based on a Duty-Cycled 2-ASK Emitter. In: 19th IEEE Interregional NEWCAS Conference, 2021. Proceedings of the 19th IEEE Interregional NEWCAS Conference, 2021.

B CIRCUIT DESIGN INCLUDING PARASITIC CAPACITANCE

The IR-UWB proposed pulse synthesizer design blocks and schematics including parasitic capacitances are presented here. The values of parasitic capacitances of the blocks VCO Control Module (a), Carrier generation (b) and digital controlled amplifier (c) of Figure 49 were extracted from a parasitic extraction of an IR-UWB pulse generator reported in (MUHR, 2016) employing the 65-nm bulk CMOS technology. In relation of blocks like envelope shaping circuit (d), DB-DCO of 8 bits (e) and slow memory (f), the parasitic capacitances values have been chosen considering the future interconnexion path size in the circuit layout. Indeed, the node connecting two different circuit blocks will have a parasitic capacitance with a higher value.

B.1 VCO CONTROL MODULE



(a) Enable (b) Phase

FIGURE 101 – VCO control modules schematics including parasitic capacitances

B.2 CARRIER GENERATION

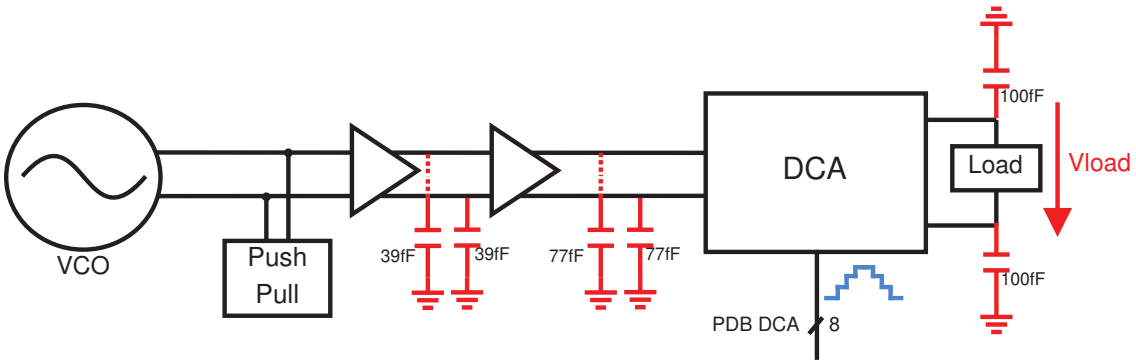


FIGURE 102 – Carrier generation block and 8-bit DCA design including parasitic capacitances

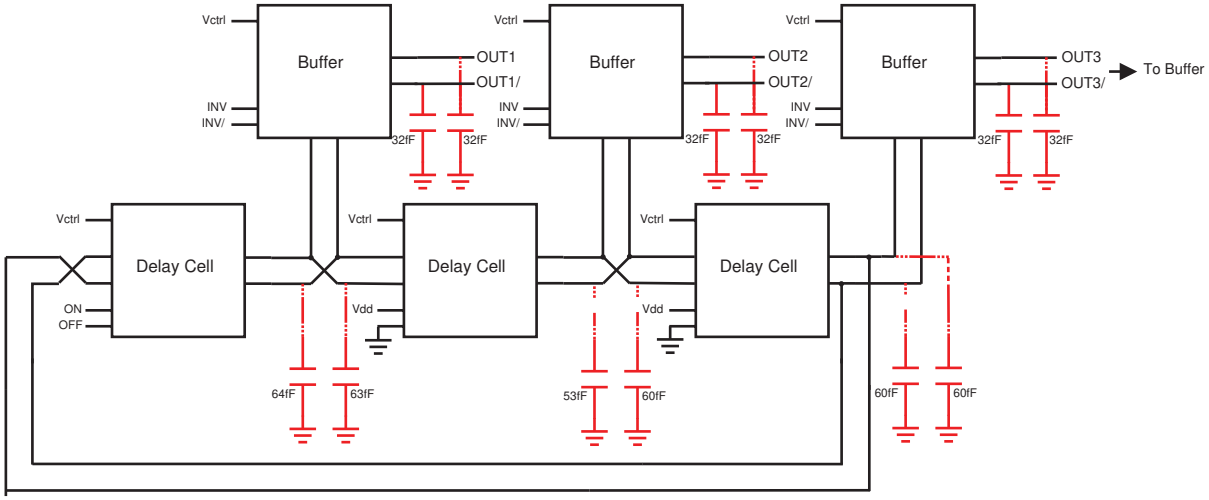


FIGURE 103 – Gated VCO design including parasitic capacitances

B.3 ENVELOPPE SHAPING CIRCUIT

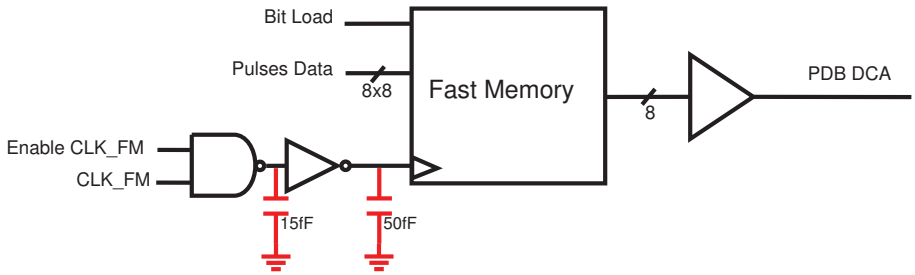


FIGURE 104 – Envelope Shaping Circuit design including parasitic capacitances

B.3.1 Based on CMOS flip-flops

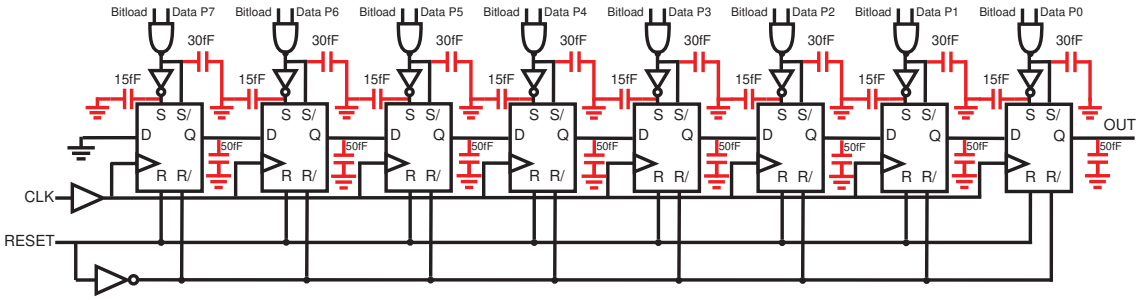


FIGURE 105 – 8-bit CMOS shift register with asynchronous preset and reset including parasitic capacitances

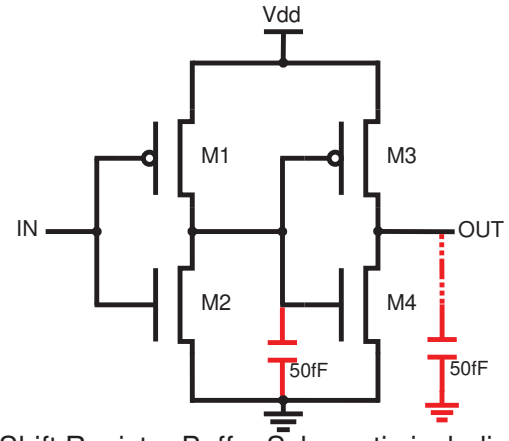
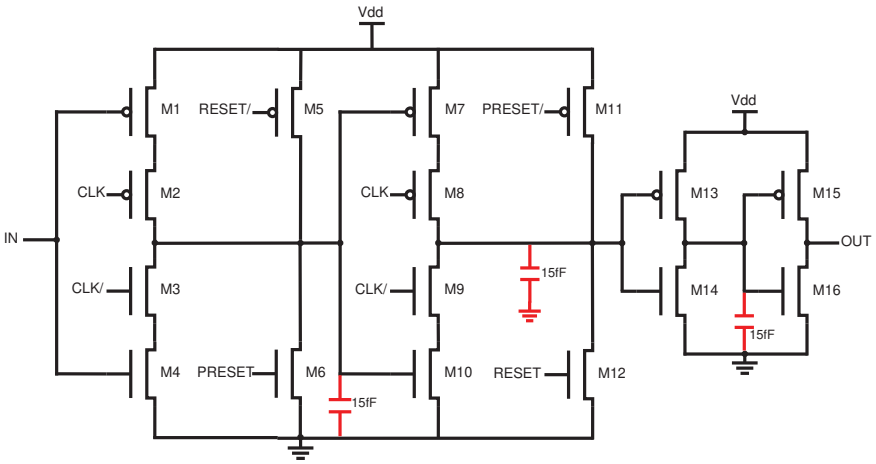
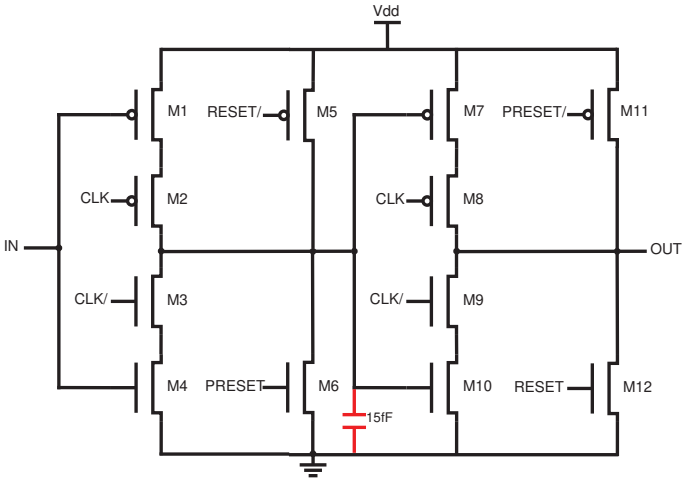


FIGURE 106 – CMOS Shift Register Buffer Schematic including parasitic capacitances



(a) With buffering stage



(b) Without buffering stage

FIGURE 107 – CMOS high asynchronous reset and preset flip flop schematic with parasitic capacitances

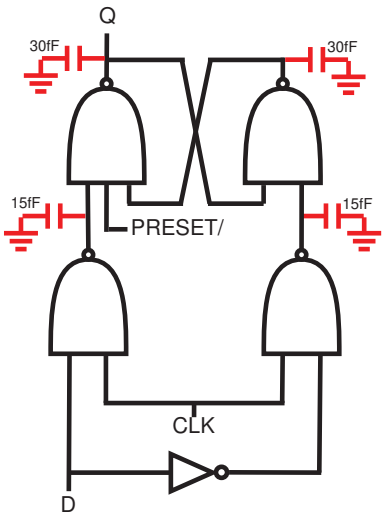


FIGURE 108 – CMOS high asynchronous preset latch schematic including parasitic capacitances

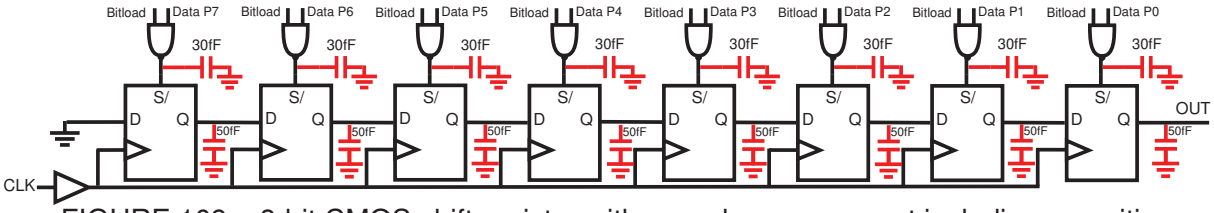


FIGURE 109 – 8-bit CMOS shift register with asynchronous preset including parasitic capacitances

B.3.2 Based on CML flip-flops

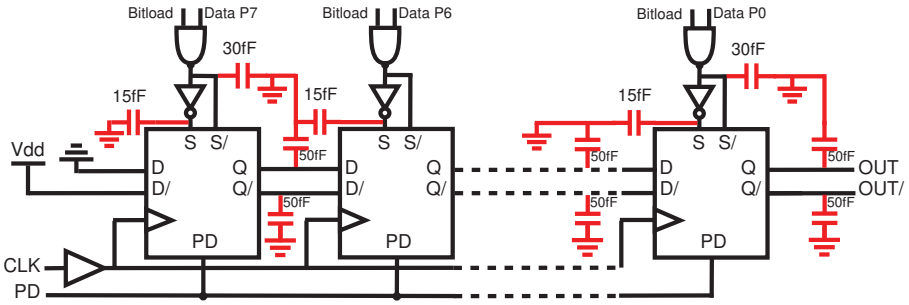


FIGURE 110 – CML-N Shift Register with asynchronous preset including parasitic capacitances

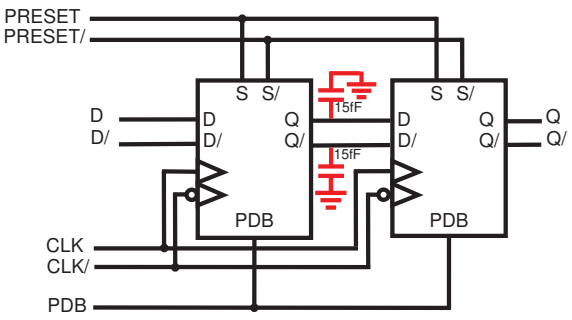


FIGURE 111 – CML-N high asynchronous preset flip flop schematic including parasitic capacitances

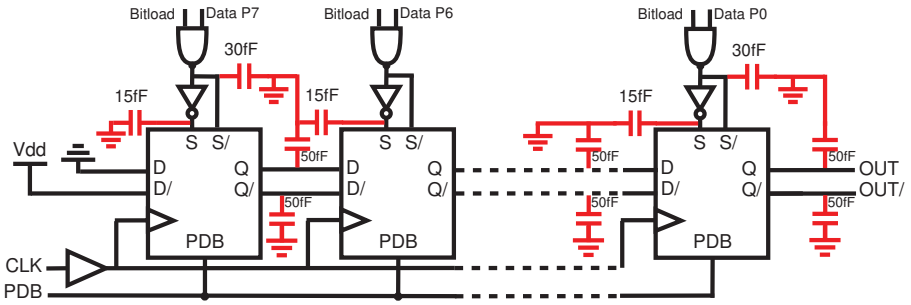


FIGURE 112 – CML-P Shift Register with asynchronous preset including parasitic capacitances

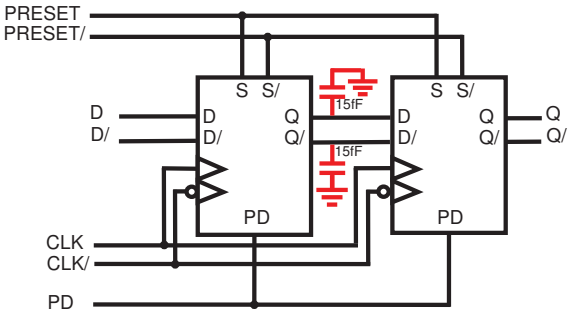


FIGURE 113 – CML-P high asynchronous preset flip flop schematic including parasitic capacitances

B.4 DB-DCO

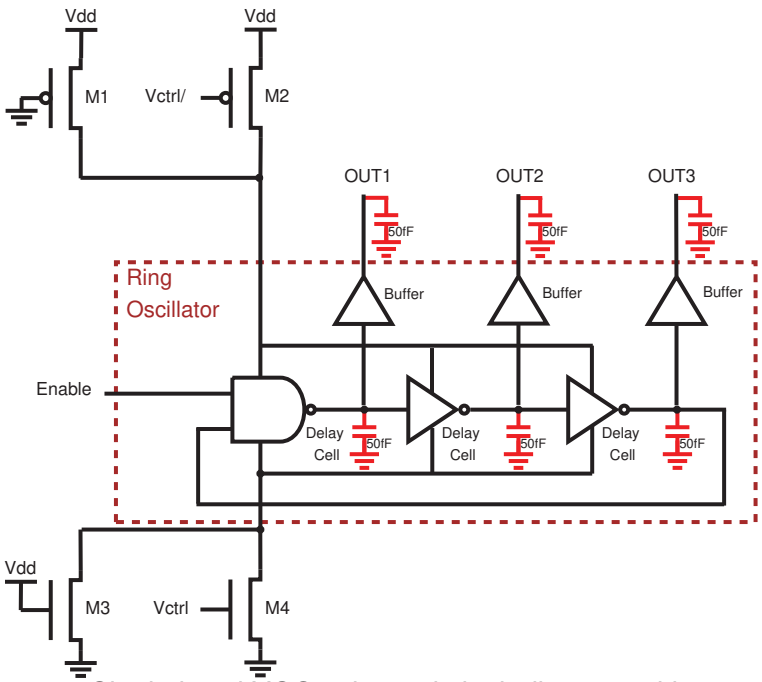


FIGURE 114 – Single band VCO schematic including parasitic capacitances

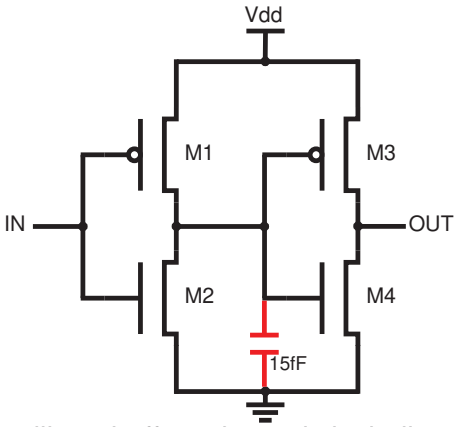


FIGURE 115 – Ring oscillator buffer schematic including parasitic capacitances

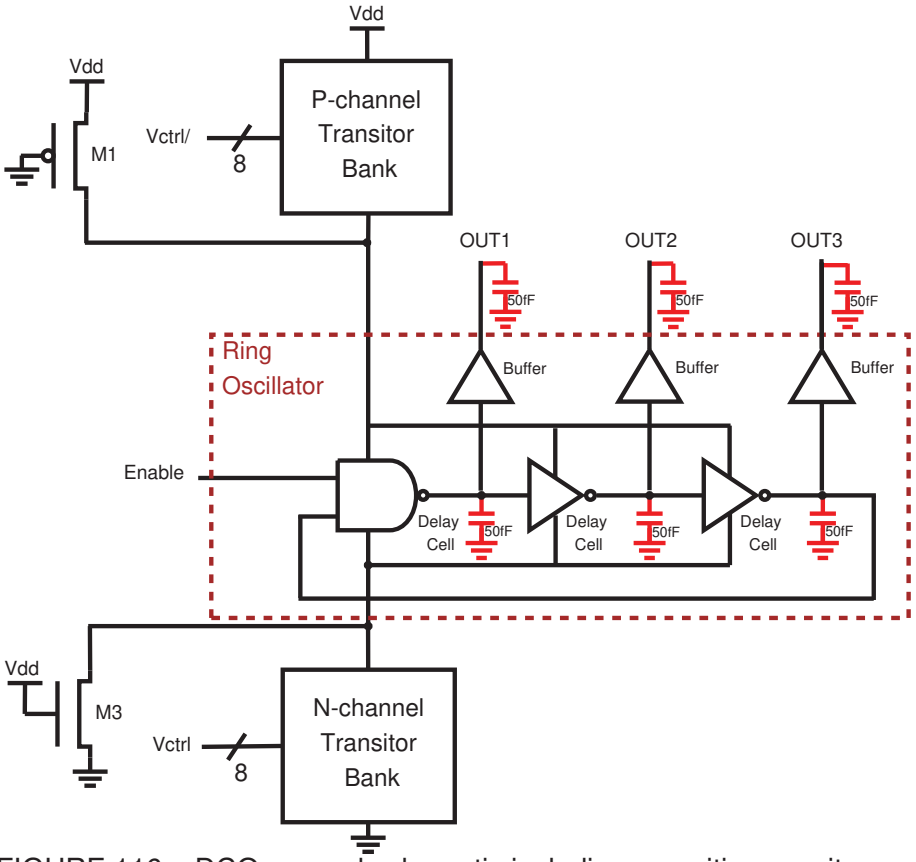


FIGURE 116 – DCO general schematic including parasitic capacitances

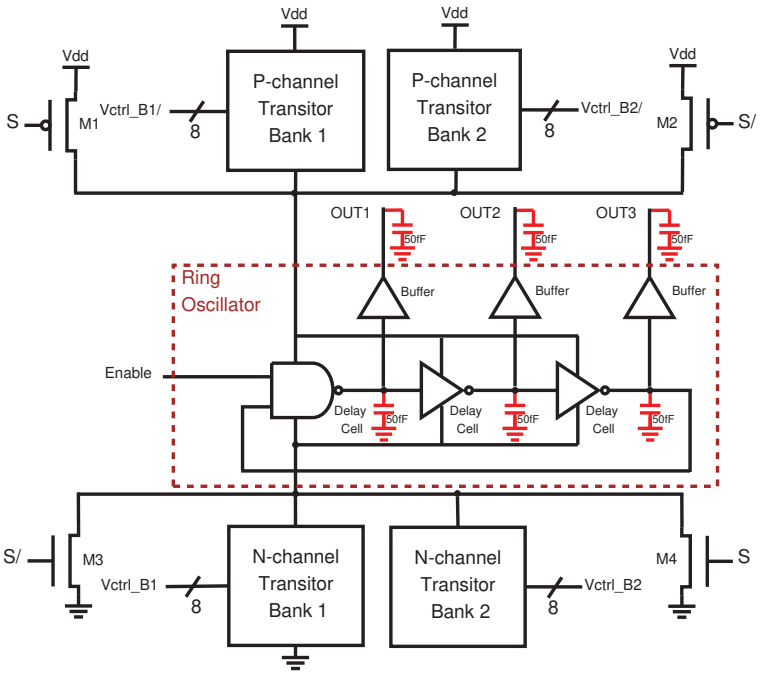


FIGURE 117 – DB-DCO core schematic including parasitic capacitances

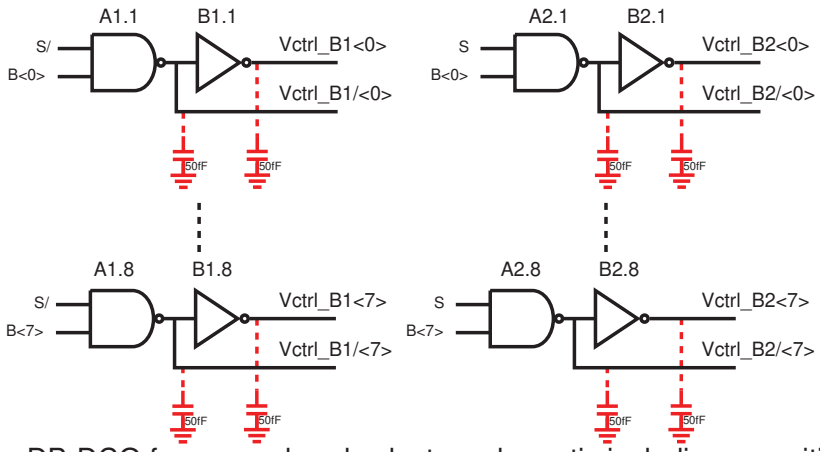


FIGURE 118 – DB-DCO frequency band selector schematic including parasitic capacitances

B.5 SLOW MEMORY

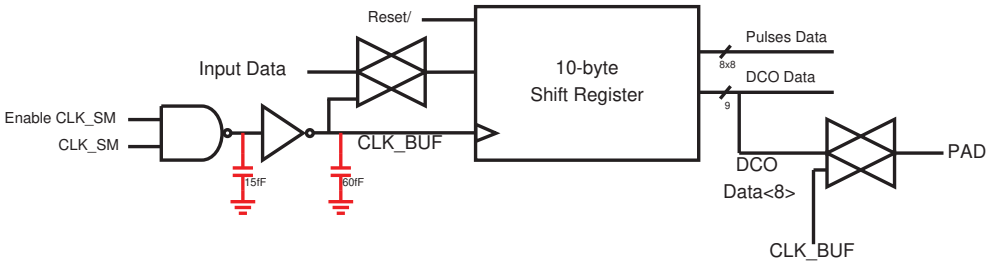


FIGURE 119 – Slow Memory design including parasitic capacitances

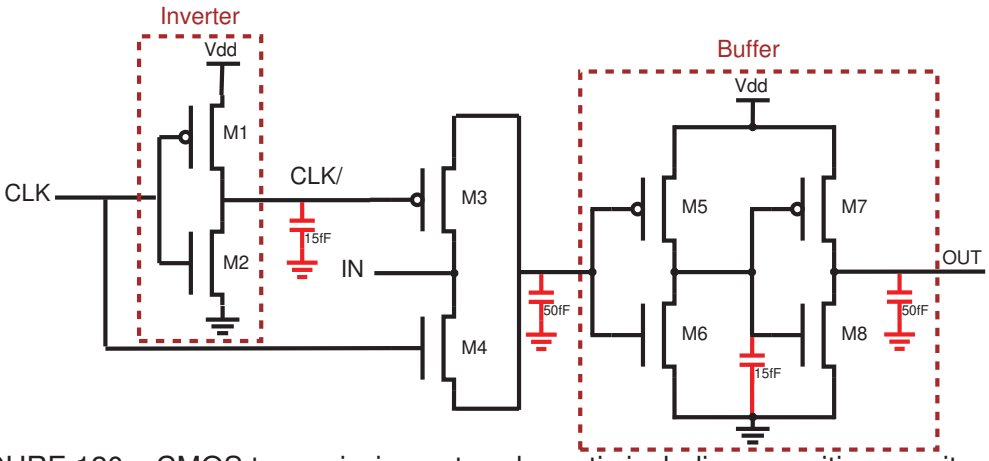


FIGURE 120 – CMOS transmission gate schematic including parasitic capacitances

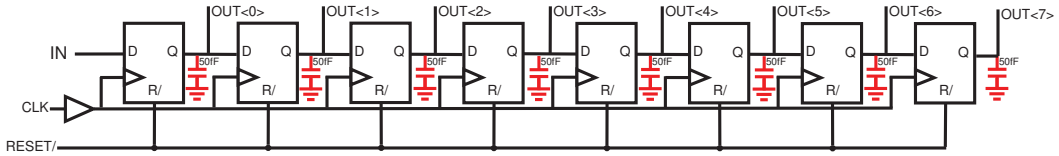


FIGURE 121 – 1-byte serial-in and parallel-out shift register design including parasitic capacitances

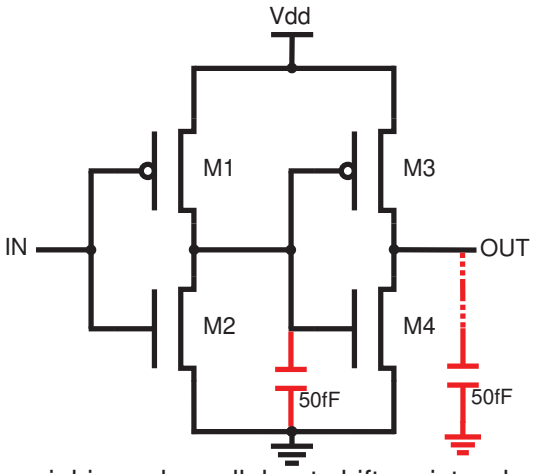


FIGURE 122 – 1-byte serial-in and parallel-out shift register design including parasitic capacitances

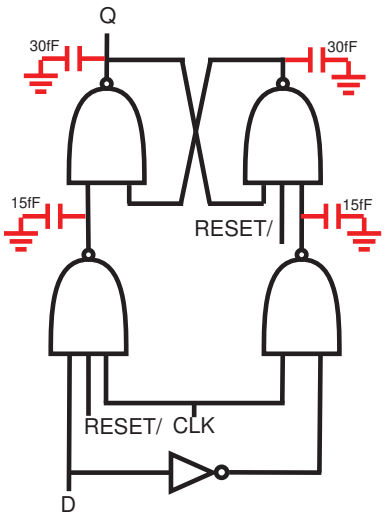


FIGURE 123 – CMOS low asynchronous reset latch schematic including parasitic capacitances