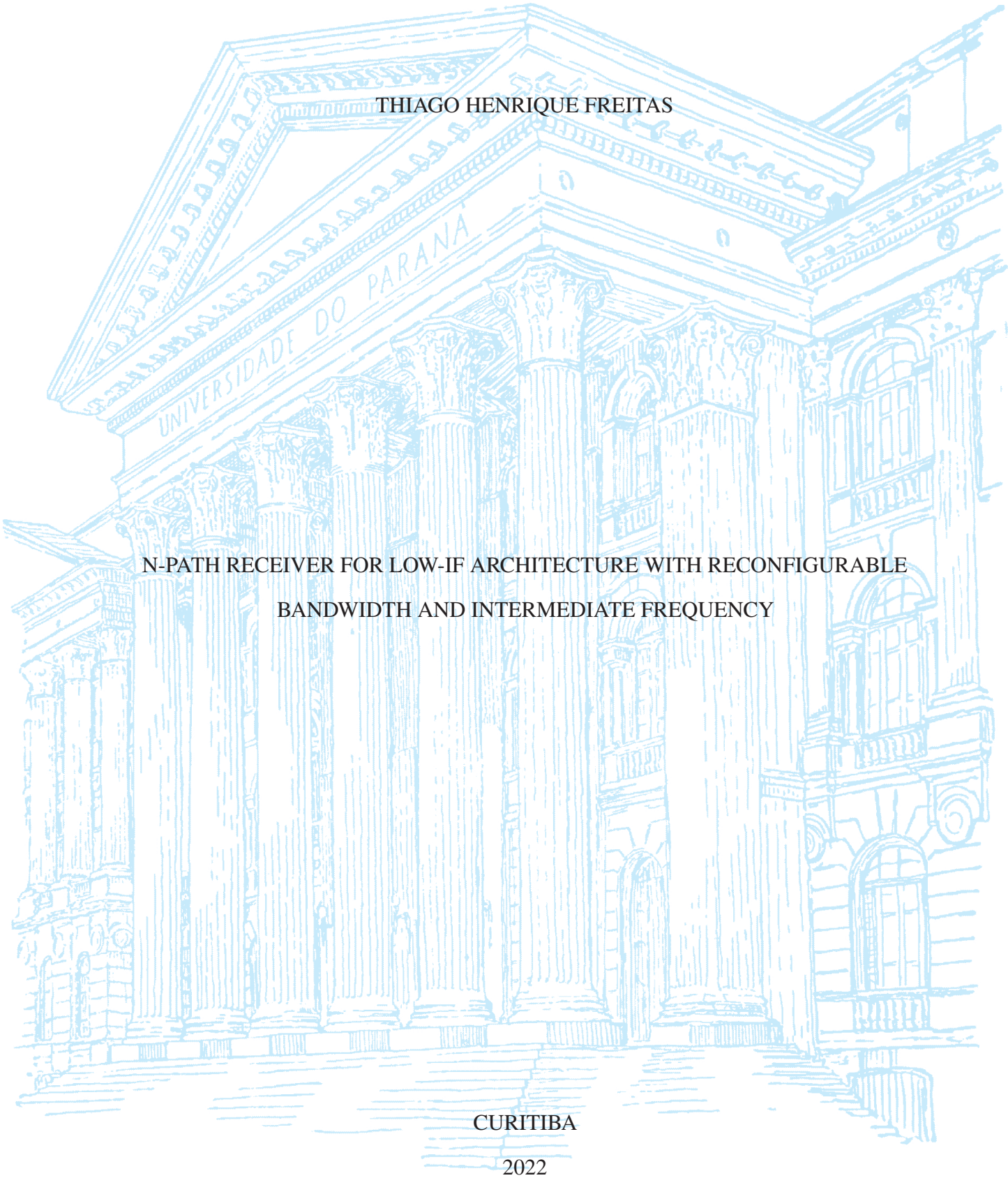
UNIVERSIDADE FEDERAL DO PARANÁ

THIAGO HENRIQUE FREITAS



N-PATH RECEIVER FOR LOW-IF ARCHITECTURE WITH RECONFIGURABLE BANDWIDTH AND INTERMEDIATE FREQUENCY

CURITIBA

2022

THIAGO HENRIQUE FREITAS

N-PATH RECEIVER FOR LOW-IF ARCHITECTURE WITH RECONFIGURABLE BANDWIDTH AND INTERMEDIATE FREQUENCY

Dissertação apresentada como requisito parcial à obtenção do grau de Mestre em Engenharia Elétrica no Programa de Pós-Graduação em Engenharia Elétrica, Setor de Tecnologia, da Universidade Federal do Paraná.

Orientador: Prof. Dr. Luis Henrique Assumpção Lolis.

Coorientador: Prof. Dr. André Augusto Mariano.

CURITIBA

2022

DADOS INTERNACIONAIS DE CATALOGAÇÃO NA PUBLICAÇÃO (CIP)
UNIVERSIDADE FEDERAL DO PARANÁ
SISTEMA DE BIBLIOTECAS – BIBLIOTECA CIÊNCIA E TECNOLOGIA

Freitas, Thiago Henrique
N-Path receiver for Low-if architecture with reconfigurable bandwidth and intermediate frequency. / Thiago Henrique Freitas. – Curitiba, 2022.
1 recurso on-line : PDF.

Dissertação (Mestrado) – Universidade Federal do Paraná, Setor de Tecnologia Programa de Pós-Graduação em Engenharia Elétrica.
Orientador: Prof. Dr. Luis Henrique Assumpção Lolis.
Coorientador: Prof. Dr. André Augusto Mariano.

1. Engenharia elétrica. 2. Rádio - Transmissores e transmissão. 3. Radiodifusão digital. 4. Wireless communication systems. I. Lolis, Luis Henrique Assumpção. II. Mariano, André Augusto. III. Universidade Federal do Paraná. Programa de Pós-Graduação em Engenharia Elétrica. IV. Título.

Bibliotecário: Nilson Carlos Vieira Junior CRB-9/1797

TERMO DE APROVAÇÃO

Os membros da Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação ENGENHARIA ELÉTRICA da Universidade Federal do Paraná foram convocados para realizar a arguição da Dissertação de Mestrado de **THIAGO HENRIQUE FREITAS** intitulada: **N-PATH RECEIVER FOR LOW-IF ARCHITECTURE WITH RECONFIGURABLE BANDWIDTH AND INTERMEDIATE FREQUENCY**, sob orientação do Prof. Dr. LUIS HENRIQUE ASSUMPÇÃO LOLIS, que após terem inquirido o aluno e realizada a avaliação do trabalho, são de parecer pela sua APROVAÇÃO no rito de defesa.

A outorga do título de mestre está sujeita à homologação pelo colegiado, ao atendimento de todas as indicações e correções solicitadas pela banca e ao pleno atendimento das demandas regimentais do Programa de Pós-Graduação.

CURITIBA, 08 de Abril de 2022.

Assinatura Eletrônica
11/04/2022 15:52:00.0
LUIS HENRIQUE ASSUMPÇÃO LOLIS
Presidente da Banca Examinadora

Assinatura Eletrônica
11/04/2022 15:24:40.0
EDUARDO GONÇALVES DE LIMA
Avaliador Interno (UNIVERSIDADE FEDERAL DO PARANÁ)

Assinatura Eletrônica
11/04/2022 18:36:35.0
DEAN BICUDO KAROLAK
Avaliador Externo (UNIVERSIDADE FEDERAL DE ITAJUBÁ)

RESUMO

Os dispositivos de comunicação sem fio estão cada vez mais presentes, e com o aumento no número desses dispositivos, o número de protocolos de frequência também aumenta. É desejado que os receptores de RF (radiofrequência) operem em todas estas frequências. Tecnologias como SDR (Rádio Definido por Software), cadeias de comunicação nas quais a maior parte dos componentes de comunicação é implementada em software, apresentam ampla reconfigurabilidade. Assim também é desejada uma ampla reconfigurabilidade do receptor RF, na sua frequência de operação e se possível também na largura de banda. Boa parte das arquiteturas reconfiguráveis mais recentes usam vários filtros BAW (*Bulk Acoustic Wave*) e SAW (*Surface Acoustic Wave*), filtros que apresentam boa linearidade e seletividade, mas não são reconfiguráveis. Assim, torna-se necessário o uso de vários filtros (cada um numa frequência central específica). Outra solução é a implementação de uma arquitetura de banda larga o suficiente para abranger todo o espectro de frequência desejado, mas isto traz interferências de frequências fora da banda.

Para atender essa demanda, o trabalho atual faz uso de receptores *mixer-1st* baseados em filtros *N-Path*. Filtros *N-Path* apresentam a vantagem de apresentar reconfigurabilidade, bom fator de qualidade, boa seletividade, além de poder ser implementado em tecnologia CMOS (Complementary Metal-oxide-semiconductor) (diferentemente de filtros BAW e SAW). O dispositivo é conectado logo no começo da cadeia, sem a necessidade de um LNA (amplificador de baixo ruído) em RF. Esses filtros apresentam boa linearidade e figura de ruído competitiva. Entretanto filtros baseados em *N-Path*, em sua maioria, são implementado numa arquitetura de conversão direta. Essas arquiteturas apresentam diversas não idealidades como por exemplo offset DC, não linearidades de segunda-ordem e, especialmente, ruído 1/f. Como este bloco será o primeiro componente da cadeia, qualquer técnica que venha a melhorar a figura de ruído é válida.

Este trabalho consiste em implementar uma arquitetura *N-Path mixer-1st low-IF* (frequência intermediária), minimizando assim as não idealidades das arquiteturas de conversão direta. A reconfigurabilidade da frequência central é intrínseca ao filtro *N-Path*, mas este trabalho também almeja reconfigurar a frequência intermediária e a largura de banda. A arquitetura alcança uma largura de banda de 1,25 MHz até 10 MHz, frequência de chaveamento entre 1 GHz e 2 GHz e frequência intermediária entre 1,25 MHz e 10 MHz. Neste trabalho são deduzidas equações que auxiliam na escolha dos componentes para cada uma das frequências intermediárias e larguras de banda. Simulações de impedância de entrada e ganho de tensão são usadas para validar das equações para cada um dos modos de operação.

Palavras-chave: Filtro N-Path. Low-IF. Mixer-1st.

ABSTRACT

Wireless communication devices become more present each day, and with the increasing number of those devices, the number of frequency protocols also increases. It is desired that RF (radio frequency) receivers operate in all frequency protocols. Technologies such as SDR (Software Defined Radio), communication chains in which a significant portion of the components is implemented in software, present wide reconfigurability. Thus, it is also wanted wide reconfigurability in the RF receiver, its operating frequency, and, if possible, bandwidth. A significant portion of the current reconfigurable architectures use multiple BAW (Bulk Acoustic Wave) and SAW (Surface Acoustic Wave) filters. Those filters present good linearity and good selectivity but are not reconfigurable. Thus, it becomes necessary the usage of multiple filters (each in a specific central frequency). Another solution is the implementation of architecture with a bandwidth wide enough to include all the desired frequency spectrum, but this brings out-of-band interferences to the architecture.

To meet this demand, this work uses a mixer-1st receiver based on N-Path filters. N-Path filters present as advantage reconfigurability, good quality factor, and good selectivity. In addition, it can be implemented in CMOS (Complementary Metal-oxide-semiconductor) technology (different from BAW and SAW filters). The device is connected as the first block of the chain without an LNA (low-noise amplifier) in RF. Those filters present good linearity and competitive noise figure. However, N-Path-based filters are primarily implemented in a zero-IF (intermediate frequency) architecture. Those architectures present multiple nonidealities, such as DC offset, second-order nonlinearities, and especially 1/f noise. Since this is the first chain component, any technique that improves the noise figure is valid.

This work consists in implementing a low-IF N-Path mixer-1st architecture, reducing the non-idealities of the zero-IF architecture. The central frequency reconfigurability is inherent to the N-Path filter, but this work also aims to reconfigure the intermediate frequency and the bandwidth. As a result, the architecture achieves a bandwidth from 1.25 MHz to 10 MHz, switching frequency between 1 GHz and 2 GHz, and intermediate frequency between 1.25 MHz and 10 MHz. In this work, equations are obtained that help choose the components for each intermediate frequency and bandwidth. Input impedance simulations and voltage gain simulations are used to validate the equations for each operation mode.

Keywords: N-Path filter. Low-IF. Mixer-1st.

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

AC	Alternating Current
BW	Bandwidth
BAW	Bulk Acoustic Wave
CMOS	Complementary Metal-oxide-semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
dB	Decibel
DTPA	Discrete-time parametric amplifier
IB	In-Band
IF	Intermediate frequency
IIP3	Third-Order Intercept Point
LNA	Low-noise Amplifier
LNTA	Low-noise Transcondutance Amplifier
LTI	Linear Time Invariant
MIMO	Multiple Input Multiple Output
MOS	Metal-Oxide-Semiconductor
NF	Noise Figure
NMOS	N-type metal-oxide-semiconductor field-effect transistors
OOB	Out of band
PAC	Periodic AC
PSP	Periodic Scattering Parameter
PSS	Periodic Steady State
Q	Quality Factor
QSM	Quadrature Sampling Mixer
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
SOI	Silicon On Insulator
SP	Scattering Parameters
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator

LIST OF SYMBOLS

f_c	Central Frequency
f_{IF}	Intermediate Frequency
f_{in}	Input Frequency
f_{LO}	Local Oscillator Frequency
f_s	Switching Frequency
R_A	Antenna Resistance
R_{in}	Input Resistance
$R_{in,amp}$	Input Resistance of the Amplifier
R_{sw}	Switch Resistance
T_{on}	On-Switch Period
V_{in}	Input Voltage
Z_A	Antenna Impedance
Z_{in}	Input Impedance
$Z_{in,amp}$	Input Impedance of the Amplifier
ω_{IF}	Intermediate Frequency Angular Frequency

CONTENTS

1 INTRODUCTION

1.1 CONTEXT AND MOTIVATION

Wireless communication devices become more abundant each day, and the increasing number of those devices also brings a large number of frequency protocols. Technologies such as software-defined radio (SDR), technology in which parts of the receiver-transceiver chain are implemented in software, have a very dynamic change in the parameters of the communication chain and require wide reconfigurability. In the RF (radiofrequency) receiver, its bandwidth (BW), central frequency, some of the physical interface connecting with the antenna, and the filters used in those receivers still present a challenge in its reconfiguration [1]. Table 1.1 shows some of the more usual wireless protocol and their center frequency and unfold the necessity of a reconfigurable receiver that addresses all those protocols.

Table 1.1: Communication protocols and its frequencies

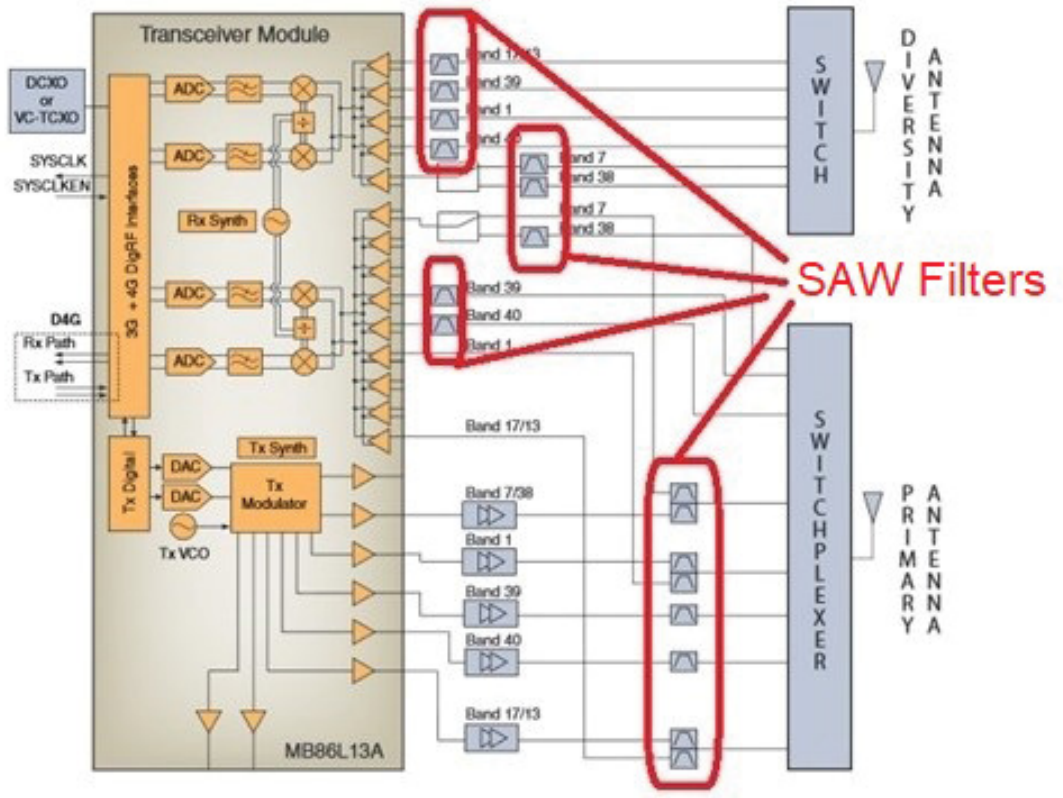
Protocol	**Frequency**
Bluetooth	2.4 GHz
ZigBee	868/915 MHz; 2.4 GHz
Wi-Fi	2.4 GHz; 5 GHz
UWB	3.1-10.6 GHz

Source:[2]

Some reconfigurable RF receivers have a very wide band, but this brings a low rejection for out-of-band (OOB) interferences (selecting both the wanted signal and blockers). Another technique is to have a receiver with multiple parallel front-ends [3], with a BAW (Bulk Acoustic Wave) or a SAW (Surface Acoustic Wave) filter tuned in each center frequency. BAW and SAW filters present good linearity and selectivity but are not reconfigurable (hence the need for multiple filters) furthermore, they are implemented off-chip. When compared to CMOS (Complementary Metal-oxide-semiconductor) technologies solutions, they have the disadvantage in cost and area [4]. Figure 1.1 shows the MB86L13A transceiver, where it is possible to notice many off-chip SAW filters due to the lack of reconfigurability in those filters.

The solution presented in this work is a mixer-1^{st} receiver with an N-Path filter. Mixer-1^{st} receivers are architectures in which the first block of the chain is a mixer (hence the name mixer-1^{st}). N-Path filters consist of switched-capacitor branches that accept signals equal to the switching frequency, f_s. This filtering technique presents a good quality factor, uses integrated CMOS technology and can be reconfigurable. N-path mixer-1^{st} architectures are usually zero-IF (intermediate frequency), so the signal is converted directly to 0 Hz central frequency. Hence,

Figure 1.1: MB86L13A transceiver schematic



Source: adapted from [5]

flicker noise, DC (direct current) offset, and second-order non-linearity can be a problem [6]. As the mixer will be the first block of the complete receiver, the noise should be mitigated as much as possible. The mixer-1st receiver presented in this work uses a low-IF technique [7]. The N-Path filter will be reconfigurable in its switching frequency, bandwidth, and low-IF frequency.

1.2 OBJECTIVES

1.2.1 General Objective

The general objective is to project a low-IF mixer-1st architecture based on N-Path filters with reconfigurable f_s, intermediate frequency (f_{IF}) and bandwidth.

1.2.2 Specific objectives

This research has the following specific objectives:

1. Study of N-Path and mixer-1st architectures;
2. Development the N-Path mixer-1st architecture;
3. Deduction of mathematical equations that describe the behavior of the architecture;

4. Study of techniques for reconfiguration of capacitors and resistors;
5. Implementation of reconfigurable capacitors and resistors in the architecture;
6. Validation of the architecture's frequency response with different f_s, f_{IF}, and bandwidth;

1.3 DOCUMENT STRUCTURE

Chapter two provides the necessary theoretical background that helps this work's understanding. It addresses classical N-Path filters and mixer-1^{st} receiver.

Chapter three presents the state of the art of mixer-1^{st} receivers and N-Path filters, presenting commonly used architectures, advantages, and disadvantages.

Chapter four addresses the development of this project. First, the simulations that were used are presented. Then, the chosen topology of the N-Path mixer-1^{st} is presented, describing its operation. A deduction of analytic equations that command the filter operation follows. The chapter is finished with a description of the process used to choose the project parameters.

Chapter five presents the results. It shows the architecture's behavior for different bandwidths, f_{IF}, and f_s, comparing simulation results with the results of the theoretical equations. Input impedance and voltage gain are observed to validate the architecture.

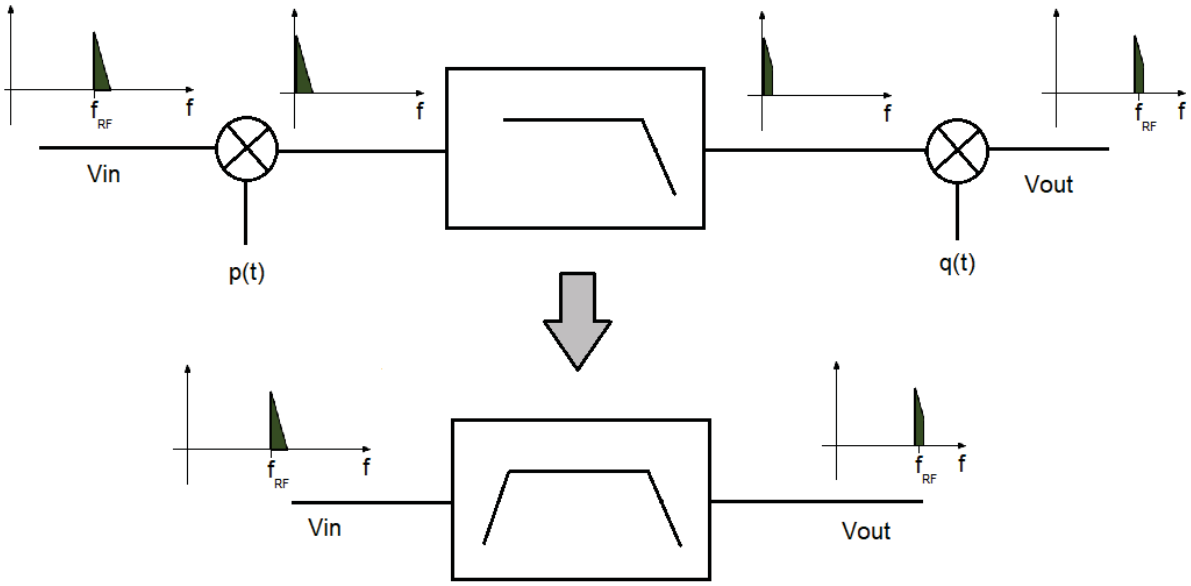
Chapter six presents a brief overview of the results and present what it is planned for future works.

2 THEORETICAL BACKGROUND

2.1 N-PATH FILTER

The N-Path filter's initial idea takes the RF frequency, downconverts, passes it through a low pass filter, and upconverts it [8]. With that, the low pass filter (in baseband) becomes a bandpass filter. Figure 2.1 presents this operation.

Figure 2.1: Representation of the upconversion and downconversion processes in the low pass filter, that results in a bandpass filter

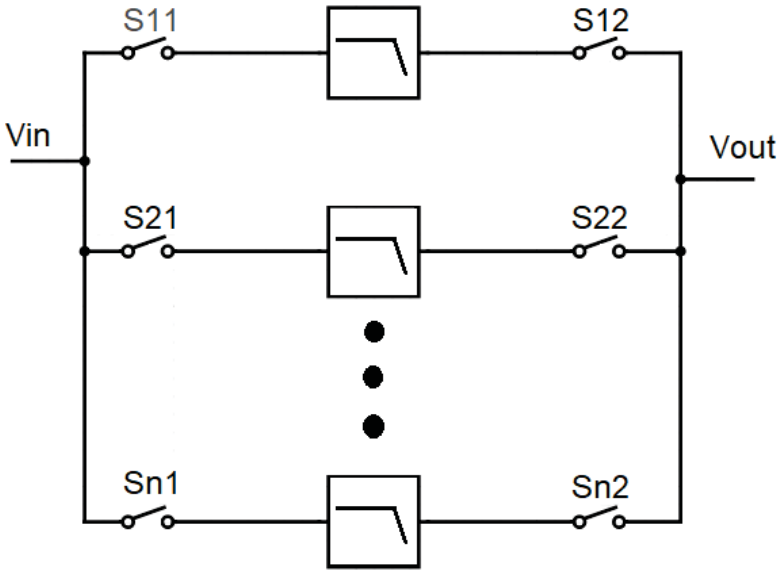


Source: adapted from [8]

The first N-Path topology that uses switches for the process of downconversion and upconversion was presented in [9]. This topology is shown in figure 2.2. Moreover, using as reference the N-Path filter presented in figure 2.2 is possible to exchange the low pass filter for RC filters. The result is presented in figure 2.3.

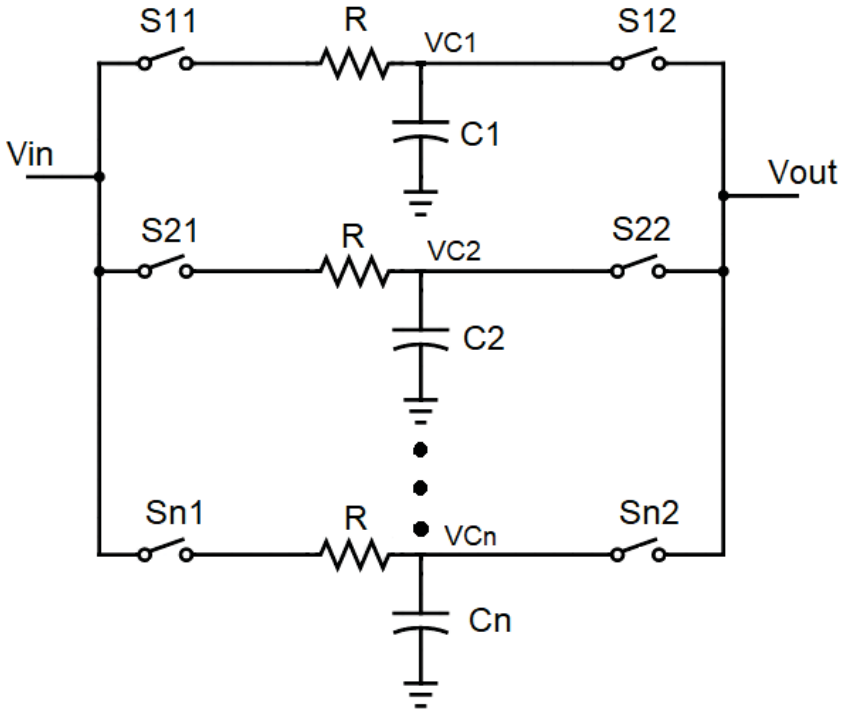
If the frequency shift in the upconversion and the downconversion are the same and the switching is in phase, the switches in the same RC filter in figure 2.3 will have the same behavior (closed and opened simultaneously; $S_{i1} = S_{i2}$ in figure 2.3). Therefore it is possible to remove one of the branches of switches [9]. Figure 2.4 shows this topology, the switches on the right-hand side are removed. The filtered and upconverted signal is obtained at the node V_x, while the voltages in the capacitors (V_{C1}, V_{C2},..., V_{Cn}) give the filtered signal in baseband. The filters in figure 2.2, 2.3 and 2.4 all have the same behavior (if the frequency shift is the same in the upconversion and the downconversion). Thus the most basic topology of the N-Path filter is conceived.

Figure 2.2: N-Path filter using switches for the process of downconversion and upconversion



Source:adapted from [9]

Figure 2.3: N-Path filter topology after exchanging the low pass filters for RC filters

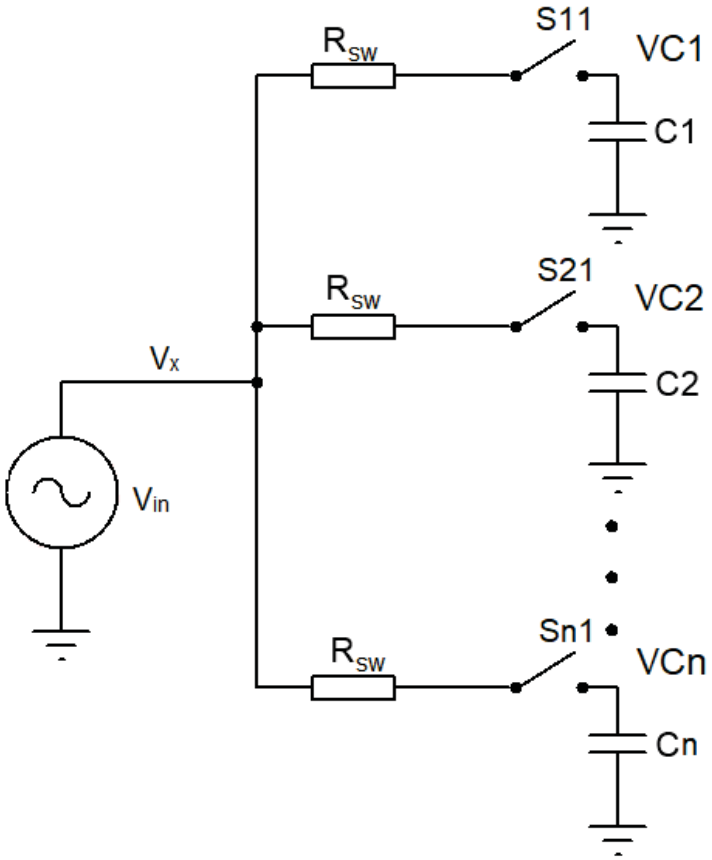


Source:[4]

The filter's switching behaves in a way that the clock's duty cycle is divided in order to close the switches in progression and have only one closed switch at a time [4]. The clock strategy is presented in figure 2.5.

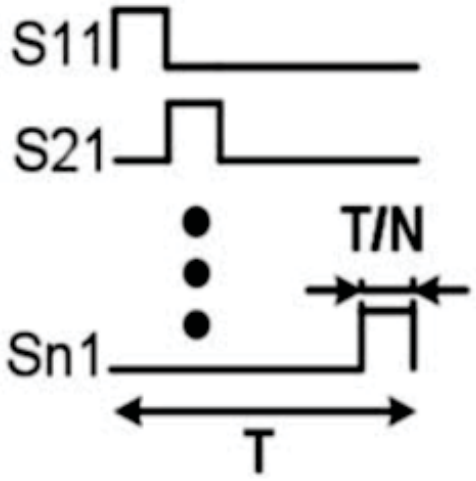
As mentioned before, N-Path filters are reconfigurable bandpass filters. Understanding its operation becomes more accessible in the time domain and assigning a 4-Path value (four

Figure 2.4: N-Path filter topology in which the low pass filters are exchanged for RC filter and the branch of switches in the right hand side are removed



Source:the author

Figure 2.5: Clock strategy for the N-Path switching

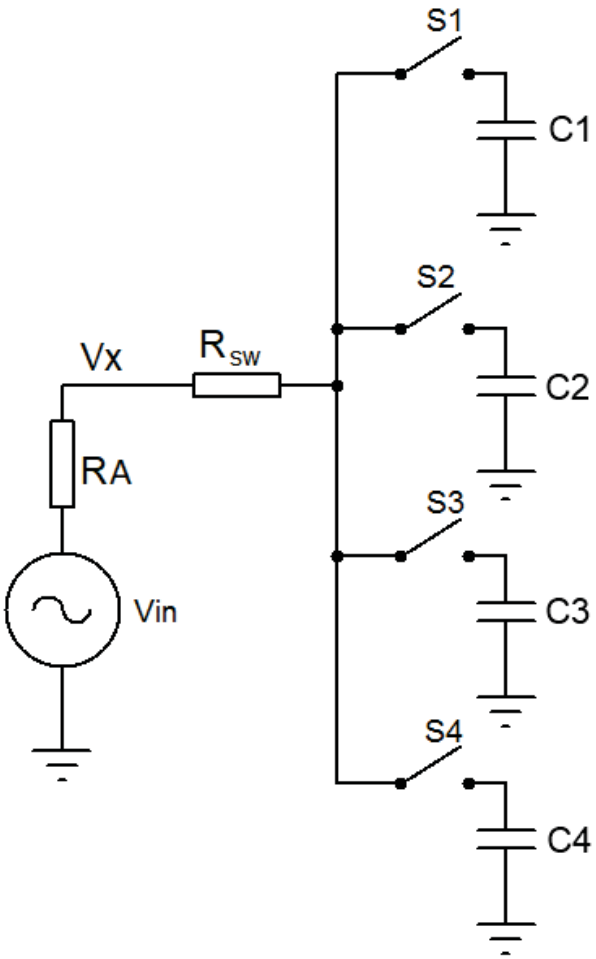


Source:[4]

switch/capacitor branches). The input source "sees" only one R_{sw} (switch resistance) at a time because only one switch is closed at a time. Therefore, it is possible to put R_{sw} before the

branches. This topology is shown in figure 2.6. In order to get the correct behavior, the RC time constant must be very high ($RC >> T_{on}$).

Figure 2.6: 4-Path filter with R_{sw} before the branches



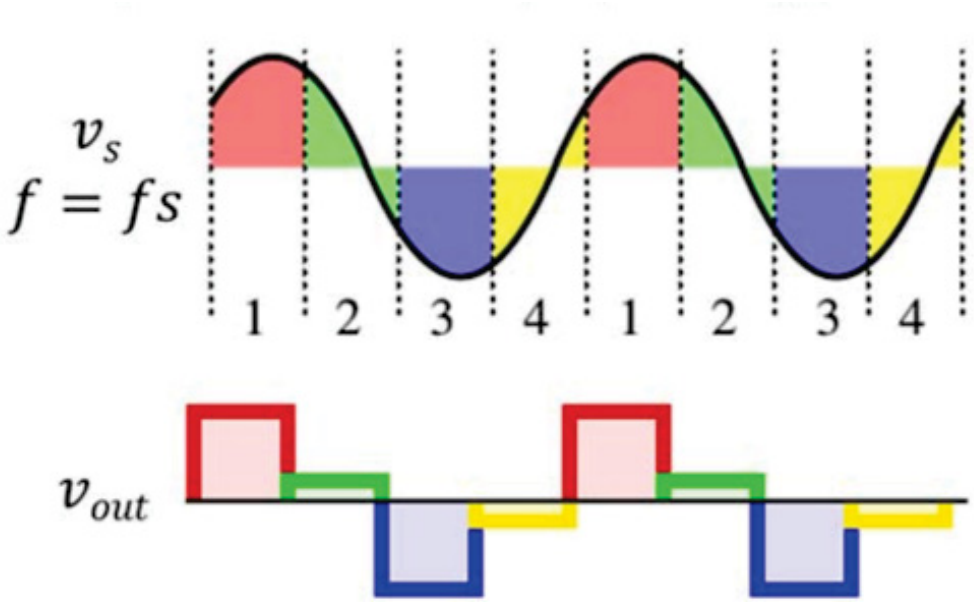
Source: [4]

Any number of paths can be chosen, but the signals at the capacitors are in baseband and give quadrature and in-phase signals. To use all the branches optimally, the number of paths is a power of 2. If the number of paths is not a power of 2, some of the capacitors will become redundant. It is not desired that the number of paths is too low because the sampled waveform in the capacitors will present too many harmonics. It is also not desired that the number of paths is too high because this will increase the LO (local oscillator) phase noise requirements.

First is the scenario in which the f_s is equal to the input frequency, f. Due to the high RC time constant, each capacitor will store a small charge value in the first duty cycle. In the second duty cycle, each capacitor will have the same voltage value in the input as in the first duty cycle because the f_s is equal to the input frequency. Therefore, two equal voltage values are separated by a switching period, T_s. Thus for $f = f_s$, each capacitor will always have the same voltage value in its input. After many duty cycles, the voltage in each capacitor will be

approximately the average voltage of its respective input. Hence the filter accepts frequencies equal to f_s. This operation is presented in figure 2.7.

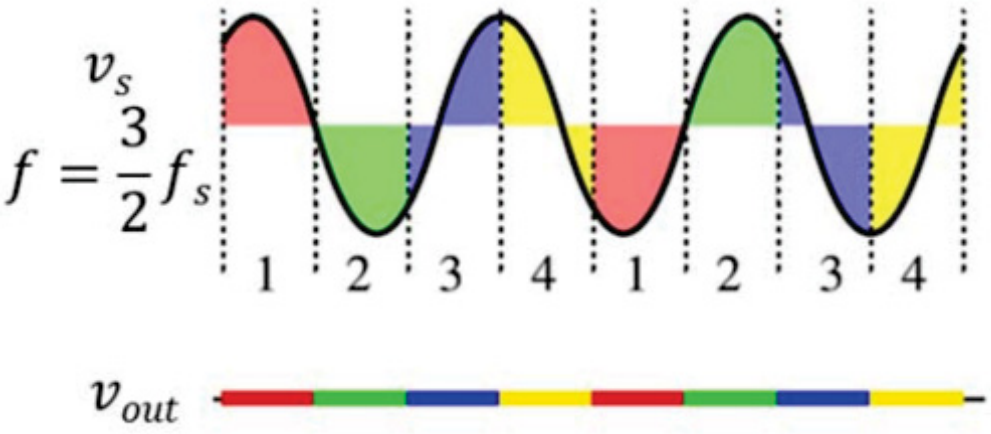
Figure 2.7: The behavior of the N-Path for $f = f_s$



Source:[4]

Now the case in which the f_s is different from the input frequency. In this case, the input voltage in the capacitor will have different values in different duty cycles. There will be a positive voltage in some cycles and a negative one in others. Thus after many duty cycles, the voltage in each capacitor will be close to zero. Hence, the filter attenuates those frequencies. Figure 2.8 presents the filter's input signal and the output signal for $f = 1.5f_s$, that is the frequency with the highest attenuation. Although other frequencies' average voltages are not exactly zero, there still is attenuation.

Figure 2.8: The behavior of the N-Path for $f = 1.5f_s$

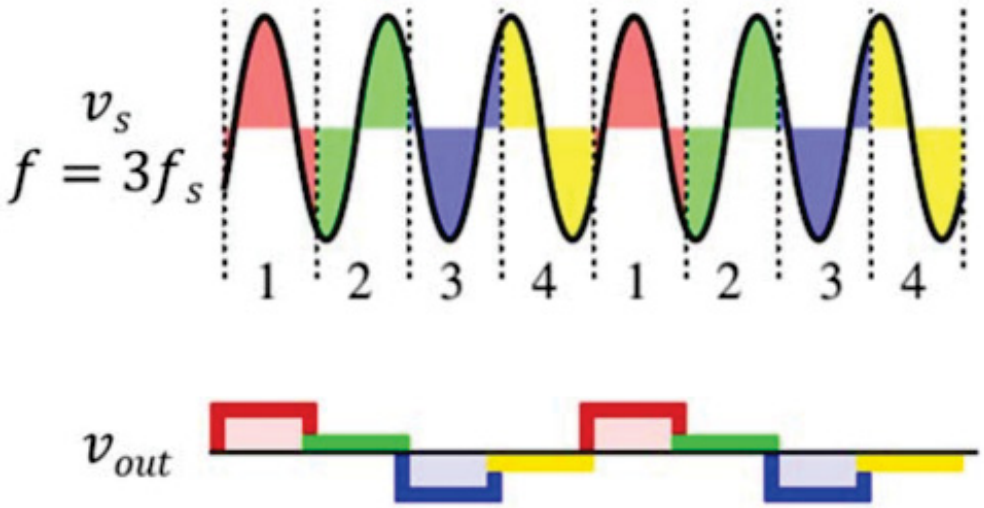


Source:[4]

It is possible to notice that the N-Path filter allows frequencies equal to f_s and attenuates frequencies different from f_s. Hence changing f_s can change the frequencies the N-Path allows, making it a reconfigurable filter.

However, this operation method prompts a disadvantage. If the input frequency is equal to a harmonic of f_s, the filter will also allow this frequency. The input voltage will be the same in each switching period or multiple of it. Therefore harmonics of f_s also cause the capacitors to store the charge of the same input voltage in all duty cycles. Thus the N-Path filter also allows these harmonics. Figure 2.9 displays input and output voltages in the time domain when the input frequency is equal to a harmonic of f_s (in this case $f = 3f_s$).

Figure 2.9: The behavior of the N-Path for $f = 3f_s$



Source:[4]

Once the behavior of the N-path is understood, it is possible to infer which frequencies are accepted and which frequencies are rejected. Figure 2.10 shows the frequency response of the N-path filter.

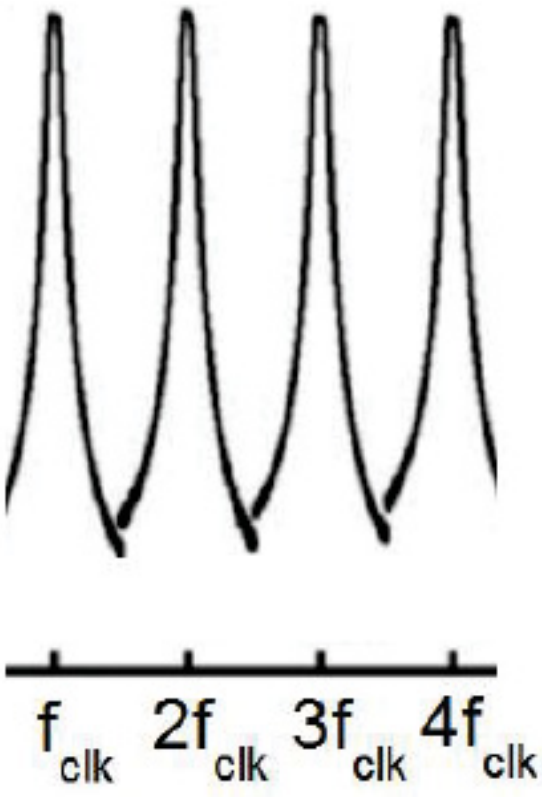
Something worth being observed in the N-Path filter is that a frequency shift happens in tandem with the filtering operation (due to the downconversion of the input signal accomplished in the low-pass filter). This process will be fundamental in the mixer-1^{st} architecture [10].

The equation of a load-less N-path bandwidth (-3dB bandwidth) is presented [4]:

$$BW_{-3dB} = \frac{1}{\pi NRC}. \tag{2.1}$$

Even though equation 2.1 is for a load-less filter, it shows one of the N-path's benefits: the bandwidth is independent of f_c (central frequency), the quality factor ($Q = \frac{f_c}{BW_{-3dB}}$) increases as f_c increases.

Figure 2.10: Theoretical frequency response of the N-path filter



Source:the author

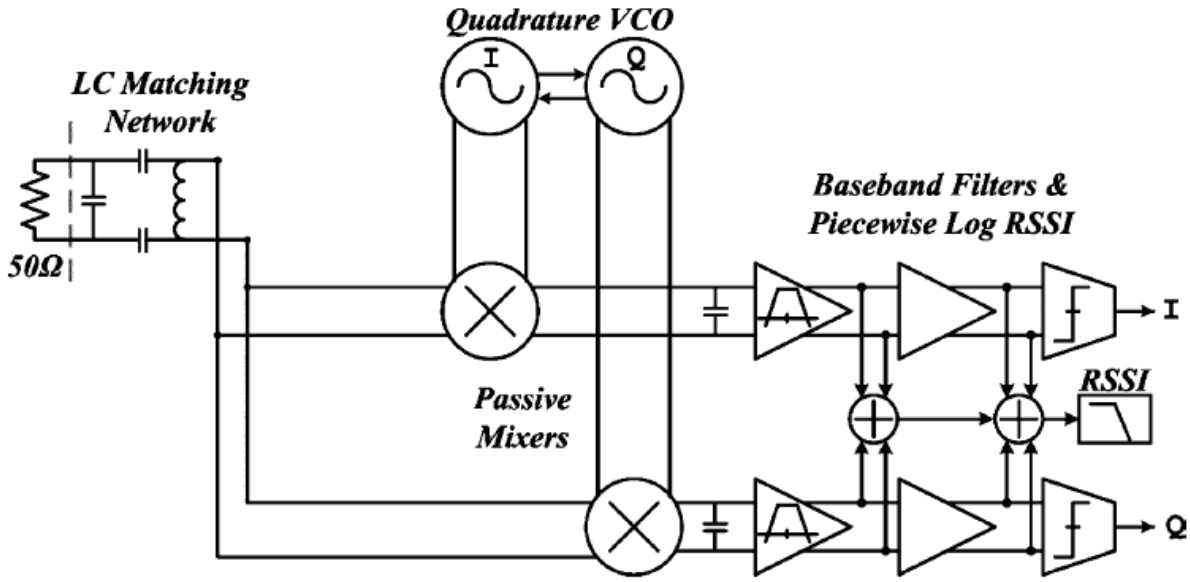
2.2 MIXER- 1^{ST} RECEIVER

Mixer-1^{st} receivers have as the main feature the absence of a Low-Noise Amplifier (LNA) before the mixer. With this, when compared to usual superheterodyne receivers, better linearity is achieved with a slightly higher noise figure (NF). In addition, the spurious-free dynamic range (SFDR) is improved since it is defined by both the NF and IIP3 (third-order intercept point) [4].

One of the first instances where the mixer-1^{st} topology was used was in [11]. An LC network (used for impedance matching) is connected directly to a double-balanced passive mixer in the receiver architecture. The main focus of removing the LNA in [11] is to reduce the power consumption, with application in ultra-low-power 2.4 GHz. The architecture is shown in figure 2.11.

The N-Path filter can be used in the mixer-1^{st} architecture because the signal if taken in the capacitors, will be filtered and downconverted before the amplification. One of the first instances the N-Path filters were used as mixer-1^{st} was in [12], where a 4-Path works as a quadrature sampling mixer (QSM) switched by four non-overlapping 25 % duty cycles. The downconverted and filtered signal is amplified in baseband, and the signal in each capacitor gives the quadrature and in-phase signals ($I+$, $I-$, $Q+$, $Q-$). When compared to sampling mixers,

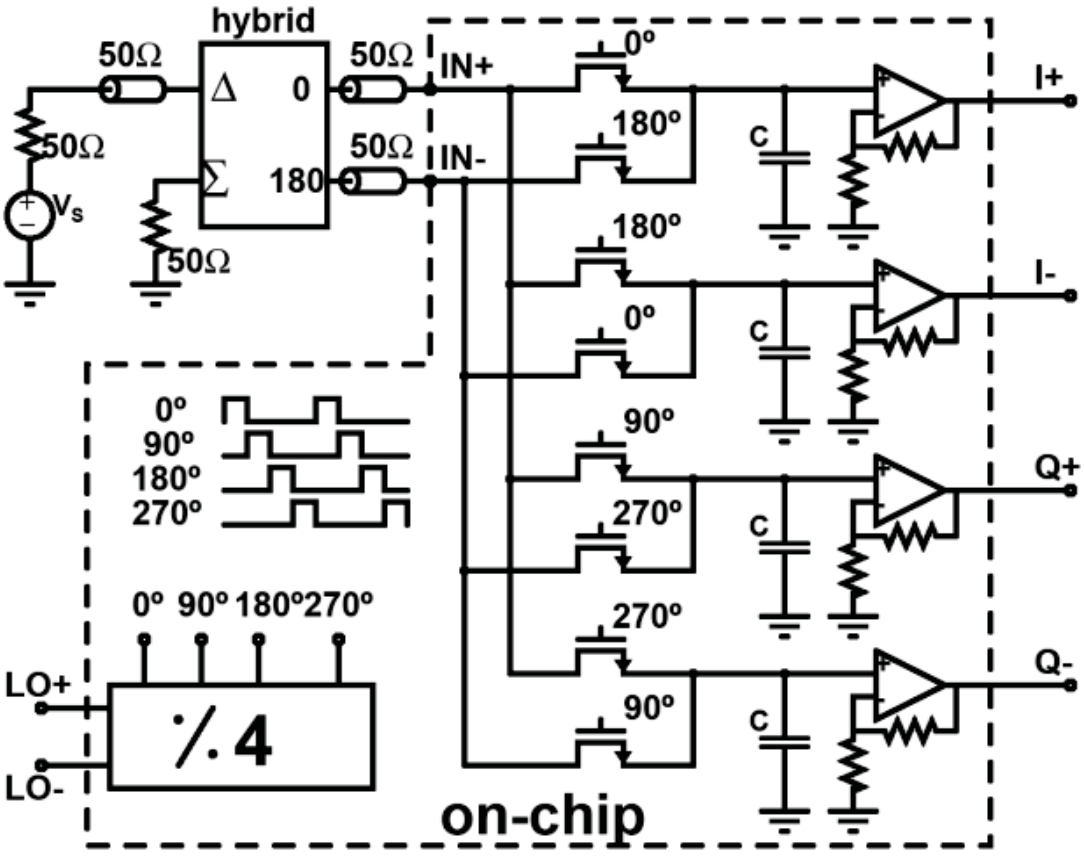
Figure 2.11: LNA-less architecture (mixer-1st)



Source: adapted from [11]

switching mixers present a much lower NF and conversion loss [12]. Figure 2.12 presents the architecture.

Figure 2.12: First N-Path mixer-1st



Source:[12]

3 STATE OF THE ART

N-Path and mixer-1st architectures are often treated as a single architecture. As it was mentioned in chapter 2, mixer-1st architectures are those in which the mixing operation is done before the amplification. Most of the mixer-1st architectures use N-Path techniques because of their filtering operation along with the mixing operation. Even though N-Path filtering has other applications, mixer-1st topologies make better use of the N-Path's advantages. N-Path that acts only as a tunable filter (acting as a "traditional filter") is also of interest in state of the art. Those architectures focus on making the frequency reconfigurability wider, sometimes with a tunable band. Mixer-1st receivers that are not N-Path can be implemented but are not of particular interest in state-of-the-art.

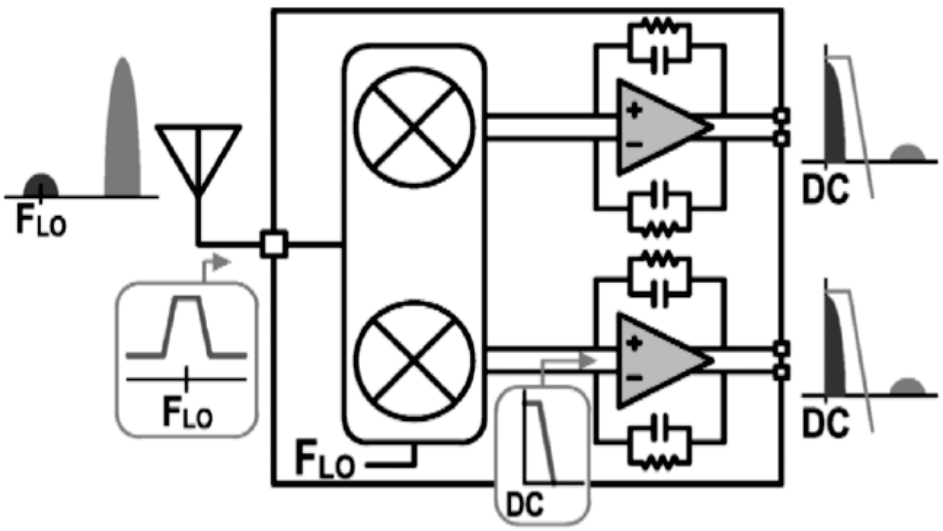
3.1 N-PATH MIXER-1ST WITH IMPROVED NF

As mentioned before, N-Path mixer-1st architectures have the advantage of having very high linearity and noise slightly higher than the architecture of the usual superheterodyne receivers. However, there is a focus on improving the noise even more. Recent works found room for improvement, relaxing the trade-off between linearity and noise.

One of the first attempts to mitigate the noise in the mixer-first was presented in [13]. It also aims to avoid voltage gain at blocker frequencies and to achieve it without SAW filters. So the most significant challenge addressed in [13] is the design of an architecture that presents competitive NF, achieved by a significant voltage amplification, without conventional SAW filters and tuned LNA. The architecture is presented in figure 3.1. The noise cancellation is achieved using two downconversion paths. Since the author aims to remove SAW filters from the architecture, N-Path was used. Using N-Path, it was possible to achieve: two downconversion paths and baseband filtering before the noise cancellation process. The voltage gain of blocker frequencies was avoided, and the trade-off between NF and OOB linearity was relaxed due to the baseband filtering before the noise cancellation. It operated with an RF frequency between 80 MHz and 2.7 GHz with a 72 dB gain. The architecture achieves an NF of 1.9 dB at 2 GHz and presents a noise degradation in the presence of a 0 dBm blocker of 4.1 dB. In terms of OOB rejection, it achieved 42 dB and 45 dB rejection for the 3rd and 5th harmonic, respectively. An OOB-IIP3 of 13.5 dB is achieved in a 40 nm CMOS technology.

The most recent works use TIA (transimpedance amplifier) for noise-canceling. The work in [14] uses a second-order noise-canceling technique. A TIA in baseband, in which each of the parameters of interest in mixer-1st architectures are controlled separately (Z_{in}, NF, IB-IIP3, OOB-IIP3, and power consumption), is used. Figure 3.2 shows the feedback amplifier topology. The noise requirement depends on g_{m2} and g_{ma}, the input matching depends on g_{m1}, and the bias currents need to be checked in order to observe if it attends the power consumption requirement.

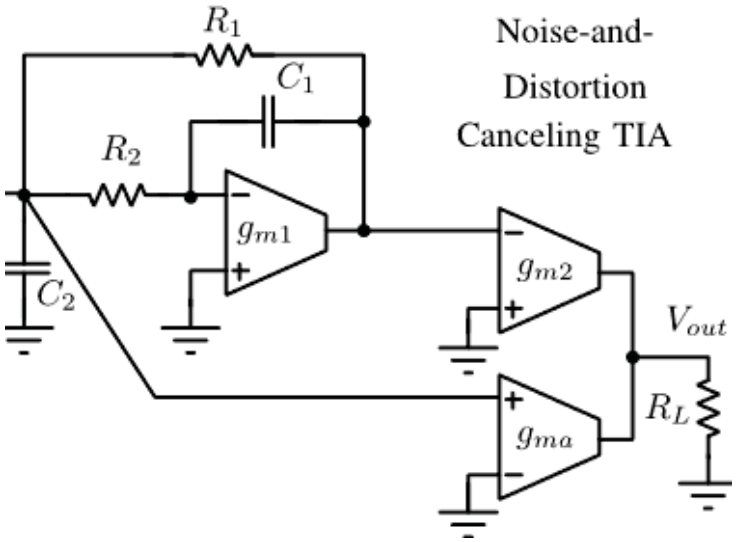
Figure 3.1: Noise cancellation achieved using two downconversion N-Path filters



Source:[13]

If the linearity, IB (in-band) and OOB, is not attended, a linearization technique is necessary for g_{m2}. The components R_2, C_1 and C_2 control the bandwidth. Implemented in 180 nm CMOS, it achieves an NF between 3.4 dB and 4 dB, IB-IIP3 of 14 dBm, OOB-IIP3 from 25 dBm to 39.8 dBm, and power consumption between 45 mW and 135 mW. With a frequency range of 0.2-1.2 GHz and baseband bandwidth of 18 MHz.

Figure 3.2: Feedback amplifier used for noise cancellation



Source: adapted from [14]

The work in [15] also uses a noise-canceling technique with TIA, but it uses it in a first-order inverter configuration, a more simple approach when compared to [14]. Due to its low complexity, it was only possible to improve the in-band linearity. It focuses on an application with a substantial bandwidth (175 MHz). Many signals are present in the band of interest in those

situations, and IB linearity is a key parameter. The receiver presented in [15] can be used in a full-duplex receiver with a self-interference cancellation and in MIMO (multiple input multiple output) applications due to its high IB linearity and large bandwidth. The receiver operates with two amplifier paths for noise-cancellation: the main path with one amplifier; an auxiliary path with an amplifier, and a low-noise transconductance amplifier (LNTA). The high linearity is achieved with a virtual ground between the input of the amplifiers and the LNTA. Input matching is achieved with a resistor before the amplifier in the main path. This architecture presents 9dBm IB-IIP3, NF between 2.5 dB and 5 dB, with a central frequency varying from 1 GHz to 6 GHz in a 28 nm technology.

In [16] it is aimed to enhance the linearity and suppress OOB blockers. In comparison with [15] and [14] it presents a low power consumption (17.2 mW). The feedback amplifier is present in each of the paths of the 4-Path filter, as can be observed in figure 3.3. The authors in [16] improve the LO phase noise to improve the linearity of the receiver as a whole. The feedback amplifiers and their components are chosen to achieve a Butterworth response with $Q = 0.7$. This work has the advantage of embedding the feedback amplifier presented in any mixer-1^{st} receiver. The architecture achieves NF of 3.1 dB, with degradation of only 0.9 dB in the presence of a 0 dBm blocker; IIP3 of 27 dBm; B1dB of 13 dBm.

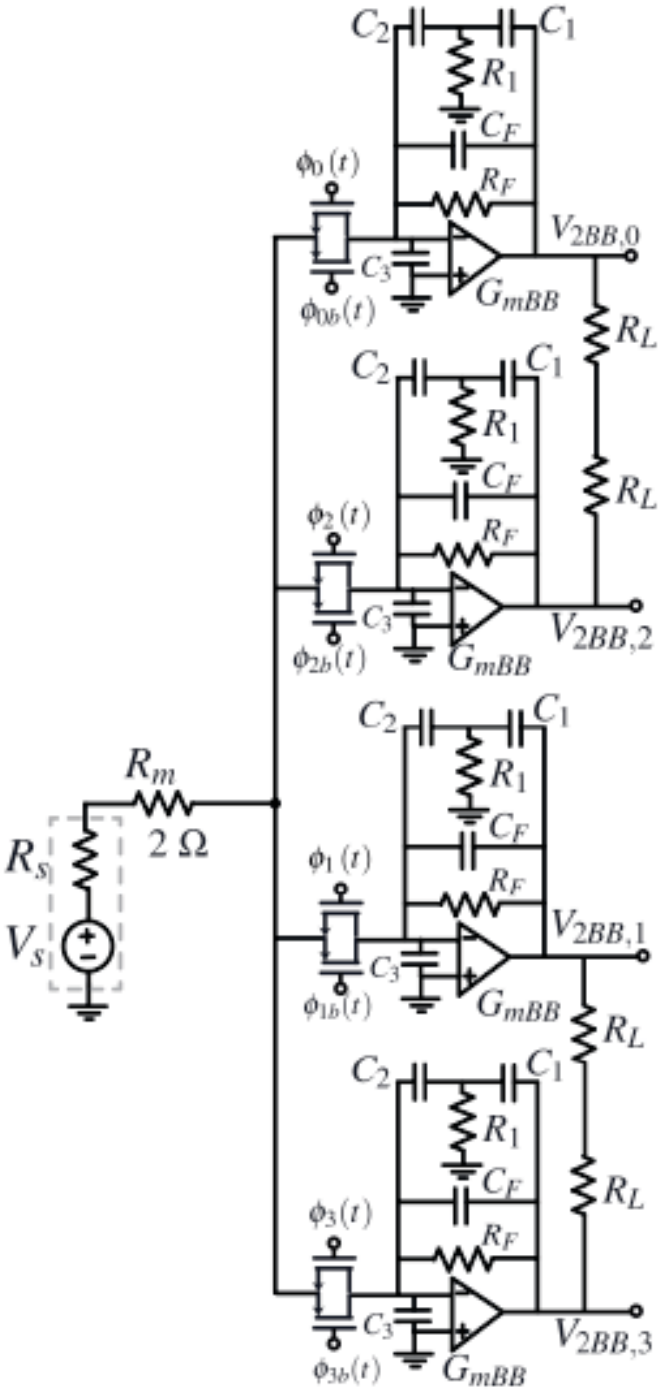
3.2 N-PATH MIXER-1^{ST} WITH FOCUS ON 8-PATH MIXING

Some works have a focus on using 8-path mixing, which for a long time was not used because it needs a 12.5 % duty cycle clock. Due to the need of flat gain and phase until the 5^{th} harmonic, 12.5 % is very hard to achieve in high frequencies [17]. Hence, applications in high RF and mm-Wave focused mainly of 4-Path mixing. But 8-path mixing has the advantage of reducing harmonic reradiation (even eliminating some of the harmonics) [3], a wider input impedance matching [17] and reducing noise folding [18].

In [17] the author makes use of an overlapping suppression technique in the LO. With that, it is possible to use a duty cycle of 25 %, reducing the requirements of the LO in high frequencies. Furthermore, the work puts interleaved inductors that reduce the IB loss due to clock overlapping, as demonstrated in [19]. The work divides the 8-Path mixer into two 4-Path sub mixers, fed by a 25 % duty cycle. The sub mixers will present a voltage difference, which will induce a current flow. The inductors are seen in series between the mixers and, in this situation, present a high impedance, reducing the LO current leakage associated with the clock overlapping. Implemented in 45 nm SOI (silicon-on-insulator) technology, and thanks to the 8-path mixing, an operation from 3.7 GHz to 6.5 GHz is achieved. The architecture's NF is between 2.4 dB and 4.7 dB, and the OOB-IIP3 of 28 dBm. The power consumption is between 89 mW and 135 mW.

In the research presented in [18] it is applied a leakage suppression in the LO to reduce the mismatch between the signals and the LO buffer. LO leakage suppression is achieved with a wide band impedance match using a DAC (digital-to-analog converter). Each pair of paths in

Figure 3.3: N-Path filter with feedback amplifiers



Source: adapted from [16]

the N-Path filter presents a DAC. The LO leakage results from mismatches between the mixers and the buffers of the LO. It is possible to minimize it with the DACs, which have 5-bits and fine-tunes the size of the circuit devices. It achieves an NF between 2.4 dB and 2.6 dB, improved due to the noise folding reduction that 8-path mixing brings, and operates between 400 MHz and 3.5 GHz. The architecture can suppress down below -62 dBm and presents harmonics rejection

of 47 dB and 51 dB for the 3^{rd} and 5^{th} harmonics, respectively. It operates with an RF frequency between 400 MHz and 3.5 GHz, with a bandwidth between 15 MHz and 50 MHz.

3.3 N-PATH MIXER-1^{ST} WITH ENHANCED OUT-OF-BAND REJECTION AND IMPROVED SELECTIVITY

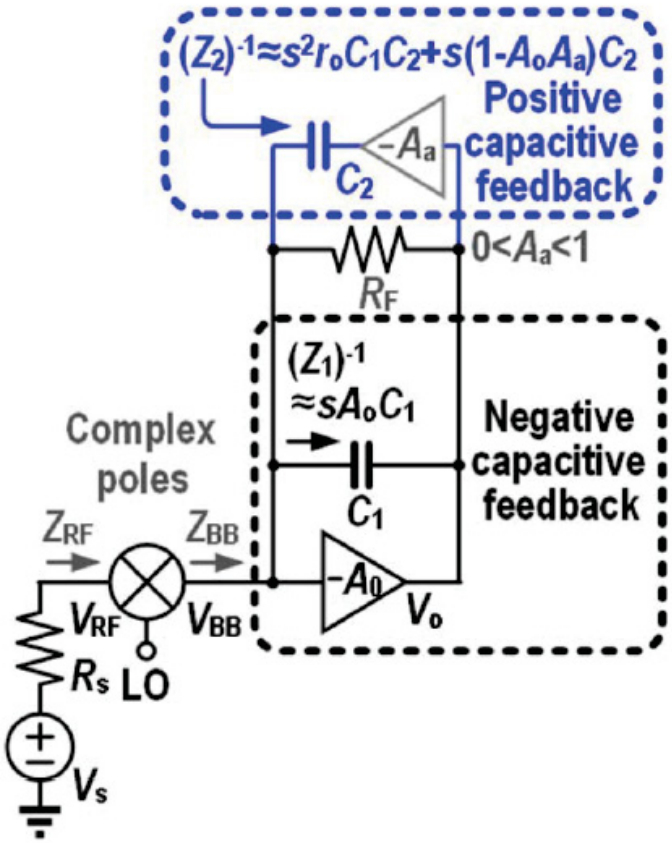
Other works improve the OOB rejection with enhanced selectivity. For example, [20] puts an impedance of 40 dB/decade roll-off in the output of the mixer-1^{st}, in opposition to the usual shunt RC impedance that brings a 20 dB/decade roll-off. A second-order transfer function is needed in order to achieve this objective. The author achieves the transfer function using a parallel combination of negative capacitance and negative resistance. The negative capacitance and resistance are synthesized using an amplifier with positive feedback and cross-coupled transistors as the amplifier's load. The zeros in the output transfer function limit the frequency up to which the 40 dB/decade is achieved. A trade-off between the zero's frequency and power consumption proceeds. The choice for the zero in the transfer function must be carefully taken. If it is too high, it can lead the circuit to instability. The work achieves 33.3 dBm of OOB-IIP3 and a 1 dB blocker compression (B1dB) of 12 dBm for an 18 MHz bandwidth and central frequency varying from 200 MHz to 2 GHz. Presenting an NF between 4.3 dB and 7.6 dB, with degradation for a 0 dBm blocker of less than 2 dB.

The authors in [21] aim to enhance the selectivity and similarly use an amplifier with positive and negative feedback, both paths with capacitances. The architecture is presented in figure 3.4. The positive feedback path works as a "blocking bypassing path," while the negative feedback path gives a better blocker rejection. Both the feedback paths synthesize a pole pair in the input of the baseband amplifier, and those poles are upconverted to RF. The poles on RF reduce distortion and present a better roll-off in the filter. In order to improve the system selectivity and linearity, the circuit also presents a sixth-order bandpass filter, achieved cascading N-Path filters coupled with transconductance amplifiers. The positive feedback in those amplifiers achieves a good frequency range, improved linearity, and a competitive NF (less than 3 dB). It presents a high dynamic range from 200 MHz to 8 GHz, with a 39 dBm OOB-IIP3 and B1dB of 12 dBm for 10 MHz bandwidth. Achieving NF between 2.3 dB and 5.4 dB, with degradation of 2.2 dB for a 0 dBm blocker and 7.1 dB for an 8 dBm blocker.

3.4 N-PATH AS A TRADITIONAL FILTER

Some works do not make use of the N-Path in a mixer-1^{st} topology. For example, [22] uses a gain-boosting technique and the low-noise amplification before the commutation, which improves the NF. The system is presented in figure 3.5. The capacitors are exchanged by transistors and driven by a 50 % duty-cycle signal used for boosting. The amplification is achieved by sampling the input signal in a MOS (Metal-Oxide-Semiconductor) transistor operating as a capacitor with high capacitance. The input is disconnected, and the value is kept constant. The

Figure 3.4: Amplifier with negative and positive feedback



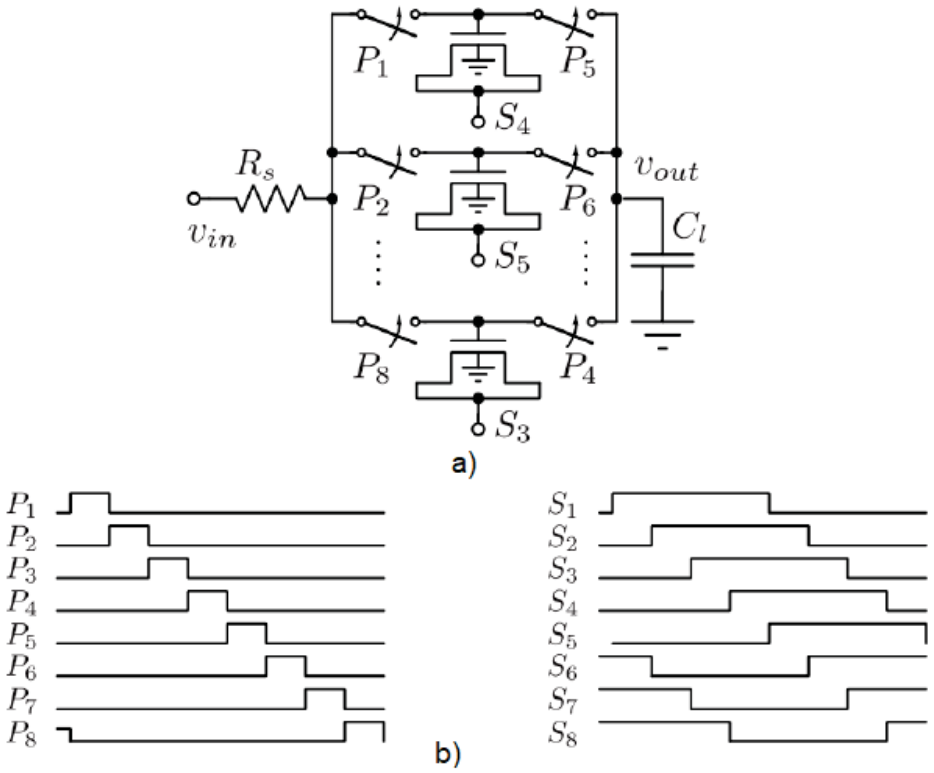
Source:[21]

voltage in the MOS source increases in the next duty cycle, and its capacitance decreases. The charge is kept constant due to the charge conservation principle, so the voltage in the gate has to increase. With that, the signal was amplified by C_{high}/C_{low}. This amplification technique is known as a discrete-time parametric amplifier (DTPA). DTPAs add noise to the system, but this is counterbalanced with amplification before the commutation. The architecture's technique reduces the NF by about 2.2 dB, achieving a final NF from 2.97 dB to 4.08 dB. The IB-IIP3 is 0.3 dBm and the OB-IIP3 10 dBm. This system operates from 0.05 GHz to 0.4 GHz, and its quality factor is between 4 and 8.

3.5 STATE OF THE ART COMPARISON

With the works in state of the art presented, it is necessary to compare them. 3.1 shows a qualitative comparison. As was mentioned before, different works focus on different points, but looking at table 3.1, it is possible to notice that none of the works focus on 1/f noise. This is mainly because all the works presented are zero-IF architectures. This work has the main objective of implementing the N-Path mixer-1st in a low-IF architecture, mitigating the 1/f noise.

Figure 3.5: a) N-Path with gain boosting technique b) clock strategy



Source: adapted from [22]

Table 3.1: Comparison between the works in the state of the art

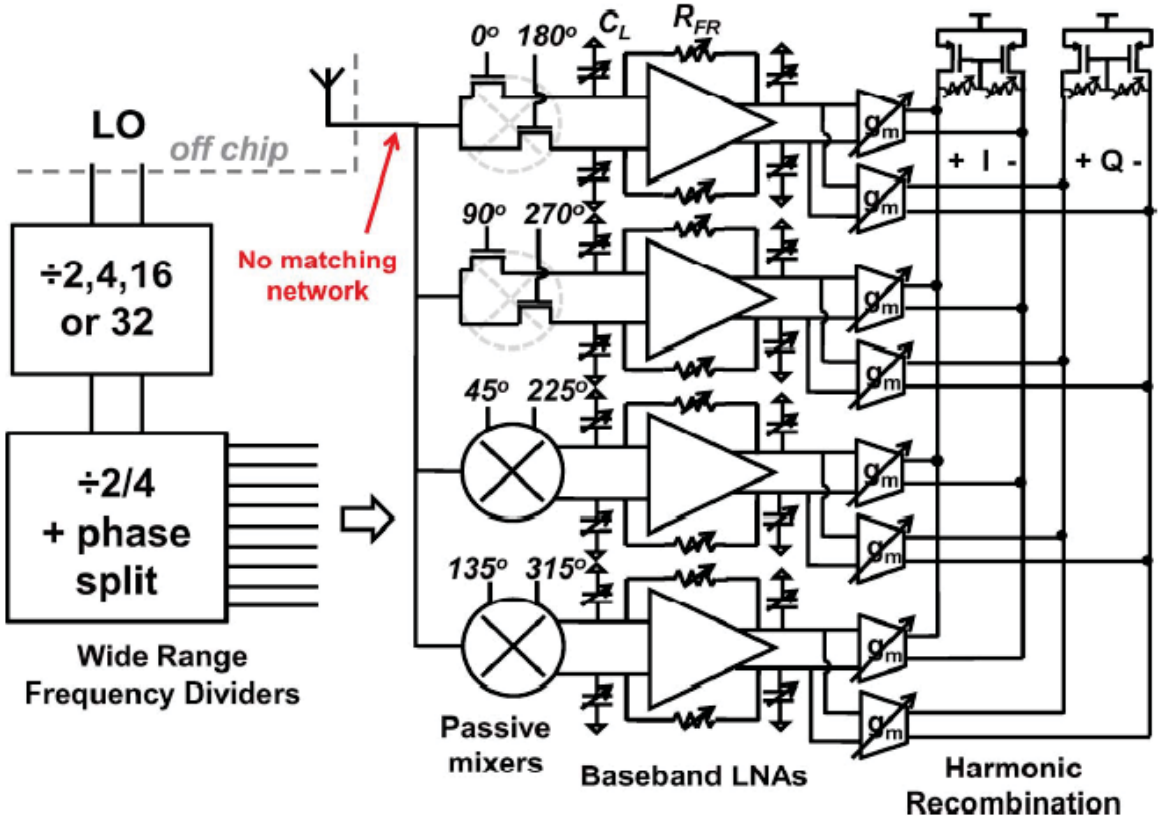
	[13]	[14]	[15]	[16]	[17]	[18]	[20]	[21]	[22]
Improved linearity	✓	✓	✓ ✓	✓ ✓	X	✓	X	✓ ✓	X
Reduced 1/f noise	X	X	X	X	X	X	X	X	X
Improved NF	✓ ✓	✓	✓ ✓	✓	✓	✓	X	✓	✓
Low Power consumption	✓	✓	X	✓ ✓	✓	✓	X	✓	X
Improved selectivity	X	X	X	X	✓ ✓	✓ ✓	✓ ✓	✓ ✓	X
Improved out-of-band rejection	X	X	X	✓	✓ ✓	✓✓	✓ ✓	✓	X

4 DEVELOPMENT AND IMPLEMENTATION OF THE N-PATH MIXER-1ST ARCHITECTURE

4.1 TOPOLOGY OF THE N-PATH MIXER-1ST ARCHITECTURE

The topology used in this work is based on [3]. Figure 4.1 presents the architecture developed in [3], it is an N-Path mixer-1st that can operate in 4-Path and 8-Path mode. The signal is amplified in baseband, and the impedance matching is achieved with the feedback loop in the baseband amplifiers. In this work, there will be a focus only on the 4-path operation. Figure 4.2 shows the clock strategy ($f_s = 1\ GHz$ example).

Figure 4.1: N-Path mixer-1st schematic

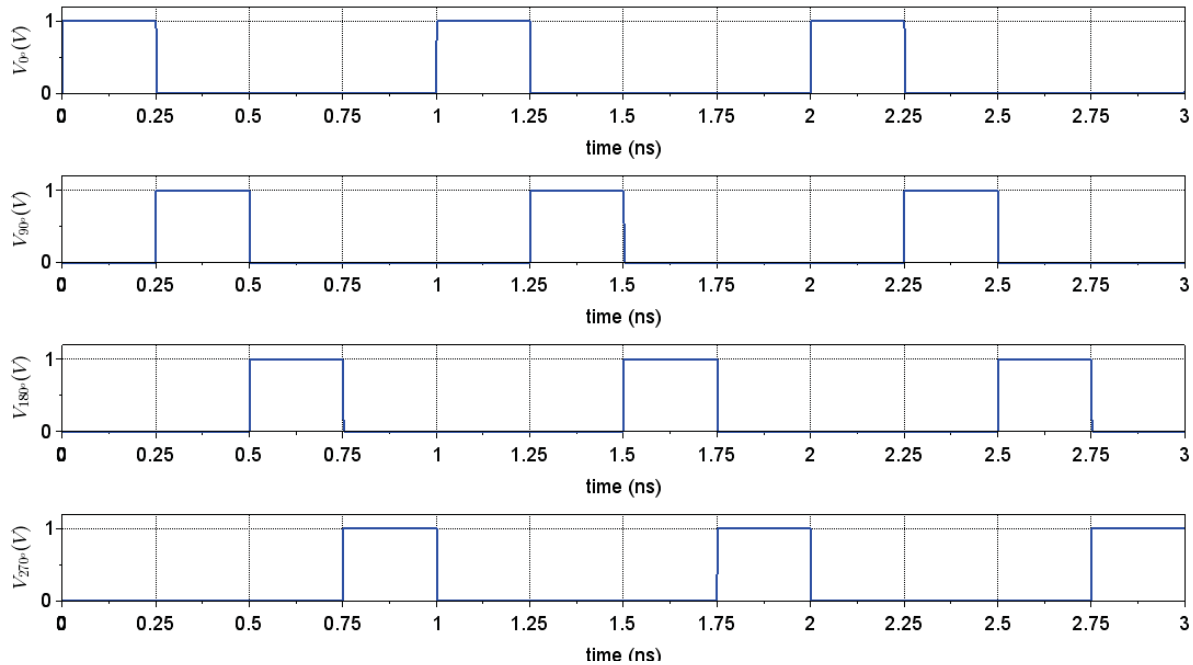


Source:[3]

This work takes the idea presented in [3] of a tunable impedance matching and uses it to center the input impedance in a new intermediate frequency, f_{IF}, to achieve a low-IF receiver. In [3] the impedance is tuned in the switching frequency.

It is desired that f_{IF} and the bandwidth are variable. Hence variable resistors and capacitors are also implemented. Deriving out an LTI (linear time-invariant) model presented in

Figure 4.2: Clock strategy for 4-path operation



Source:the author

[3] analytical equations are deduced in this work. The values of resistors and capacitors for f_{IF} and bandwidths will be obtained from those equations.

Figure 4.3 presents a block diagram of the architecture. The first block is an N-Path filter, in which four squared voltage signals with approximately 25 % duty cycle that never overlap feed the architecture. The input signal is a power source in RF frequency. The output is four signals in baseband that can be processed as quadrature and in-phase. In this block, a capacitor C_L can be controlled, and with it, the bandwidth of the system is controlled. System's parameters are also present in this block: R_{sw} is the switches' resistance, γ is a constant, and R_{in2} is an input impedance value that will provide the bandwidth.

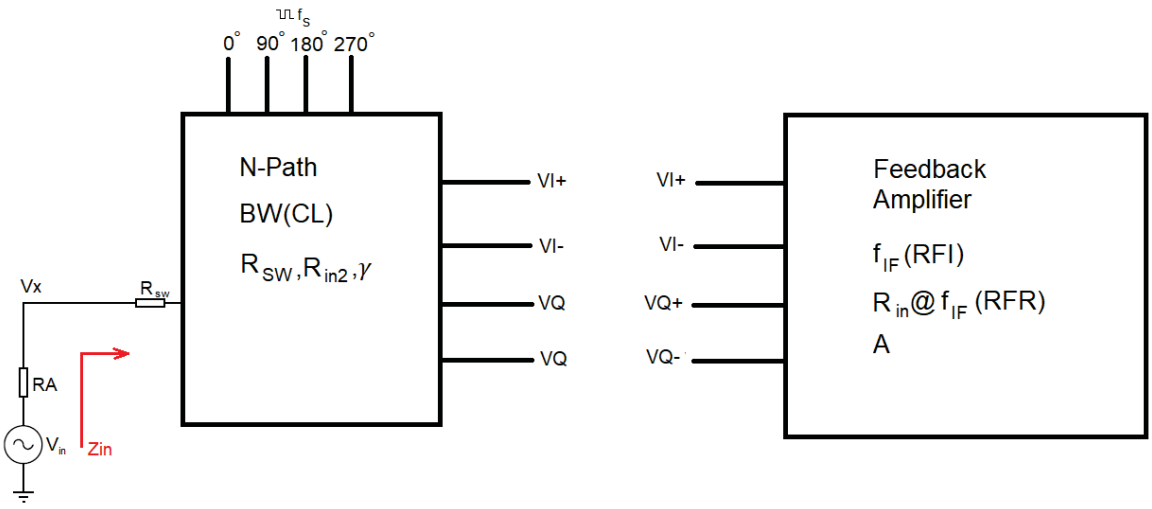
The second block is the feedback amplifiers, in which the outputs of the first block are inserted. In this block, $VI+$, $VI-$, $VQ+$, and $VQ-$ are fed back. Hence in the second block, the outputs and the inputs are the same. The resistors R_{FR} and R_{FI} are controlled. Although R_{FR} interferes, R_{FI} mostly controls f_{IF} and R_{FR} mainly controls the input resistance at f_{IF} ($R_{in}@f_{IF}$). The system's parameter in this block is the voltage gain, A.

4.2 IMPEDANCE ANALYSIS

To understand the impedance in this architecture first is helpful to observe a simplified 4-Path (like the one shown in figure 2.3) with a resistor, R_B, representing the load. This simplified model is presented in figure 4.4.

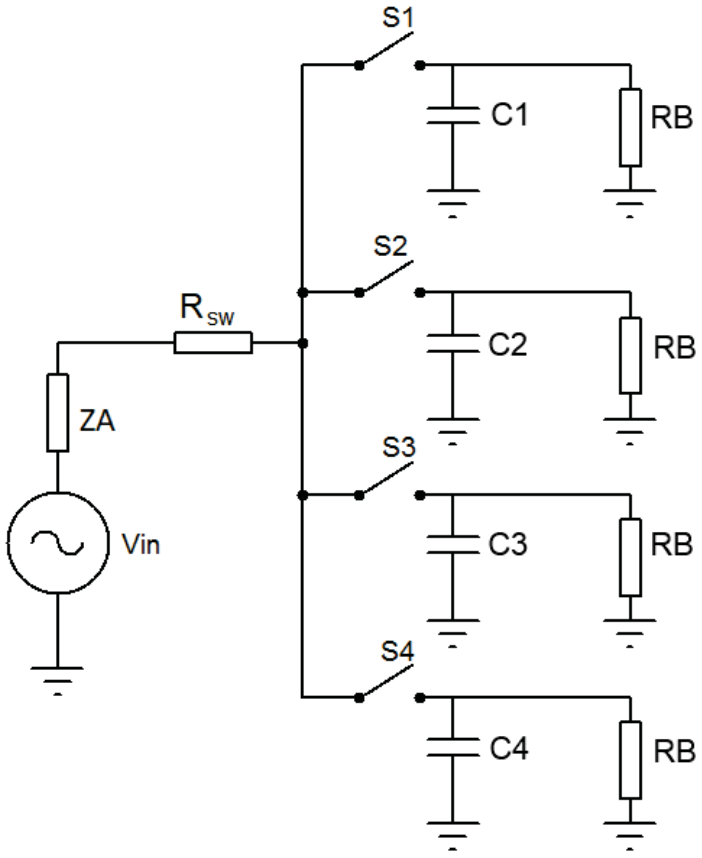
A LTI analysis for the circuit presented in 4.4 was conducted in [1]. The LTI model is only valid for $f_{in} = f_s$. Because the capacitor's voltage will present a frequency equal to

Figure 4.3: Block diagram of the architecture presented in this work



Source:the author

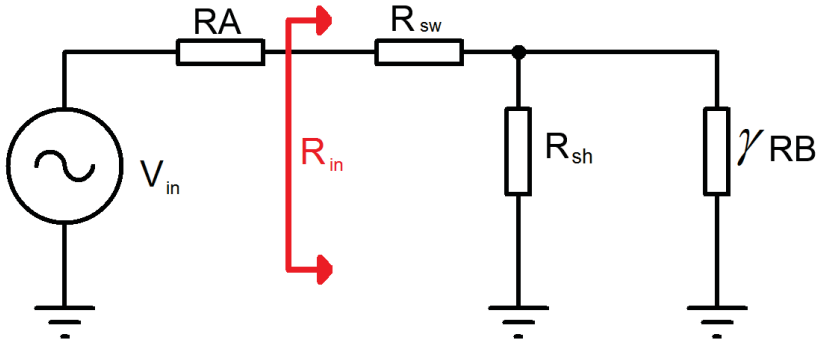
Figure 4.4: Simplified model of the N-Path mixer-1st architecture



Source:the author

$f_{in} - f_s$, and when both frequencies are equal, the capacitor becomes an open circuit. The model is presented in figure 4.5. It is possible to observe that the input resistance (R_{in}) can be altered when R_B is altered.

Figure 4.5: LTI circuit for the N-Path mixer-1st



Source:the author

In figure 4.5, V_{in} is the input voltage, R_A the antenna resistance and the input resistance is defined as:

$$R_{in} = R_{sw} + \gamma R_B || R_{sh}, \tag{4.1}$$

where R_{sw} is the switch resistance, R_{sh} is defined as the shunt resistance:

$$R_{sh} = \frac{4\gamma}{1 - 4\gamma}(R_{sw} + R_A), \tag{4.2}$$

and γ is

$$\gamma = \frac{2}{\pi^2}. \tag{4.3}$$

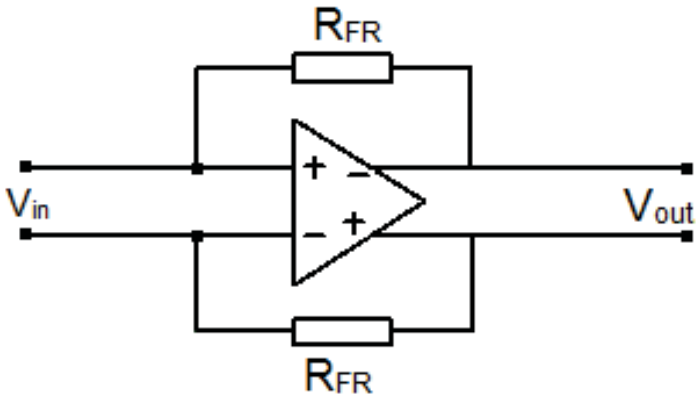
It is desired to amplify the signal from each of the capacitors, so the load R_B is exchanged for a baseband amplifier with a feedback loop, as shown in figure 4.6. The resistor R_B in figure 4.5 will be represented by the amplifier's input impedance ($R_{in,amp}$). And $R_{in,amp}$ can be defined as:

$$R_B = R_{in,amp} = \frac{R_{FR}}{1 + A}, \tag{4.4}$$

hence the input resistance of the amplifier can be controlled by altering R_{FR}, and the input resistance of the N-Path mixer-1st can be controlled by altering the input resistance of the amplifier.

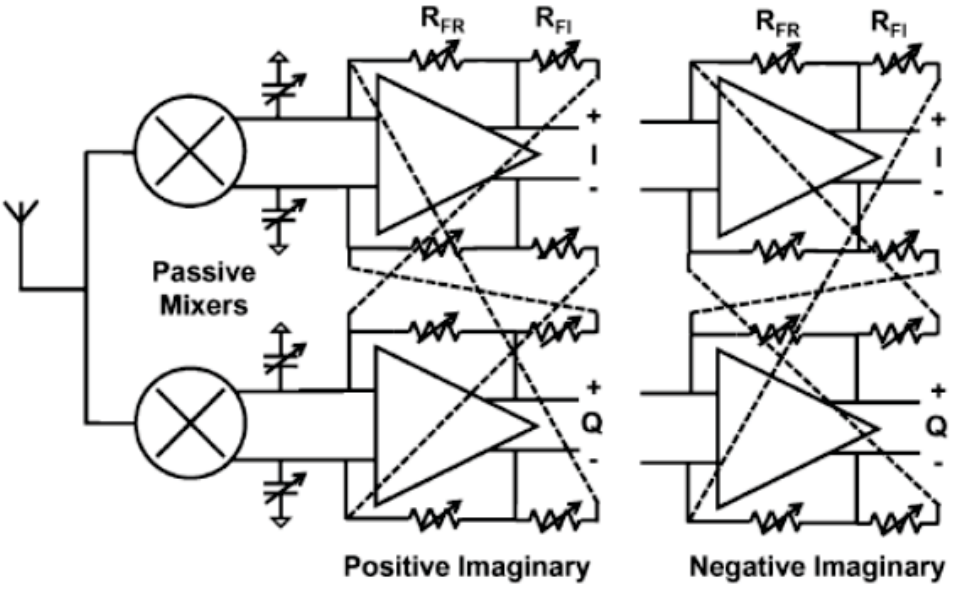
However, as it can be seen in equation 4.1, the input resistance can only assume real values. With this topology is not possible to match an imaginary impedance in the antenna (Z_A) without adding extra inductors and capacitors. Those components are avoided because of the surface occupied by those components; a tunable impedance matching is desired. Therefore, the solution presented in [3] is a complex feedback that takes the output of one amplifier and puts it in the input of the other, as shown in figure 4.7.

Figure 4.6: Schematic of the amplifier with feedback



Source:the author

Figure 4.7: Schematic of the complex feedback



Source:[3]

Figure 4.7 presents two feedback loops: positive imaginary (that will give a positive value in the input reactance) and negative imaginary (that will give a negative value in the input reactance). The value of the Z_B impedance is given as [3] (only for $f_s = f_{in}$):

$$Z_B = \left[\left(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}\right) \pm j\frac{A}{R_{FI}}\right]^{-1}, \tag{4.5}$$

this changes the input resistance from equation 4.1 to an input impedance:

$$Z_{in} = R_{sw} + \gamma Z_B || R_{sh}. \tag{4.6}$$

4.3 COMPLEX INPUT IMPEDANCE N-PATH MIXER-1ST ANALYTIC EQUATION DEDUCTION

This work aims to take the LTI model presented in [3], only valid for $f_{in} = f_s$, and deduce equations valid in the whole spectrum. The equation presented in 4.5 represents the load impedance, but only in f_s. In order to obtain the impedance value throughout the whole frequency spectrum, it is necessary to consider the impedance of the capacitor from each one of the paths in parallel with the Z_B impedance. Hence a new impedance, $Z_B^{'}$, is defined:

$$Z_B^{'}(\omega) = Z_B||(j\omega C_L)^{-1}. \tag{4.7}$$

ω in this case is the baseband frequency, that is $2\pi|f_{in} - f_s|$. Replacing 4.5 in 4.7:

$$Z_B^{'}(\omega) = \left[\left(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}\right) \pm j\frac{A}{R_{FI}}\right]^{-1} ||(j\omega C_L)^{-1}. \tag{4.8}$$

Manipulating equation 4.8:

$$Z_B^{'}(\omega) = \frac{j\omega C_L}{1 + j\omega_{IF} C_L \left[\left(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}\right) \pm j\frac{A}{R_{FI}}\right]}. \tag{4.9}$$

From figure 4.5 (having in mind that R_A is replaced by Z_A, and R_B is replaced by $Z_B^{'}$):

$$Z_{in}(\omega) = R_{sw} + \gamma Z_B^{'}(\omega)||R_{sh}, \tag{4.10}$$

replacing 4.2 and 4.9 in 4.10:

$$Z_{in}(\omega) = R_{sw} + \frac{4\gamma(R_{sw} + R_A)}{\left[(1-4\gamma) + 4(R_{sw} + R_A)\left(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}\right)\right] + j\left[4(R_{sw} + R_A)\left(\omega C_L + \frac{A}{R_{FI}}\right)\right]}. \tag{4.11}$$

In order to achieve a equation in the form of $a + b \cdot i = c + d \cdot i$, equation 4.11 is manipulated:

$$\frac{Z_{in}(\omega) - R_{sw}}{4\gamma(R_{sw} + R_A)} = \frac{\left[(1-4\gamma) + 4(R_{sw} + R_A)(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}})\right] - j\left[4(R_{sw} + R_A)\left(\omega C_L + \frac{A}{R_{FI}}\right)\right]}{\left[(1-4\gamma) + 4(R_{sw} + R_A)\left(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}\right)\right]^2 + \left[4(R_{sw} + R_A)\left(\omega C_L + \frac{A}{R_{FI}}\right)\right]^2}, \tag{4.12}$$

this way, an equation that describes the behavior of the input impedance throughout the whole frequency spectrum is obtained. C_L, R_{FI} and R_{FR} will be obtained, equalizing the real part of the left-hand side with the real part of the right-hand side, and the same for the imaginary part.

It can be observed in equation 4.12 that three variables can be set in the project (C_L, R_{FI} and R_{FR}). Hence, three points in the frequency spectrum can be set. The first two will be used in the impedance matching (Z_{in}) for f_{IF} (this will be the best impedance matching). Two

points are used because there are a real and an imaginary part. The last point (R_{in2}) will be used to set the real part of another frequency, defining the bandwidth.

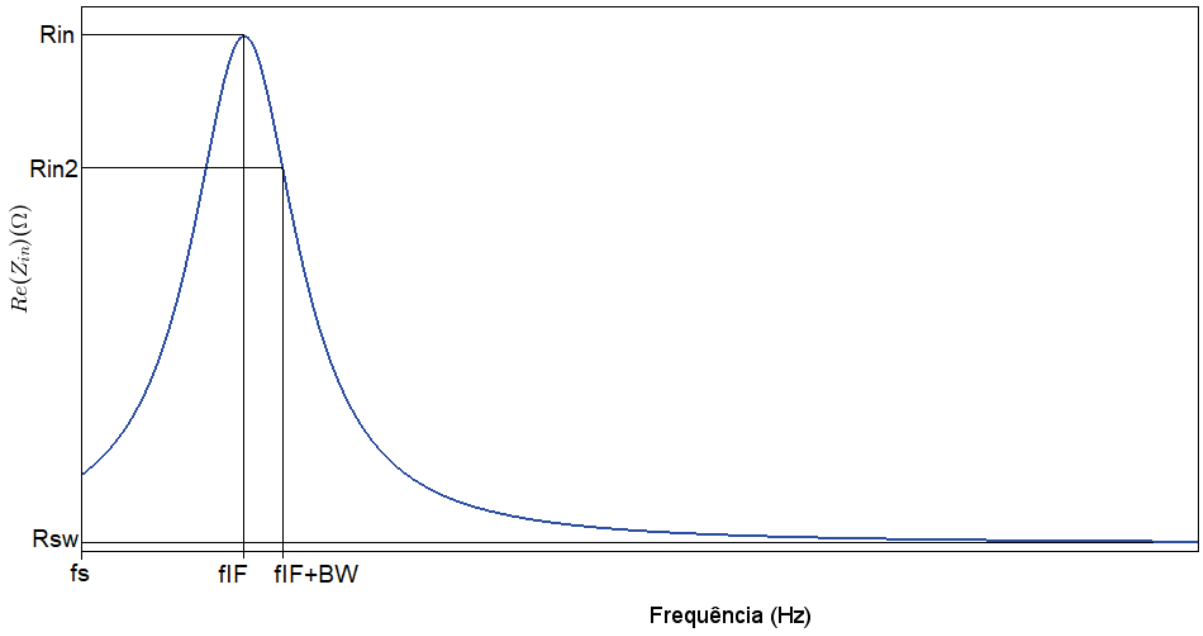
4.4 PROJECT SPECIFICATIONS

Before showing how the topologies for reconfigurable components are implemented, this section aims to present the specifications for which the architecture will operate. Table 4.1 shows all the bandwidths, f_s, and f_{IF} in which the system operates. Figure 4.8 shows qualitatively each of the frequencies presented in table 4.1. The input impedance is centered around the f_s. The best input impedance matching is in f_{IF}. The difference between f_{IF} and a second frequency (whose input impedance matching is R_{in2}) is the bandwidth.

Table 4.1: Bandwidths, central frequencies and intermediate frequencies

f_s	BW	f_{IF1}	f_{IF2}	f_{IF3}	f_{IF4}
1 GHz	1.25 MHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
1 GHz	2.5 MHz	2.5 MHz	5 MHz	10 MHz	
1 GHz	5 MHz	5 MHz	10 MHz		
1 GHz	10 MHz	10 MHz			
2 GHz	1.25 MHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
2 GHz	2.5 MHz	2.5 MHz	5 MHz	10 MHz	
2 GHz	5 MHz	5 MHz	10 MHz		
2 GHz	10 MHz	10 MHz			

Figure 4.8: Qualitative representation of the frequencies used in the project



Source: the author

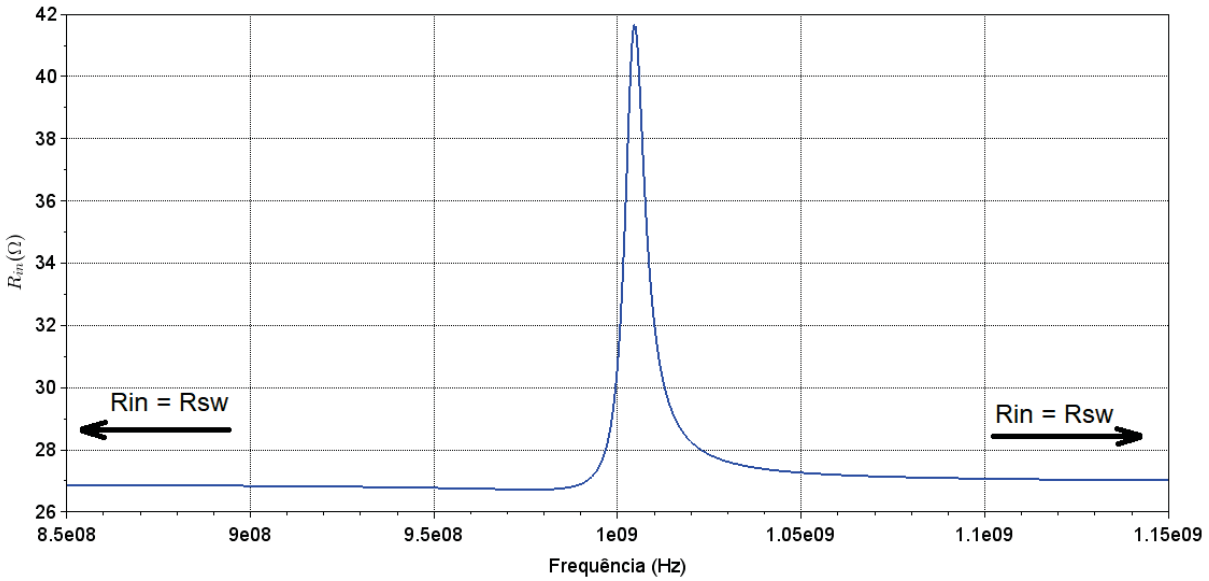
4.4.1 Obtaining the secondary parameters

Before continuing with the project specifications, it is essential to obtain some parameters for the equations presented in section 4.3.

4.4.1.1 Obtaining R_{sw}

The switch resistance, R_{sw}, will be obtained using the PSP simulation. In this simulation, R_{sw} is achieved in an operation closer to reality (switching the filter with an AC input). R_{sw} will not only be dependent on the N-Path filter switch but also on the switches that will do the capacitance variation operation. Hence it will be possible to reach an "effective R_{sw}." PSP simulation can provide the input resistance of the whole architecture. As it can be seen in equation 4.11 the more ω_{IF} increases (gets further away from the 50 Ω frequency), the closer Z_{in} gets to R_{sw}. This can also be observed in figure 4.4, for high frequencies, the capacitor C_L presents low impedance. Therefore R_B becomes negligible, and R_{sw} prevails. Hence R_{sw} can be obtained by looking at the R_{in} graph (obtained with the real part of the $Z11$ parameter from the PSP simulation) in a frequency far enough from f_{IF}, where the aimed resistance is 50 Ω, shown in figure 4.9. This figure is an example of the input resistance obtained from the architecture. f_s is 1 GHz, f_{IF} is 5 MHz, and the bandwidth 5MHz. This curve will be discussed in greater detail in chapter 5. For now, the main focus of this curve is to show how to obtain R_{sw} from a frequency far from f_s.

Figure 4.9: Obtaining R_{sw} from the input resistance (R_{11}) graph



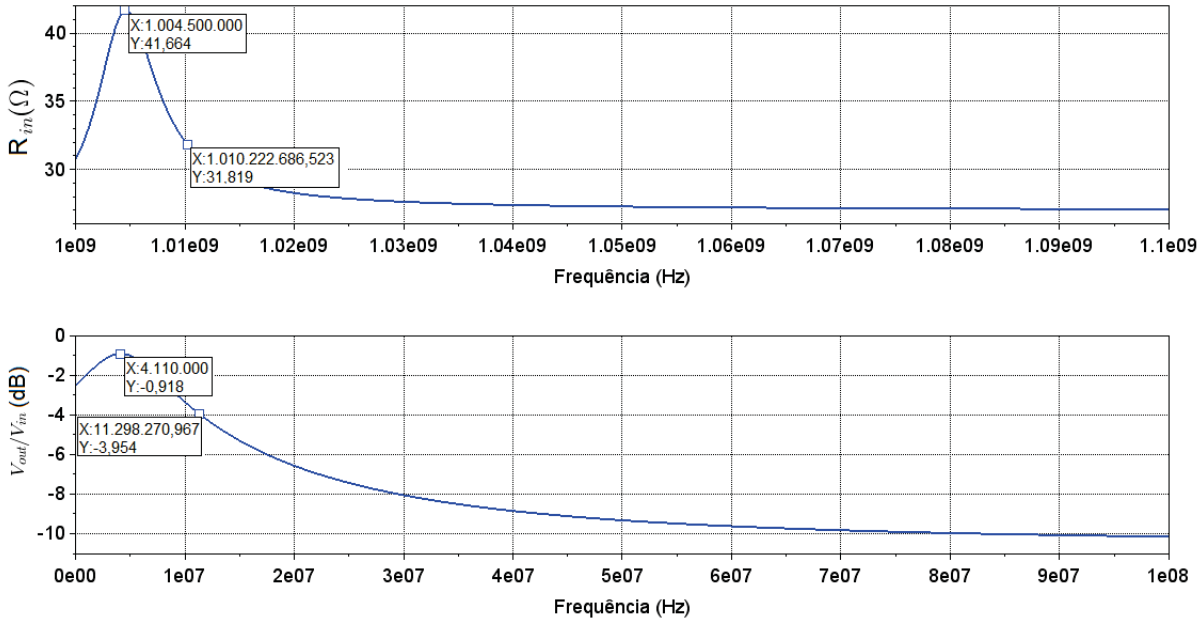
Source: the author

4.4.1.2 R_{in2} selection

As mentioned in subsection 4.4.2, it is possible to choose two frequencies and assign different impedance values to both of them. The first frequency will be the f_{IF}, and the selection of the impedance for this frequency is straightforward: $Z_{in} = 50 + j \cdot 0\ \Omega$, as the best impedance matching is desired for this frequency. The selection of the impedance of the second frequency, Z_{in2}, is not so obvious. As mentioned before, the second frequency will be related to the system's bandwidth. As seen in section 4.4.2, two variables are used to set the real part and imaginary part of the input impedance for f_{IF}. Only one variable is left for Z_{in2}. Hence, only the real part of Z_{in2} will be set, represented as R_{in2}.

Bandwidth is when the maximal signal's amplitude decays to half of its more significant value ($-3\ dB$), so the frequency to which the output signal falls to half of its larger amplitude is observed, and the input resistance for this frequency is taken; this resistance will be R_{in2}. This can be done because if the baseband amplifier is wideband enough, the bandwidth of the signal is defined only by the N-Path filter, and it can be described as the LTI model presented in figure 4.5. It is important to clarify that any value between R_{sw} and $Re(Z_{in})$ can be chosen for R_{in2}, the technique presented for R_{in2} selection is just a methodology for this architecture. This operation is shown in figure 4.10, for $f_{IF} = 5$ MHz and $f_{-3dB} = 10$ MHz. The input impedance graph is centered around f_s (in this case, $f_s = 1$ GHz), and the voltage gain is centered around 0 Hz. Those graphs will be discussed in further detail in chapter 5.

Figure 4.10: Frequency selection for R_{in2}

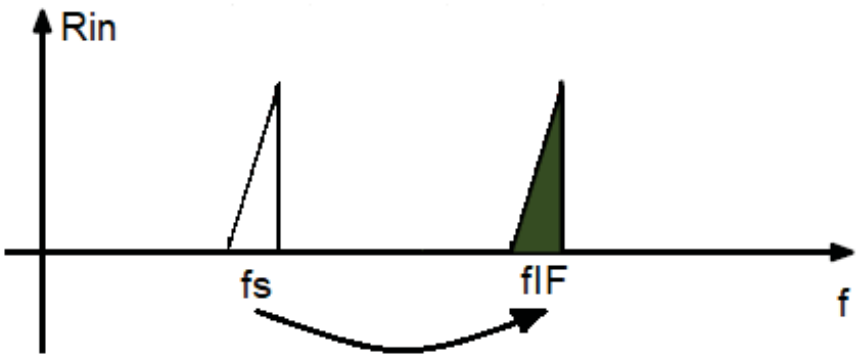


Source: the author

4.4.2 Selection of C_L, R_{FR} and R_{FI}

Looking at equation 4.12 it is possible to notice that three components can be altered: C_L, R_{FR}, R_{FI}. The work presented in [3] is centered around f_s. In this work a new central frequency is chosen. This new central frequency will be the f_{IF} of the low-IF architecture [7]. f_{IF} will be a shift in the architecture's input resistance, concerning the previous central frequency, defined as f_s. Figure 4.11 represents the shift in the input resistance of the architecture.

Figure 4.11: Shift from f_s (previous central frequency) to f_{IF} (new central frequency)



Source: the author

f_{IF} will present the best impedance matching. In equation 4.12 f_{IF} is a configurable project parameter. Thus it is possible to shift the impedance matching of the architecture to any frequency. To this frequency, the impedance $Z_{in} = R_{in} + j \cdot 0\Omega$ is assigned, in most of the cases R_{in} will be 50Ω. Hence for ω_{IF} (angular representation of f_{IF}), two parameters are defined: $Re(Z_{in})$ and $Im(Z_{in})$. Thus, two of the project components will be used.

Taking the imaginary part for equation 4.12:

$$\frac{-\left[4(R_{sw}+R_A)\left(\omega_{IF}C_L+\frac{A}{R_{FI}}\right)\right]}{\left[(1-4\gamma)+4(R_{sw}+R_A)\left(\frac{1+A}{R_{FR}}+\frac{1}{R_{FI}}\right)\right]^2+\left[4(R_{sw}+R_A)\left(\omega_{IF}C_L+\frac{A}{R_{FI}}\right)\right]^2}=0, \tag{4.13}$$

it is possible to notice that equation 4.13 will be zero when the numerator is zero and the denominator is non-zero. The denominator will never be zero because γ, R_{sw}, R_A, A, R_{FR} and R_{FI} are all positives. Thus the denominator will always be positive. Hence:

$$4(R_{sw}+R_A)\left(\omega_{IF}C_L+\frac{A}{R_{FI}}\right)=0, \tag{4.14}$$

so:

$$R_{FI}=\frac{-A}{\omega_{IF}C_L}. \tag{4.15}$$

ω_{IF} can be negative and, in this case, must be negative. If ω_{IF} was positive, the complex feedback topology should be changed (as shown in figure 4.7).

Now looking at the real part:

$$\frac{\left[(1-4\gamma)+4(R_{sw}+R_A)\left(\frac{1+A}{R_{FR}}+\frac{1}{R_{FI}}\right)\right]}{\left[(1-4\gamma)+4(R_{sw}+R_A)\left(\frac{1+A}{R_{FR}}+\frac{1}{R_{FI}}\right)\right]^2+\left[4(R_{sw}+R_A)\left(\omega_{IF}C_L+\frac{A}{R_{FI}}\right)\right]^2}=\frac{Re(Z_{in})-R_{sw}}{4\gamma(R_{sw}+R_A)}, \tag{4.16}$$

using

$$Re(Z_{in})=R_{in}, \tag{4.17}$$

$$R_{FI}=-\frac{A}{\omega_{IF}C_L} \tag{4.18}$$

and isolating R_{FR}:

$$R_{FR}=(1+A)\left[\frac{\frac{4\gamma(R_{sw}+R_A)}{R_{in}-R_{sw}}-(1-4\gamma)}{4(R_{sw}+R_A)}+\frac{\omega_{IF}C_L}{A}\right]^{-1}. \tag{4.19}$$

One can observe that in both 4.18 and 4.19, the parameters depend on C_L, which is not yet defined nor will be arbitrary. Hence a second frequency value can be chosen, and the real part of the impedance (Z_{in2}) can be set in this frequency. Herewith, it is possible to control the bandwidth of the architecture. Thus looking at the real part of the input impedance for a second frequency value, $\omega_{IF}^{'}=\omega_{IF}+2\pi BW$, for which a second value of the real part of the input impedance will be set, $Re(Z_{in2})=R_{in2}$:

$$\frac{\left[(1-4\gamma)+4(R_{sw}+R_A)\left(\frac{1+A}{R_{FR}}+\frac{1}{R_{FI}}\right)\right]}{\left[(1-4\gamma)+4(R_{sw}+R_A)\left(\frac{1+A}{R_{FR}}+\frac{1}{R_{FI}}\right)\right]^2+\left[4(R_{sw}+R_A)\left((\omega_{IF}+2\pi BW)C_L+\frac{A}{R_{FI}}\right)\right]^2}=\frac{R_{in2}-R_{sw}}{4\gamma(R_{sw}+R_A)}, \tag{4.20}$$

replacing 4.18 and 4.19 in 4.20:

$$C_L=\frac{\gamma\sqrt{\frac{1}{(R_{in2}-R_{sw})(R_{in}-R_{sw})}-\frac{1}{(R_{in}-R_{sw})^2}}}{2\pi BW}. \tag{4.21}$$

The process for calculating the components C_L, R_{FR} and R_{FI} start with the systems parameters for this architecture shown in table 4.2. The project starts with choosing f_s, bandwidth, and f_{IF} with those parameters. Once the parameter of the project and the system's parameters are known, C_L is calculated with equation 4.21. With C_L, equation 4.18 is used to calculate R_{FI}. The last parameter, R_{FR}, is obtained with equation 4.19.

Table 4.2: System's parameters

R_{sw}	26 Ω
R_A	50 Ω
γ	$\frac{2}{\pi^2}$
A	100
R_{in2}	32 Ω

4.5 TOPOLOGIES FOR RECONFIGURABLE RESISTORS AND CAPACITORS

The variable components used in this work are mainly controlled by switches that turn branches on and off. Each one of the components has its particularities.

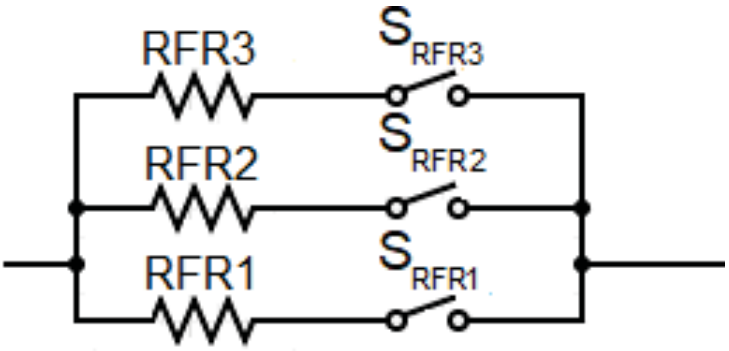
4.5.1 Variable resistor

4.5.1.1 R_{FR}

The R_{FR} component is the one whose value is the least variable, it does not depend on the bandwidth, and it depends very little on f_{IF}. In equation 4.19 $\frac{\frac{4\gamma(R_{sw}+R_A)}{R_{in}-R_{sw}}-(1-4\gamma)}{4(R_{sw}+R_A)}$, independent of the f_{IF}, is much larger than $\frac{\omega_{IF}C_L}{A}$, dependent of f_{IF}. Thus the component R_{FR} varies very little with changes in f_{IF}. Due to its small variability, only three values were chosen, and the architecture is presented in figure 4.12. It is a topology that turns branches of resistors on and off, where each branch is better adapted for each operation mode.

The switches used for this topology aim to have very low parasitic capacitances, even if it degrades R_{sw}. Because in comparison with the values of the resistors, R_{sw} is much smaller. At the same time, a large parasitic capacitance can interfere with the N-Path filter's behavior because this switch will be connected to the output capacitor. The switch was implemented with an NMOS (N-type metal-oxide-semiconductor field-effect transistors) in 28 nm technology. The transistor presents one finger with 20 μm width and 30 nm length.

Figure 4.12: Architecture of the variable R_{FR}



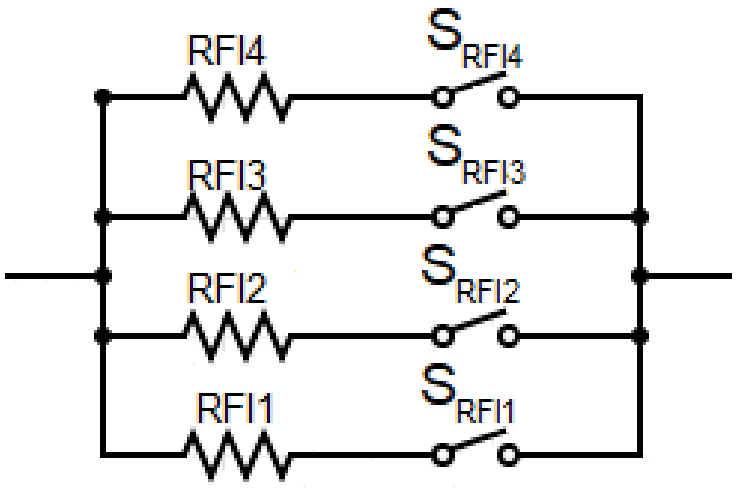
Source: the author

4.5.1.2 R_{FI}

The architecture used for R_{FI} is very similar to the one used with R_{FR}. Different from equation 4.19, that defines R_{FR}, equation 4.18 depends mainly on f_{IF} and also depends on the bandwidth (because it depends on C_L). Hence R_{FI} changes a lot with the f_{IF}. Due to its broad range, four branches are implemented, each one to a specific f_{IF}. Multiple branches can be turned on if there is some mismatch in the nominal values of the resistor. The schematic is presented in figure 4.13.

Similarly to R_{FR}, and for the same reasons, the switch used for this topology also aims to have a low capacitance. Hence the same switch used for R_{FR} is used for R_{FI}.

Figure 4.13: Architecture of the variable R_{FI}



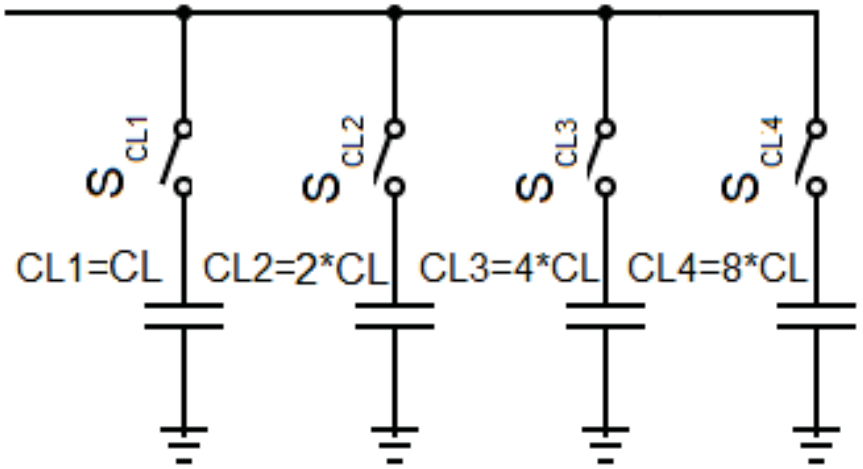
Source: the author

4.5.2 Variable CL

The architecture used for C_L is similar to the previous ones, but some parameters need to be carefully examined. It will also be an architecture in which branches will be turned on and off, but the switches will need to present a low R_{sw}, even if it affects the capacitance. This happens because this is where the sample will be stored and be connected to the amplifier. Furthermore, the theoretical model of the N-Path filter does not take into account a resistor in series with the capacitor in the amplifier's input. Hence having a resistance, even if it is small, can cause significant mismatches in the architecture's response. However, the switch capacitance does not need to be as low as the previous one. Because it will not switch very fast, and having a capacitance in the input of the amplifier is already predicted by the theoretical model (as long as it does not change the predicted capacitance a lot). The schematic of the variable capacitor is presented in figure 4.14.

The switch was implemented with an NMOS transistor in 28 nm technology that presents 32 fingers with 35 μm width and 30 nm length each.

Figure 4.14: Architecture of the variable C_L



Source: the author

4.6 COMPLETE ARCHITECTURE IMPLEMENTATION

The complete circuit topology is presented at figure 4.15. The N-Path filter from figure 4.4 has its resistors exchanged by the complex feedback amplifiers presented in figure 4.7. The variable resistor and capacitors presented in figure 4.14, 4.12 and 4.13 are implemented instead of C_L, R_{FR} and R_{FI}, respectively. The resistors, used in R_{FR} and R_{FI}, and the capacitor, used in C_L, are implemented from the 28 nm technology.

The N-Path's switches, driven by f_s, were implemented with NMOS transistors that aim to have low R_{sw} and low capacitance. The low R_{sw} is because it is desired that most of the voltage is in the capacitor. At the same time, the low capacitance is because it switches with a frequency in the GHz order. Therefore, an NMOS switch was implemented in the 28 nm technology with one finger with 20 μm width and 30 nm length to balance those parameters.

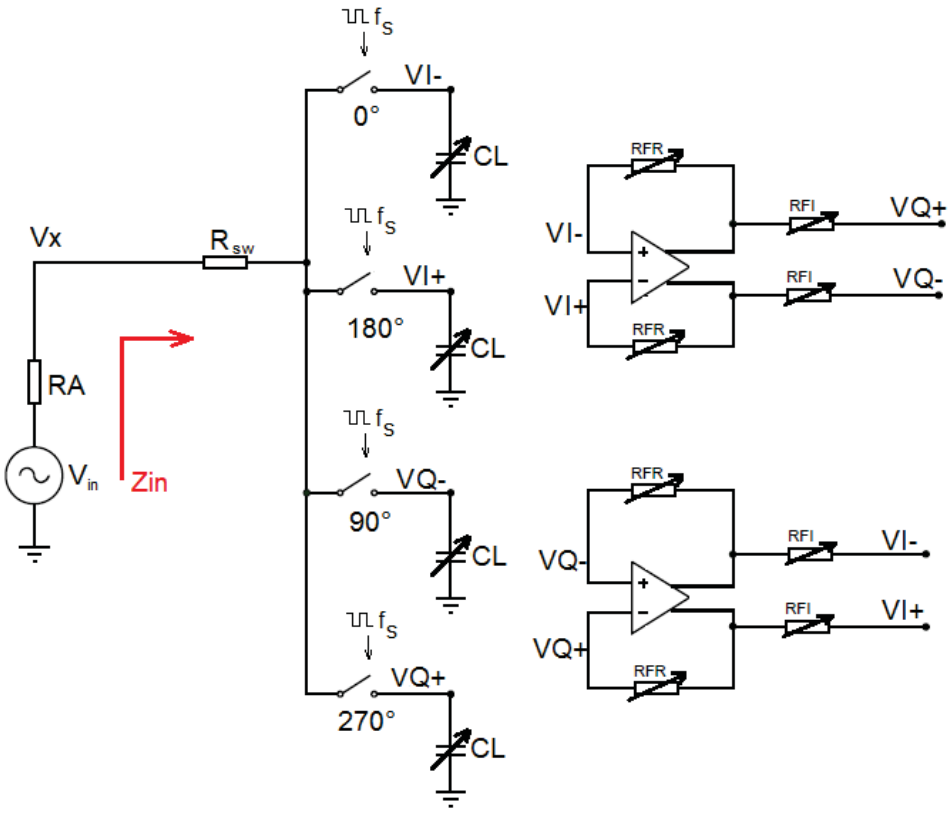
The amplifier is the only component not to be implemented at the circuit level. An ideal voltage-controlled voltage source is used instead. The square waves are implemented with an ideal voltage pulse source. In each pulse source, a delay is implemented to close one switch at a time. The square wave presents a duty cycle of approximately 25 %. The duty cycle is a bit smaller than 25 % to guarantee that two switches will never be closed simultaneously.

4.7 SIMULATION METHODS

4.7.1 Transient simulation

The transient simulation consists of a time-variant input signal, taking all the time variations into account. Therefore, the circuit response is also a function of time. However, unlike the periodic simulations, a steady-state is not necessary, so it is possible to understand the system's intrinsic behavior.

Figure 4.15: Complete architecture schematic



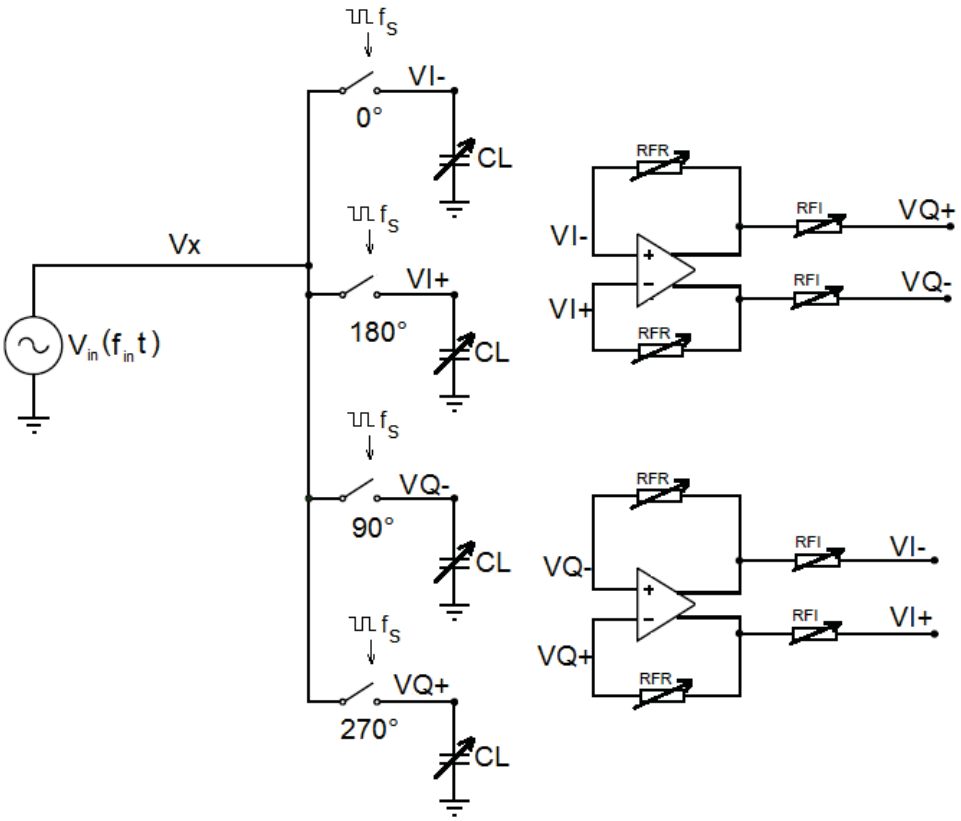
Source: the author

With the transient simulation, it will be possible to observe curves that were important to the theoretical analysis of the N-Path filter, like 2.7 and 2.8. The testbench of this simulation is presented in figure 4.16. The input is a time-varying voltage source with a fixed frequency and 1 mV amplitude. The output is taken in the V_x node. In this node, it will be possible to observe the voltage in each of the capacitors when its respective switch is on.

Two simulations will be conducted with two different frequencies. One of the frequencies will be a frequency that the filter accepts and the other one that the filter rejects. The result will be taken in the V_x node from the architecture in figure 4.15, so it will be in RF.

The main objective of this simulation is to validate the architecture qualitatively. For example, comparing the simulated curves with the theoretical curves that were key to understanding the behavior of the N-Path mixer-1st architecture. However, it is also possible to observe the rejection between an accepted frequency and a rejected frequency in this simulation. However, it is only possible to observe the rejection for two previously set frequencies. Therefore, a PAC simulation is more recommended if desired to obtain the rejection throughout the whole frequency spectrum.

Figure 4.16: Transient simulation testbench



Source: the author

4.7.2 AC simulation

AC (alternate current) simulation consists of observing the circuit's behavior for different frequency values in the input. This way, it is possible to observe how the circuit operates in the whole spectrum. A pure AC simulation can not be used in this architecture due to the time-variant nature of the system. A simulation that takes into account the time variance will be needed.

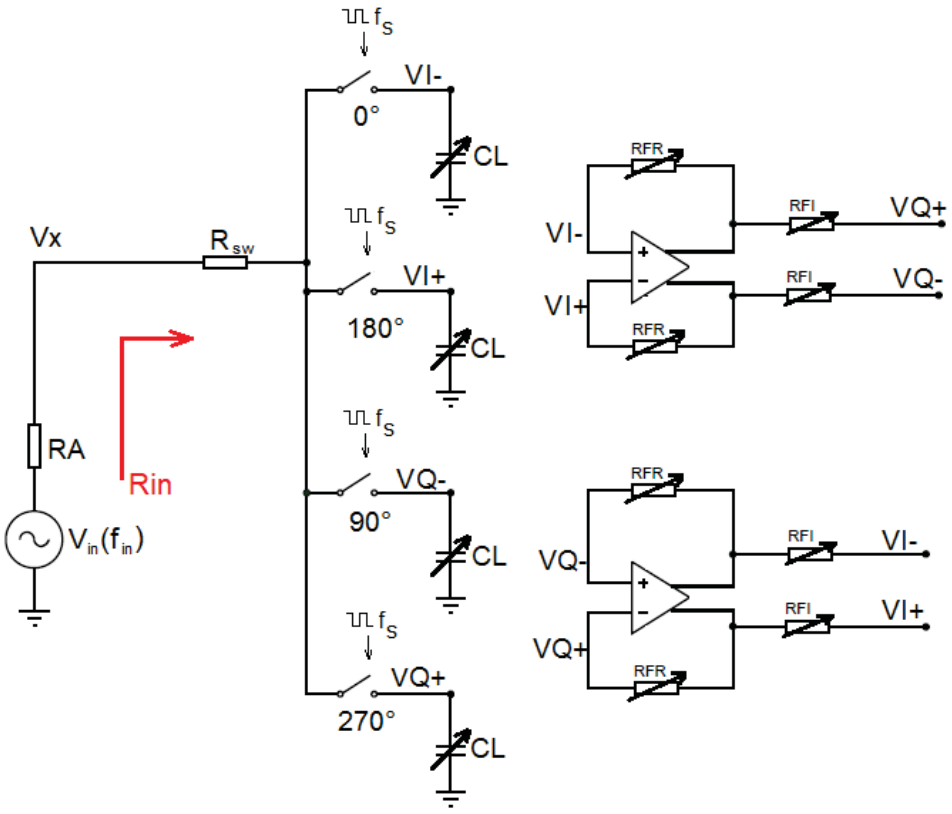
4.7.3 PSS (Periodic Steady State) simulation

The idea of a PSS simulation is to find a periodic steady-state using numerical integration until the response o the system becomes periodic [23]. Knowing the input signal frequency brings an advantage to circuits simulation, reducing the simulation time [24].

With the PSS, time-varying systems can be analyzed, and simulations similar to those operated for non-time varying systems can be operated. No result will be obtained from the PSS simulation, but this simulation is necessary to run PAC (Periodic AC) and PSP (Periodic S-Parameter) simulations.

The schematic that will be used both for the PAC and PSP simulations is presented in figure 4.17. The input is a power source of -40 dBm.

Figure 4.17: PSS simulation testbench



Source: the author

4.7.3.1 PSP simulation

PSP is an SP (S-Parameter) simulation with a PSS simulation. The PSP simulation reveals the system's S (scattering) parameters and the Z-parameters (impedance parameters) in a time-varying system. In this simulation the input impedance is provided (R_{in} in figure 4.17) with the real part of the $Z11$ Z-parameter. The input impedance is of particular interest to this work because it is the parameter for which an equation was deduced. Hence, the equation will be validated for the whole frequency spectrum.

4.7.3.2 PAC simulation

PAC simulation is an AC simulation operated with the PSS simulation. This can bring to light the system's behavior in the frequency domain in time-variant systems. Moreover, it is possible to observe the frequency behavior in multiple harmonics.

The PAC simulation will provide the whole frequency spectrum. The output voltage will be obtained between the nodes $VI+$ and $VI-$ in figure 4.17. It will be possible to observe the whole spectrum and the filter's rejection in all the frequencies. It will also be possible to observe the signal in baseband, because nodes $VI+$, $VI-$, $VQ+$ and $VQ-$, in figure 4.15, are equivalent to the nodes V_{C1}, V_{C3}, V_{C2} and V_{C4}, in figure 2.4, respectively. The voltage obtained in the PAC

simulation will also be compared to the input resistance obtained with the PSP simulation, and verifying if the resistance R_{in2} corresponds to that frequency in which the rejection is 3 dB.

5 RESULTS AND DISCUSSION

Chapter 4 derived the expressions from calculating the components for the required transfer function. Table 5.1 shows the values of bandwidth and f_{IF} that were previously calculated with those equations (as in the specifications in table 4.1). Those values only have one of each component turned on. The topologies of variable C_L, R_{FI} and R_{FR} were shown in figures 4.14, 4.13 and 4.12 respectively.

Table 5.1: Bandwidth and central frequency for C_L, R_{FI} and R_{FR}

$S_{C_{L1}}$	$S_{C_{L2}}$	$S_{C_{L3}}$	$S_{C_{L4}}$	$S_{R_{FI1}}$	$S_{R_{FI2}}$	$S_{R_{FI3}}$	$S_{R_{FI4}}$	$S_{R_{FR1}}$	$S_{R_{FR2}}$	$S_{R_{FR3}}$	BW	f_{IF}
1	0	0	0	1	0	0	0	1	0	0	1.25 MHz	1.25 MHz
1	0	0	0	0	1	0	0	1	0	0	1.25 MHz	2.5 MHz
1	0	0	0	0	0	1	0	0	1	0	1.25 MHz	5 MHz
1	0	0	0	0	0	0	1	0	0	1	1.25 MHz	10 MHz
0	1	0	0	1	0	0	0	1	0	0	2.5 MHz	2.5 MHz
0	1	0	0	0	1	0	0	1	0	0	2.5 MHz	5 MHz
0	1	0	0	0	0	1	0	0	1	0	2.5 MHz	10 MHz
0	0	1	0	1	0	0	0	1	0	0	5 MHz	5 MHz
0	0	1	0	0	1	0	0	1	0	0	5 MHz	10 MHz
0	0	0	1	1	0	0	0	1	0	0	10 MHz	10 MHz

As it can be noticed in table 5.1, the following bandwidths were aimed: 1.25 MHz, 2.5 MHz, 5 MHz, and 10 MHz. Through equation 4.21 the capacitors C_L were calculated, being directly proportional to the filters' bandwidth. Therefore, the capacitors double per bandwidth mode. Regarding the switching structure of figure 4.14, the control is done by four binary digits.

A similar process is operated for the resistors. First, R_{FI} is calculated. It is important to note that to calculate this component it is necessary to have the C_L value (see equation 4.18). So for each one of the capacitors, different values of R_{FI} are calculated for different f_{IF}. The chosen values of f_{IF} and bandwidth were shown in table 4.1.

R_{FR} is the value that changes the less, and three values were chosen to get the best impedance matching in f_{IF}. Table 5.2 shows the values of each component.

Although it is not shown in table 5.1, multiple components can be turned on at once. The capacitors can provide 15 values of bandwidth ($2^4 - 1$, because the situation where all capacitors are turned off is not used). The R_{FI} resistor can provide 16 intermediate frequencies for each bandwidth (the situation where all resistors are turned off can be used and gives f_{IF}=0). The R_{FR} resistor will only give the best impedance matching in each f_{IF}.

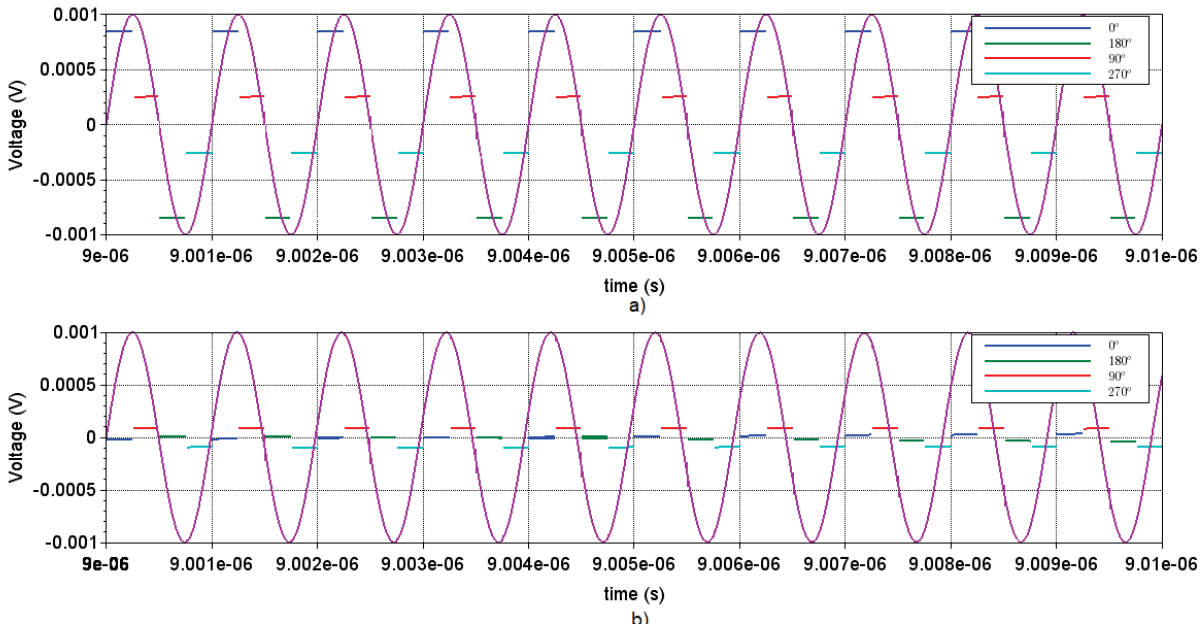
The first simulation with the circuit implementation (except for the amplifier) of the architecture will be transient. Thus, it is possible to observe the architecture behavior in the time domain (shown theoretically in figure 2.7 and 2.8). Figure 5.1 a) presents a 1GHz frequency in the input, while 5.1 b) presents a 1.01 GHz. It is possible to notice that 1 GHz is accepted by the filter, while 1.01 GHz frequency is rejected. It is also possible to observe the voltage stored in

Table 5.2: Components used in the architecture

C_{L1}	1.87 nF
C_{L2}	933 pF
C_{L3}	467 pF
C_{L4}	233 pF
R_{FR1}	20105 Ω
R_{FR2}	22040 Ω
R_{FR3}	25290 Ω
R_{FI1}	6800 Ω
R_{FI2}	3390 Ω
R_{FI3}	1690 Ω
R_{FI4}	835 Ω

each of the capacitors after many duty cycles. In this simulation, the filter presents a f_{IF} =0, f_s=1 GHz, and a bandwidth of 1.25 MHz. The rejection is about 10 dB.

Figure 5.1: Transient simulation for a a) accepted frequency and a b) rejected frequency



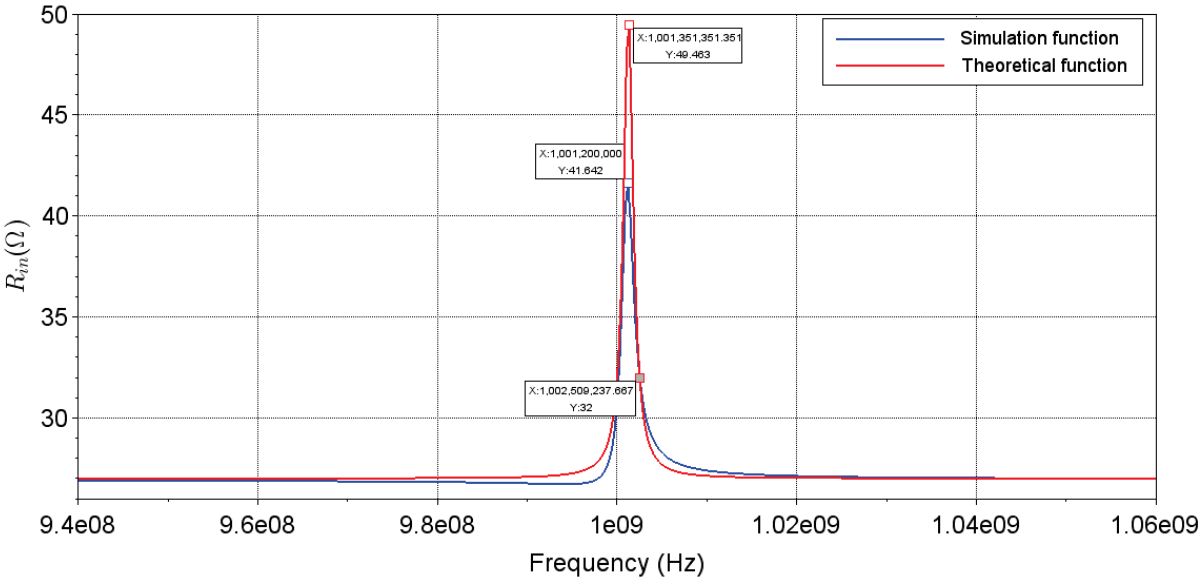
Source: the author

5.1 N-PATH EQUATIONS VALIDATION

The first test is the validation of the equations deduced in chapter 4. In each simulation, two situations are taken into account: one with the circuit level architecture and the other with the theoretical equations. The first simulation takes the minimal bandwidth and the minimal intermediate frequency, and it is presented in figure 5.2. The second simulation takes the opposite case, with the maximum bandwidth and maximum f_{IF}, and it is presented in figure 5.3. It is possible to observe that both the curves have approximately the same behavior. When the

frequency gets further away from f_{IF}, both curves tend to have the same value (R_{sw}). The point that was chosen as R_{in2}, 32 Ω in this case, is the same in both curves. In f_{IF} lies the largest mismatch, but, as expected, the frequency presents the best impedance matching in both curves. Those mismatches are mainly because real technology components have imperfections, such as parasitic resistances and capacitances. The parasitic resistance of the switch from the variable C_L has the biggest impact. Bandwidth and f_{IF} values are as expected in calculations. In both tests, no fine-tuning was made because the main focus of those simulations is to show the viability of the equations.

Figure 5.2: Input resistance for 1.25 MHz bandwidth and 1.25 MHz f_{IF}



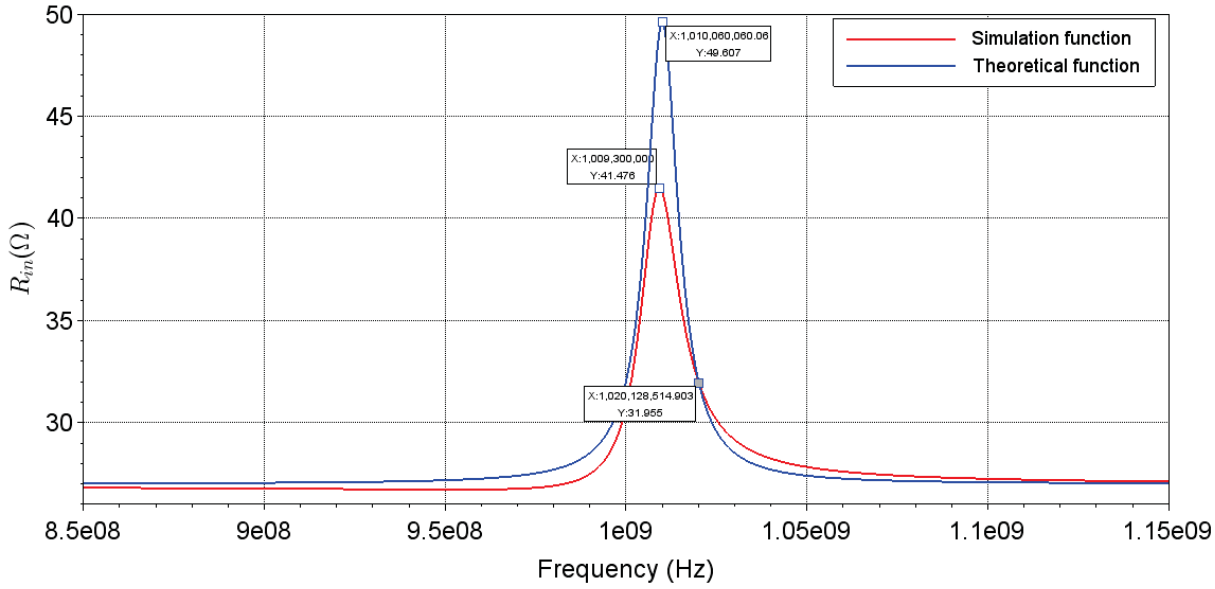
Source: the author

5.2 N-PATH MIXER-1ST PAC AND R_{IN} VALIDATION

Once the equations are validated, the aim is to validate the voltage gain. f_{IF} and bandwidth are observed in the PAC simulation and compared to those presented in the input resistance. Direct gain and output voltage are wanted in a filter/mixer architecture. However, the whole work is based on input impedance because this is the parameter for which equations were deduced. All the simulations in this section were conducted with the circuit level implementation of the architecture.

Figures 5.4, 5.5 and 5.6, present the architecture for the three cases: 1.25 MHz bandwidth and 1.25 MHz f_{IF}; 5 MHz bandwidth and 5 MHz f_{IF}; 10 MHz bandwidth and 10 MHz f_{IF}, respectively. All those cases present f_s of 1 GHz. The input impedance simulation shows the better impedance matching for f_{IF}, R_{in2} in the bandwidth frequency, and it is centered around f_s. The voltage gain simulation is centered around 0 Hz, this way it can validate the frequency

Figure 5.3: Input resistance for 10 MHz bandwidth and 10 MHz f_{IF}



Source: the author

shift as well as the filtering operation. f_{IF} presents the larger gain and the bandwidth frequency presents a 3 dB rejection in the voltage gain simulation.

These cases cover the smaller f_{IF} case, a central case, and the largest frequency case, respectively. Input resistance and voltage gain simulations are shown, and markers are placed in the intermediate and bandwidth frequencies. The mismatches between the values expected in the input resistance and the voltage gain simulations are very low in those frequencies.

The minor mismatches are due to approximations used for the system's parameters, switch parasitic resistances, and parasitic capacitances. The input impedance curve also varies fast, close to f_{IF}, and some small approximations in the values of capacitances (C_L) and resistances (R_{FR} and R_{FI}) can cause a mismatch. However, the leading cause of the mismatch is the switch resistance of the variable capacitor, C_L. The switch resistance of the N-Path filter itself is expected and was considered in equations 4.21, 4.18 and 4.19 (represented by R_{sw}). The switches' resistance for the variable resistors, R_{FR} and R_{FI}, are not considered in the equation. However, the resistances R_{FR} and R_{FI} are much larger than the switch resistance. Thus, those switches do not cause a big mismatch. The switch resistance of the variable capacitor is not considered in the equations, and it can cause a big mismatch because a resistance was not expected in the input of the amplifier. Therefore the C_L capacitor's resistance is the one that interferes the most as a parasitic. To reduce the most the switch resistance from C_L, a very large switch is implemented (32 fingers with 35 μm width and 30 nm length each).

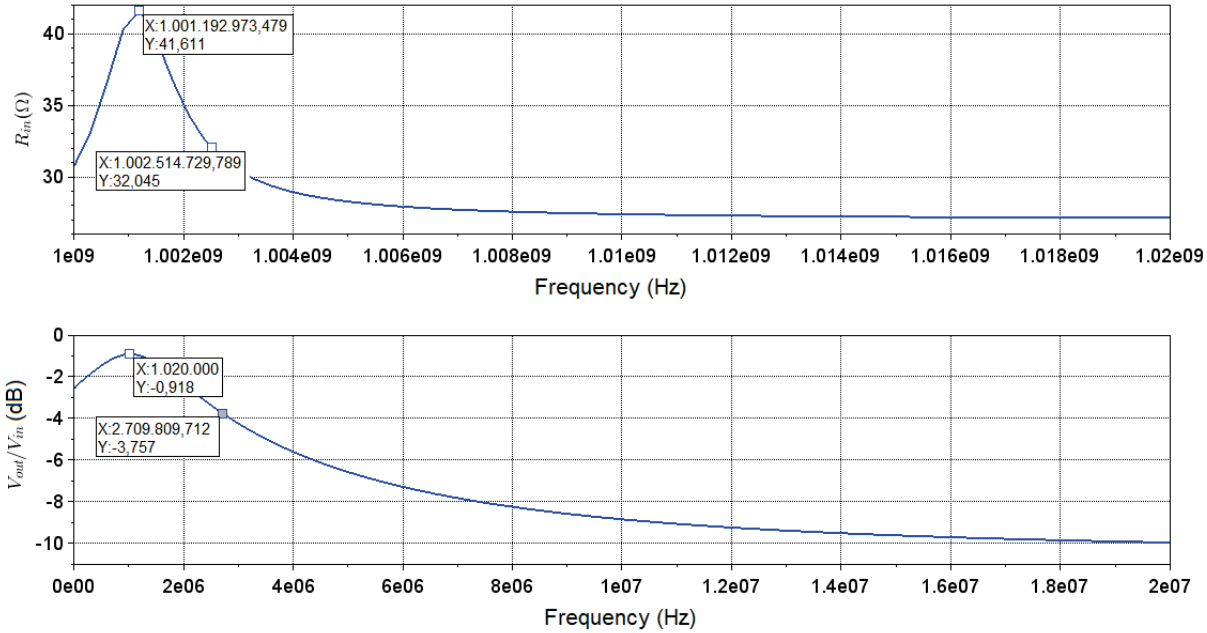
Those mismatches can be observed in figure 5.4, 5.5 and 5.6 in the bandwidth and f_{IF} when R_{in} and V_{out}/V_{in} are compared. Table 5.3 quantifies those mismatches. For the smallest bandwidth values, the error is low. However, the errors start to increase with the higher bandwidth. This is mainly because, in the frequency that defines the bandwidth, only the real value of

the impedance was chosen. With a frequency further from f_{IF}, the imaginary part from the impedance starts to interfere.

Table 5.3: Comparison between the frequencies from the voltage gain simulation and the impedance simulation

f_{IF} (R_{in})	$f_{R_{in2}}$ (R_{in})	f_{IF} (PAC)	$f_{R_{in2}}$ (PAC)	f_{IF} (error)	$f_{R_{in2}}$ (error)
1.19 MHz	2.514 MHz	1.02 MHz	2.709 MHz	170 kHz	195 kHz
4.652 MHz	10.016 MHz	4.148 MHz	10.687 MHz	500 kHz	626 kHz
9.235 MHz	20.037 MHz	8.267 MHz	22.109 MHz	968 kHz	2.072 MHz

Figure 5.4: PAC simulation and input resistance for 1.25 MHz bandwidth and 1.25 MHz f_{IF}



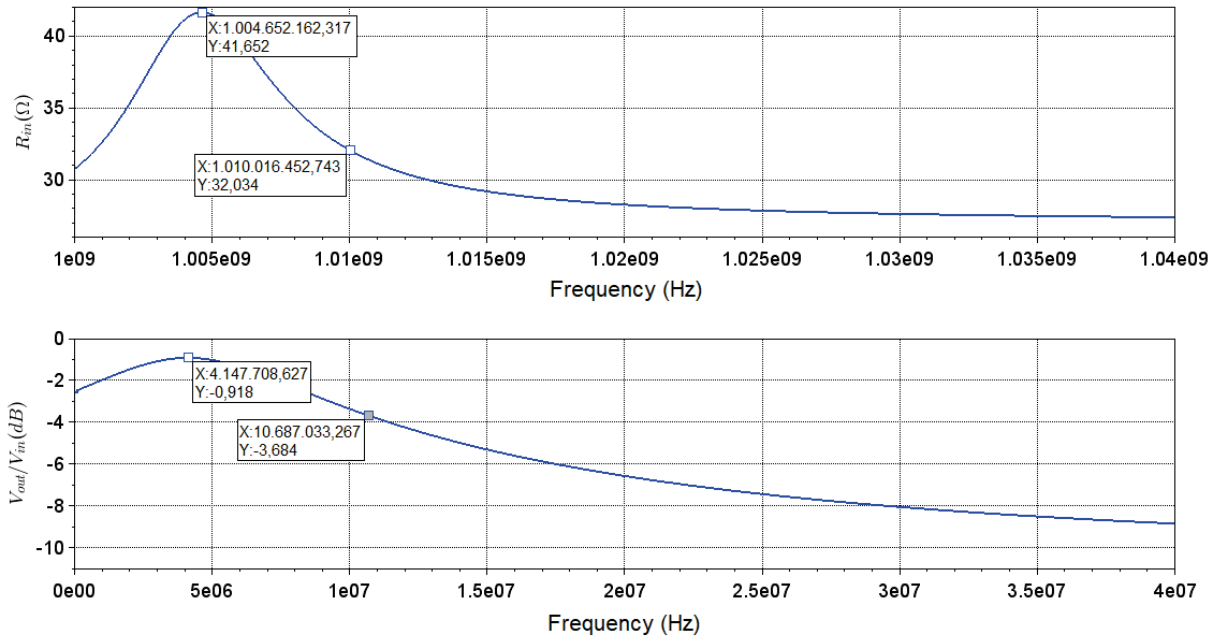
Source: the author

Table 5.4 presents the theoretical f_{IF}, theoretical bandwidths, simulated f_{IF}, simulated bandwidths (for the input resistance simulation) and the errors between them.

Table 5.4: Intermediate frequencies and bandwidths for switching frequency of 1 GHz

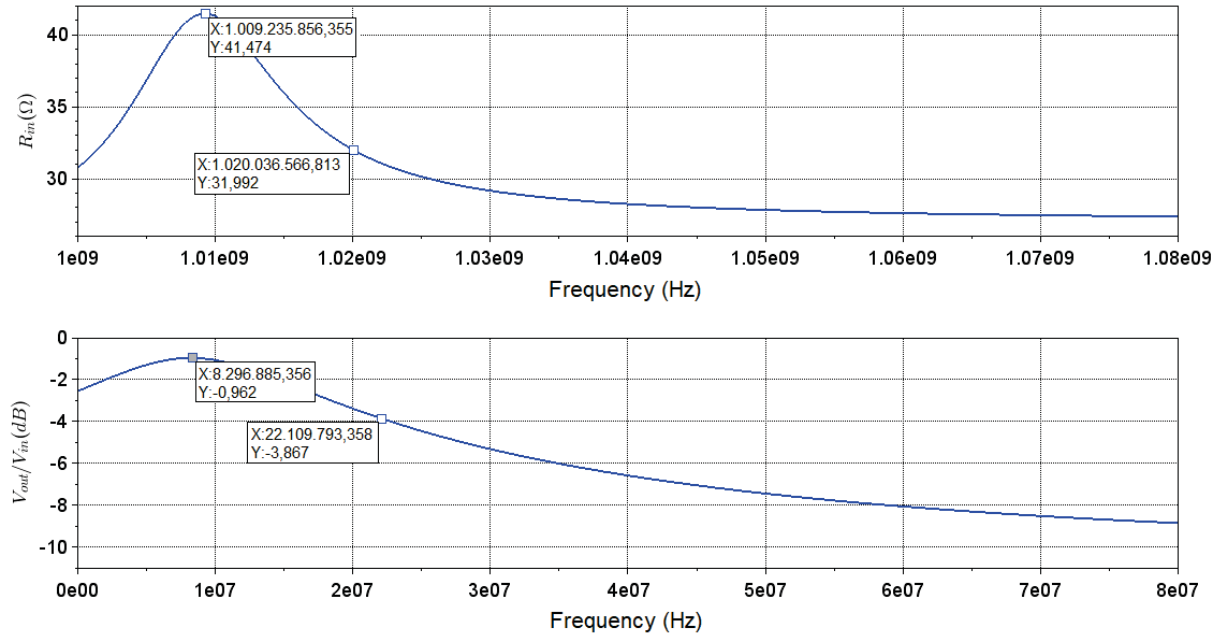
BW (theoretical)	f_{IF} (theoretical)	BW (simulated)	f_{IF} (simulated)	BW (error)	f_{IF} (error)
1.25 MHz	1.25 MHz	1.199 MHz	1.19 MHz	51 kHz	50 kHz
1.25 MHz	2.5 MHz	1.269MHz	2.5 MHz	69 kHz	0
1.25 MHz	5 MHz	1.299 MHz	5 MHz	49 kHz	0
1.25 MHz	10 MHz	1.446 MHz	10 MHz	196 kHz	0
2.5 MHz	2.5MHz	2.797 MHz	2.5 MHz	297 kHz	0
2.5 MHz	5 MHz	2.598 MHz	5 MHz	98 kHz	0
2.5 MHz	10 MHz	2.949 MHz	9.9 MHz	449 kHz	100 kHz
5 MHz	5 MHz	4.983 MHz	5 MHz	17 kHz	100 kHz
5MHz	10 MHz	5.487 MHz	9.9 MHz	487 kHz	100 kHz
10 MHz	10 MHz	10.025 MHz	9.9 MHz	25kHz	100 kHz

Figure 5.5: PAC simulation and input resistance for 5 MHz bandwidth and 5 MHz f_{IF}



Source: the author

Figure 5.6: PAC simulation and input resistance for 10 MHz bandwidth and 10 MHz f_{IF}

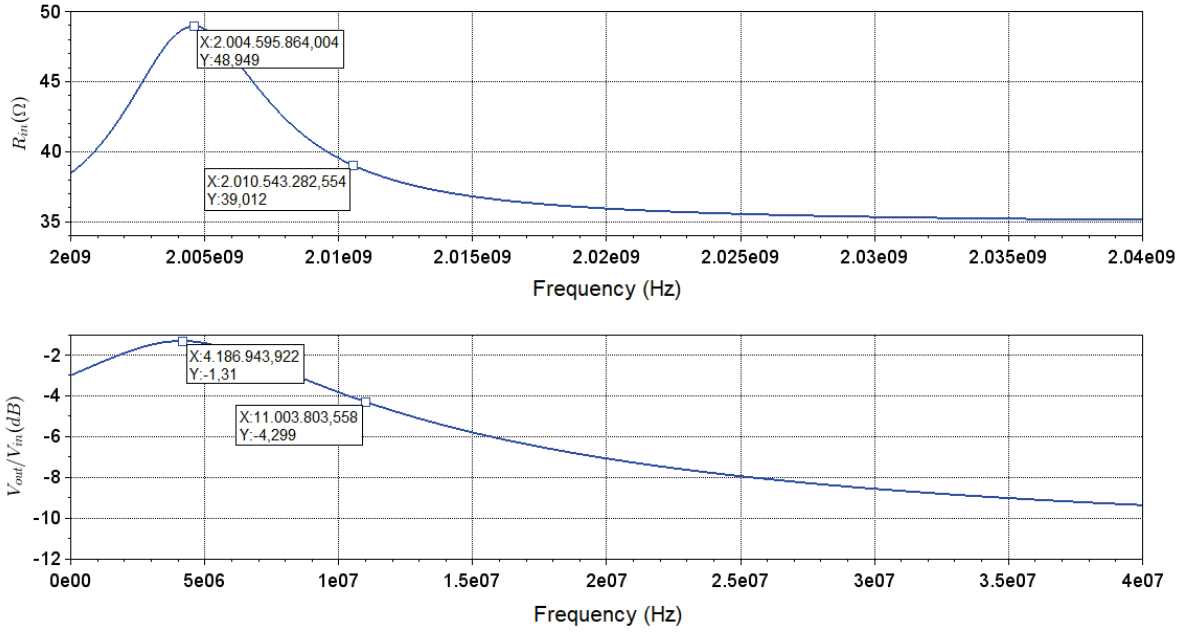


Source: the author

As was mentioned before in chapter 2, the N-Path's center frequency is proportional to f_s. Another simulation keeps C_L, R_{FR}, and R_{FI} while changing f_s. Equations 4.18, 4.19 and 4.21 are complex baseband models, so the bandwidth and the frequency shift related to f_s are kept. Figure 5.7 shows voltage gain and R_{in} for $f_s = 2\ GHz$. R_{FR}, R_{FI} and C_L are kept the same as in the 5 MHz bandwidth and 5 MHz f_{IF}. It is possible to observe that the R_{in}

curve is "shifted up" for both cases. However, even with this shift, some properties are kept. The intermediate frequency of 5 MHz is still the one with better impedance matching, and the frequency with approximately -3 dB gain still 5 MHz above f_{IF}. R_{in2} is now 39 Ω and R_{in} in f_{IF} 49 Ω. Both R_{in} and R_{in2} were "shifted" 7 Ω. Thus, changing f_s, the central frequency is changed, and the input impedance curve increases 7 Ω in all frequencies. However, even with this shift, the system's behavior is still the same. This can be validated by observing the voltage gain curve. The frequency with the better gain is approximately 5 MHZ, and the -3 dB bandwidth is approximately 5 MHz. So it can be observed that the same architecture can be used in different switching frequencies without the further adaptation on R_{FR}, R_{FI}, C_L.

Figure 5.7: Gain simulation and input resistance for 5 MHz bandwidth, 5 MHz f_{IF} and 2 GHz f_s



Source: the author

6 CONCLUSIONS AND FUTURE WORKS

Due to the increasing need for more frequency protocols, it is also wanted to have RF receivers with reconfigurable operation frequency. Many recent works present reconfigurable filters with BAW and SAW filters. Those filters have good linearity and selectivity, but they are not reconfigurable. So for a reconfigurable RF receiver, one BAW or SAW filter is necessary for each operating frequency. The solution presented in the literature uses N-Path filters, which are reconfigurable. However, current works in state of the-art have the disadvantage of being zero-IF, which brings 1/f noise. The solution presented in this work is a low-IF N-Path mixer-1st receiver. Mitigating any noise in this architecture is valid because it will be the first block in the receiver chain (mixer-1st receiver).

This work presented a low-IF N-Path mixer-1st architecture, which has a reconfigurable switching frequency, intermediate frequency, and bandwidth. Theoretical equations and a project pattern were presented. The theoretical equations present a formula for the input impedance and present a way to shift the frequency with better impedance matching. The frequency shift in the input impedance matching makes it possible to transform the zero-IF architecture into low-IF. A "link" was conceived between the input impedance and voltage gain. It was possible to observe the frequency of -3 dB, the bandwidth frequency, and identify the input impedance matching that brings this frequency. This way, the input impedance is controlled the bandwidth and f_{IF}.

Simulations and theoretical equations validated the architecture in the time and frequency domain. The architecture operates with 1.25 MHz, 2.5 MHz, 5 MHz, and 10 MHz bandwidth. f_{IF} are also 1.25 MHz, 2.5 MHz, 5 MHz, and 10 MHz (as long as the f_{IF} is greater than the bandwidth). It was also validated with f_s of 1 GHz and 2 GHz.

The future projects consist of operating the architecture presented with a real low-noise baseband amplifier. It is also desired to understand how much of an impact fabrication mismatches will have in this architecture. If those mismatches are significant, observing if the modes in which two or more resistors or capacitors are switched on (in this work, only the cases where one of each is on were studied) can mitigate those uncertainties. In a scenario where it is not enough to remove the mismatches, it can be necessary to implement the architecture where f_{IF} and bandwidths depend on capacitors and resistors ratios instead of resistors and capacitors' absolute values. As a future project, it is also desired to validate the architecture with noise and linearity once the baseband amplifier is implemented with circuit components.

REFERENCES

[1] Caroline Jayne Andrews. *Analysis and Design of Wideband Passive Mixer-first Receivers*. PhD thesis, Faculty of the Graduate School of Cornell University, 8 2012.

[2] Jin-Shyan Lee, Yu-Wei Su, and Chung-Chou Shen. A comparative study of wireless protocols: Bluetooth, UWB, ZigBee, and Wi-Fi. In *IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society*, pages 46–51, 2007.

[3] Caroline Andrews and Alyosha C. Molnar. A passive mixer-first receiver with digitally controlled and widely tunable RF interface. *IEEE Journal of Solid-State Circuits*, 45(12):2696–2708, 2010.

[4] E. A. M. Klumperink, H. J. Westerveld, and B. Nauta. N-path filters and mixer-first receivers: A review. In *2017 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8, April 2017.

[5] Fujitsu. *MB86L13A LTE-Optimized Transceiver: Ideal for 4G LTE mobile handsets*, 1 edition, 2012.

[6] Rakesh Rena, Suraj Kumar Verma, and Vijaya Sankara Rao Pasupureddi. A process scalable architecture for low noise figure sub-sampling mixer-first RF front-end. In *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, 2021.

[7] Luis H. A. Lolis, Guilherme Sionek, André A. Mariano, and Thiago H. Freitas. A discrete-time double-quadrature low-IF receiver for multi-standard and multi-carrier applications. *Analog Integrated Circuits and Signal Processing*, 108:335–349, 2021.

[8] N. F. Barber. Narrow band-pass filter using modulation. *Wireless Enginner*, pages 132–134, 1947.

[9] L. E. Franks and I. W. Sandberg. An alternative approach to the realization of network transfer functions: The N-path filter. *The Bell System Technical Journal*, 39(5):1321–1350, Sep. 1960.

[10] Dong Yang, Caroline Andrews, and Alyosha Molnar. Optimized design of N-phase passive mixer-first receivers in wideband operation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(11):2759–2770, 2015.

[11] Ben W. Cook, Axel Berny, Alyosha Molnar, Steven Lanzisera, and Kristofer S. J. Pister. Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply. *IEEE Journal of Solid-State Circuits*, 41(12):2757–2766, 2006.

[12] M. C. M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta. A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving »11 dBm IIP3 and «6.5 dB NF. In *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pages 222–223,223a, 2009.

[13] David Murphy, Hooman Darabi, Asad Abidi, Amr A. Hafez, Ahmad Mirzaei, Mohyee Mikhemar, and Mau-Chung Frank Chang. A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications. *IEEE Journal of Solid-State Circuits*, 47(12):2943–2963, 2012.

[14] Prateek Kumar Sharma and Nagarjuna Nallam. Breaking the performance tradeoffs in N-path mixer-first receivers using a second-order baseband noise-canceling TIA. *IEEE Journal of Solid-State Circuits*, 55(11):3009–3023, 2020.

[15] Anoop Narayan Bhat, Ronan van der Zee, Salvatore Finocchiaro, Francesco Dantoni, and Bram Nauta. A baseband-matching-resistor noise-canceling receiver architecture to increase in-band linearity achieving 175 MHz TIA bandwidth with a 3-stage inverter-only OpAmp. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 155–158, 2019.

[16] Qaiser Nehal. Low power mixer-first receiver with second-order baseband filtering TIA. In *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 117–120, 2020.

[17] Shimin Huang and Alyosha Molnar. A 3.7-6.5GHz 8-phase N-path mixer-first receiver with LO overlap suppression achieving <5 dB NF and >5 dBm OOB B1dB. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 87–90, 2021.

[18] Charles Wu, Yanjie Wang, Borivoje Nikolic, and Christopher Hull. A passive-mixer-first receiver with LO leakage suppression, 2.6 dB NF, >15dBm wide-band IIP3, 66 dB IRR supporting non-contiguous carrier aggregation. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 155–158, 2015.

[19] Caroline Andrews, Changhyuk Lee, and Alyosha Molnar. Effects of LO harmonics and overlap shunting on N-phase passive mixer based receivers. In *2012 Proceedings of the ESSCIRC (ESSCIRC)*, pages 117–120, 2012.

[20] Sashank Krishnamurthy and Ali M. Niknejad. Enhanced passive mixer-first receiver driving an impedance with 40 dB/decade roll-off, achieving +12 dBm blocker-P1dB, +33 dBm IIP3 and sub-2 dB NF degradation for a 0 dBm blocker. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 139–142, 2019.

[21] Yuan-Ching Lien, Eric A. M. Klumperink, Bernard Tenbroek, Jon Strange, and Bram Nauta. Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback. *IEEE Journal of Solid-State Circuits*, 53(5):1348–1360, 2018.

[22] Shouri Chatterjee, Kamlesh Badiyari, and Nagarjuna Nallam. An N-path band-pass filter with parametric gain-boosting. In *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–1, 2020.

[23] T.J. Aprille and T.N. Trick. Steady-state analysis of nonlinear circuits with periodic inputs. *Proceedings of the IEEE*, 60(1):108–114, 1972.

[24] S.H.M.J Houben and J.M. MAubach. Periodic steady-state analysis of free-running oscillators. *Lecture Notes in Computational Science and Engineering*, 18, 2001.