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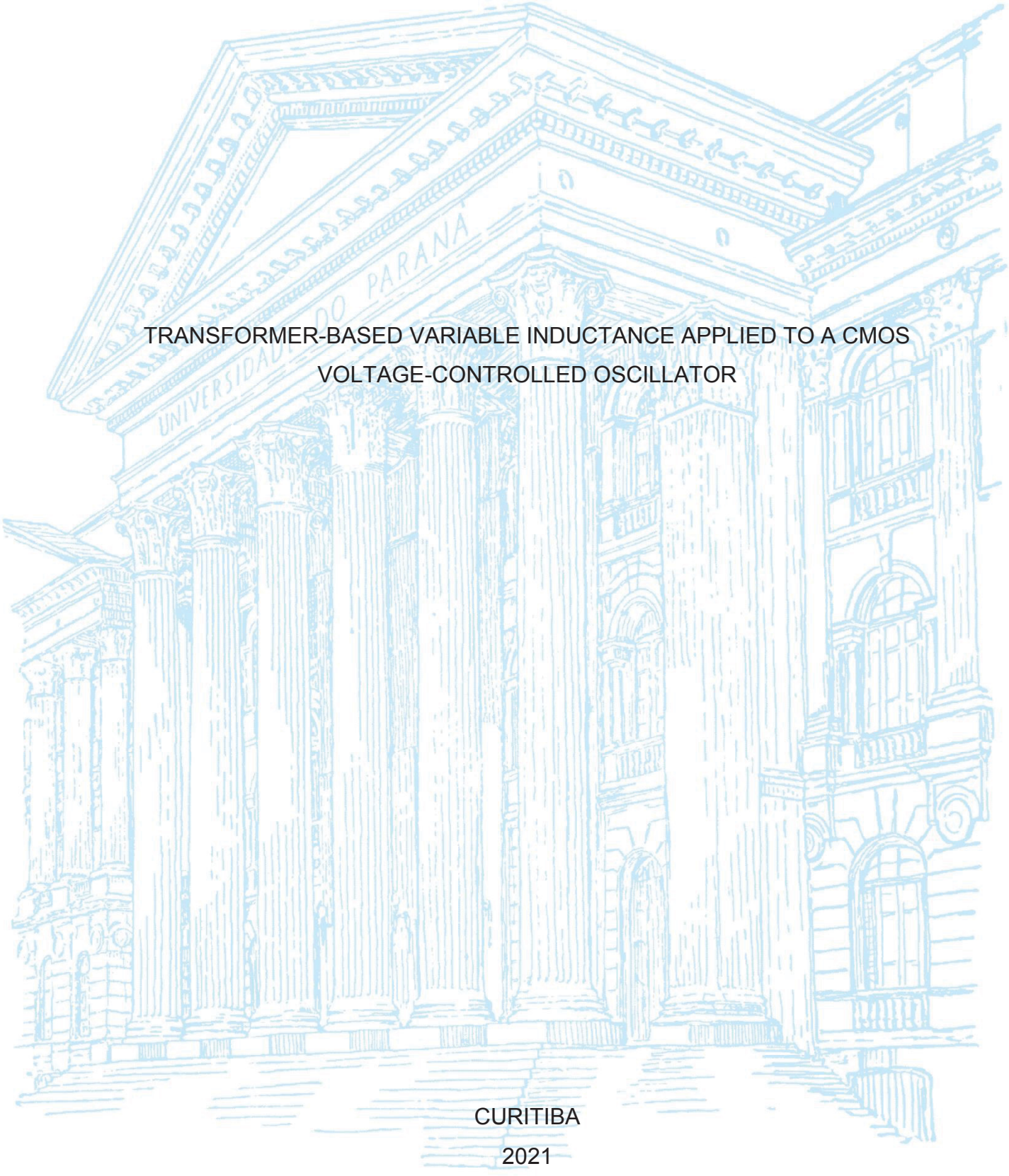
RODRIGO GODINHO SILVA



TRANSFORMER-BASED VARIABLE INDUCTANCE APPLIED TO A CMOS VOLTAGE-CONTROLLED OSCILLATOR

CURITIBA

2021

RODRIGO GODINHO SILVA

TRANSFORMER-BASED VARIABLE INDUCTANCE APPLIED TO A CMOS VOLTAGE-CONTROLLED OSCILLATOR

Tese apresentada ao curso de Pós-Graduação em Engenharia Elétrica, Setor de Tecnologia, Universidade Federal do Paraná, como requisito parcial à obtenção do título de Doutor em Engenharia Elétrica - Telecomunicações.

Orientador: Prof. Dr. Bernardo Rego Barros de Almeida Leite

Coorientador: Prof. Dr. André Augusto Mariano

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TERMO DE APROVAÇÃO

Os membros da Banca Examinadora designada pelo Colegiado do Programa de Pós-Graduação em ENGENHARIA ELÉTRICA da Universidade Federal do Paraná foram convocados para realizar a arguição da tese de Doutorado de **RODRIGO GODINHO SILVA** intitulada: **Transformer-based variable inductance applied to a CMOS voltage-controlled oscillator**, sob orientação do Prof. Dr. BERNARDO REGO BARROS DE ALMEIDA LEITE, que após terem inquirido o aluno e realizada a avaliação do trabalho, são de parecer pela sua APROVAÇÃO no rito de defesa.

A outorga do título de doutor está sujeita à homologação pelo colegiado, ao atendimento de todas as indicações e correções solicitadas pela banca e ao pleno atendimento das demandas regimentais do Programa de Pós-Graduação.

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RESUMO

Com o aumento constante dos requisitos necessários para operação em padrões de comunicação mais recentes, aliado à indispensabilidade da interação com os padrões já existentes, a complexidade e integrabilidade na implementação de circuitos de radiofrequência tem alcançado patamares cada vez mais altos. Em paralelo, existe a sempre crescente necessidade da redução do consumo da energia gasta em circuitos eletrônicos integrados. Neste cenário, a versatilidade dos circuitos é essencial. Diversos elementos como capacitores e transistores dispõem de soluções corriqueiras em se tratando de variabilidade, permitindo que esses elementos operem dependendo de um controle externo, promovendo assim essa versatilidade tão essencial. Por outro lado, indutores integrados ainda carecem de soluções mais consistentes. Este trabalho apresenta uma estrutura capaz de fornecer diferentes indutâncias utilizando um transformador e um esquema de chaveamento; o funcionamento da estrutura é descrito, bem como suas limitações. A operação do transformador é extraída a partir de simulações eletromagnéticas, possibilitando uma análise criteriosa do seu funcionamento. Um oscilador controlado por tensão é projetado utilizando uma indutância variável com quatro modos de operação; os resultados são extraídos através de simulações pós-leiaute. As quatro indutâncias fornecidas pela estrutura permitem um considerável alcance percentual de frequências de oscilação de aproximadamente 88%. O circuito oscila entre 2.31 GHz e 5.93 GHz, apresentando uma frequência central de 4.12 GHz. O ruído de fase em 1 MHz varia entre - 108 dBc/Hz e - 117.7 dBc/Hz mantendo um consumo de potência abaixo de 3.21 mW. Esses parâmetros rendem uma FoMT entre - 214 dBc/Hz e - 224 dBc/Hz; resultados bastante interessantes quando comparados ao atual estado da arte.

Palavras-chave: Indutância Variável. Circuitos de Radiofrequência. Circuitos Integrados. Transformadores. Oscilador Controlado por Tensão.

ABSTRACT

In order to keep up with the increasing requirements that the newest communication standards demand while being capable of interacting with older technologies, radiofrequency circuits need to achieve an ever-increasing level of integrability and complexity in its implementation. Accompanying this tendency is the environmental necessity to reduce energy consumption in electronic devices; versatility is key in this scenario. Different elements such as capacitors and transistors possess ubiquitous solutions in variability, allowing these elements to perform in accordance to an external control composition, granting them a so desired versatility. Variable inductors, however, still struggle to present a dependable solution. This work presents an integrated transformer-based variable inductance that utilizes a switching scheme to present an interchangeable equivalent inductance; the proposed structure is described and its capabilities and limitations are discussed. Electromagnetic simulations are utilized to extract the operating performance of the proposed structure, which conveys reliable results. An integrated voltage-controlled oscillator is designed utilizing a 4-mode variable inductance and its performance is extracted from post-layout simulations. Due to the four different equivalent inductances provided to oscillator, an extended frequency tunning range (of around 88%) is achieved. The circuit oscillates from 2.31 GHz to 5.93 GHz, with a central frequency of 4.12 GHz. A phase noise @ 1 MHz varying from -108 dBc/Hz to -117.7 dBc/Hz is obtained, while consuming no more than 3.21 mW. These parameters promote a FoM_T from - 214 dBc/Hz to - 224 dBc/Hz, which are notable results when compared to state-of-the-art circuit.

Keywords: Variable Inductance. Radiofrequency Circuits. Integrated Circuits. Transformer. Voltage-Controlled Oscillator.

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RF	- Radiofrequency
VCO	- Voltage-Controlled oscillator
PA	- Power Amplifier
LNA	- Low-Noise Amplifier

SUMMARY

1 INTRODUCTION

The surge in popularization of handheld applications, as well the dissemination of technologies such as internet of things and its consequent impact in the industry 4.0, further increased the relevance of wireless applications in the last decade. Consequently, radiofrequency (RF) devices' complexity has been increasing to keep up with the higher demands expected from new implementations. Despite that, lower energy consumption and higher integrability are also defining criteria of these solutions.

One technique utilized to allow for a lower energy consumption is the implementation of reconfigurable circuits. Activating or deactivating portions of the circuit depending on the situation can promote smart energy consumption and is already exercised in multi-mode applications (HUYNH; LEE; NGUYEN, 2014; TANT et al., 2015). Moreover, reconfiguring individual elements also allows to adjust several functionalities that depends on its parameters, such as the LC tank resonant frequency in VCOs (HUANG; HSU; WANG, 2019), or the output matching in a PA (KO; LEE; NAM, 2017).

In order to deal with the premise of multi-mode applications, an important tool is the utilization of controllable elements, since by altering the properties in one or more devices it is possible to enable the desired multi-mode operation without the inclusion of any additional circuitry. Since transistors are devices whose operation depends on an external biasing, they are the most common source of external control exercised in integrated circuits.

Since passive elements carry a strong dependance on its geometric characteristics, the component's size also needs to be taken into consideration when designed in integrated circuits. Despite that, variable capacitances can be implemented by capitalizing on the parasitic capacitance manifested in CMOS transistors and its correlation to the voltage applied to the transistor's terminals; this technique is prevalent in VCOs (such as in (LIM; NOH; YUN, 2017; LU; WANG; HORNG, 2013; ZOU et al., 2019)).

Integrated variable inductances are more challenging to implement. Despite that, different approaches have been employed to achieve variable inductances ((AGARWAL; PANDE; HEO, 2015; HUANG; HSU; WANG, 2019; JIN; WU; XUE, 2018; KO; LEE; NAM, 2017; PARK et al., 2004; QING et al., 2009; SADHU; OMOLE; HARJANI, 2008; VIGILANTE; REYNAERT, 2015; YOU; HUANG, 2013)). These

solutions required the designing of integrated inductors and applying an external control source (usually transistors) in order to provide these elements with the desired variability. In this regard, designing integrated inductors is especially complicated, since its layout usually occupies a considerable area when compared to other elements (even among other passive devices such as resistors and capacitors). These elements are also widely employed in RF circuits, such as power amplifiers (PA) (DONG; MAO; XIE, 2017; ZHAI; CHENG, 2018), low noise amplifiers (LNA) (QIN; XUE, 2017), (HEDAYATI et al., 2018), mixers (CHEN; CHIANG; JOU, 2009; KASHANI et al., 2019), voltage-controlled oscillators (VCO) (LI et al., 2017; ZOU et al., 2019), switches (JIN; NGUYEN, 2007; PARK; LEE; HONG, 2020), among other applications. This means that this element possesses remarkable importance in the radiofrequency ecosystem and taking advantage of a consistent variable inductance could be significantly beneficial.

This thesis is organized as follows: Chapter 2 reviews the theoretical baseline used to develop the structure, while assessing similar projects and state of the art applications. Chapter 3 presents the variable inductance and the ideal operation, followed by utilizing real elements and electromagnetic simulations to characterize the transformer. Finally, Chapter 4 shows the design process of the variable inductance, followed by an application developing a wideband voltage-controlled oscillator.

1.1 OBJECTIVES

This work aims to present a transformer-based reconfigurable integrated inductance by switching connections between the windings of the transformer. Altering the active connections controls the overall equivalent inductance delivered by the structure. A study of the resulting inductance based on the configurations is presented, as well as a use case for the proposed structure.

1.1.1 Main Objective

This work’s main objective is to propose, describe, design and implement a transformer-based integrated variable inductance.

1.1.2 Secondary Objectives

In order to reach this work's main objective, the following objectives must also be attained.

1. Analyze current solutions in variable integrated inductances.
2. Propose an alternative to the solutions found in the literature.
3. Characterize the proposed alternative, investigate its advantages as well as its shortcomings.
4. Introduce a comprehensive method analysis of the proposed structure.
5. Design the proposed structure and simulate its implementation in an RF circuit.

2 THEORETICAL FOUNDATION

This chapter presents figures of merit to evaluate the inductance delivered by the transformer-based structure, an overall introduction to integrated transformers and the technology used in this thesis. Lastly, a collection of previous works on integrated variable inductances are presented.

2.1 FIGURES OF MERIT

Two main figures of merit are commonly utilized to evaluate integrated inductors: the equivalent inductance and the quality factor. The inductance is an intrinsic property of every circuit where there is current flowing; it is related to the circuit's physical geometry. A common definition to inductance is the ratio of the of flux linkage (that represents the sum of all magnetic fluxes applied to a specific element) and the electric current flowing through the element.

In order to obtain the equivalent inductance, its scattering parameters are extracted through measurement (or simulations) and, mathematically converted to impedance parameters. From the impedance matrix, the equivalent impedance is extracted and can be described by:

$$Z_{DD} = Z_{11} + Z_{22} - Z_{21} - Z_{12} \quad (1)$$

and, subsequently, the equivalent inductance is obtained by:

$$L_{eq} = \frac{imag(Z_{DD})}{\omega} \quad (2).$$

The fundamental definition of an inductor's quality factor correlates the average power dissipation and the maximum energy storage. In integrated circuits process technologies is commonplace to interpret the quality factor as the difference between the average magnetic and electric stored energies(KENNETH, 1998), as defined by:

$$Q = -\frac{imag(Z_{DD})}{real(Z_{DD})} \quad (3).$$

Finally, it is interesting to note the self-resonant frequency. It is a metric defined by the frequency in which the inductor resonates with its own parasitic capacitances.

In frequencies higher than the self-resonant frequency, the inductor behaves as a capacitor (DANG; MILADY; MEINERZHAGEN, 2012). It can be obtained by analyzing the frequency in which the equivalent inductance (and quality factor) drops to zero, before acting as a capacitance (i.e., when the inductance becomes negative).

2.2 INTEGRATED TRANSFORMERS

Integrated transformers are devices comprised of two (or more) magnetic coupled windings laid out in a stack of layers over a substrate. Each winding exhibits a self-inductance, when coupled with another winding the electromagnetic flux from the second winding influences the first winding's inductance, this effect is known as mutual inductance.

The self-inductance is a byproduct from the magnetic flow generated from the coil when there is a variable current flowing through. It can be described by:

$$L = \frac{\psi_{11}}{I_1}, \tag{4}$$

the mutual inductance originates from a magnetic flux flowing from a second coil through the first one. This incites a current flow in the first winding, which affects its self-inductance, this effect is known as the mutual inductance and can be represented by:

$$M_{21} = \frac{\psi_{21}}{I_1}. \tag{5}$$

Another intrinsic characteristic in transformers is the parasitic resistance inherent to each coil. It is a function of the resistivity of the conductor and the coil's dimensions. However, as the operation frequency increases, the current tends to flow through the element's surface, which reduces the conductor's effective cross-cut area, increasing its resistance. This phenomenon is called skin effect.

Integrated inductors, as well as transformers present their own complexity in its design; since integrated technologies are comprised of a set of layers stacked on top of each other, topologies employed in these elements are limited. Depending on the technology utilized, the angles between the conductors placed in the layers are restricted. Typically, the transformer's windings are arranged horizontally, as

exemplified in figure 1. It is interesting to notice that, in the same occupied area, the higher the number of sides, higher the resistance and inductance delivered by the winding. However, the inductance grows faster than the resistance, culminating in a higher quality factor (FAKHFAKH; TLELO-CUAUTLE; SIARRY, 2015). Therefore, utilizing a topology with the higher number of sides possible is usually the best choice.

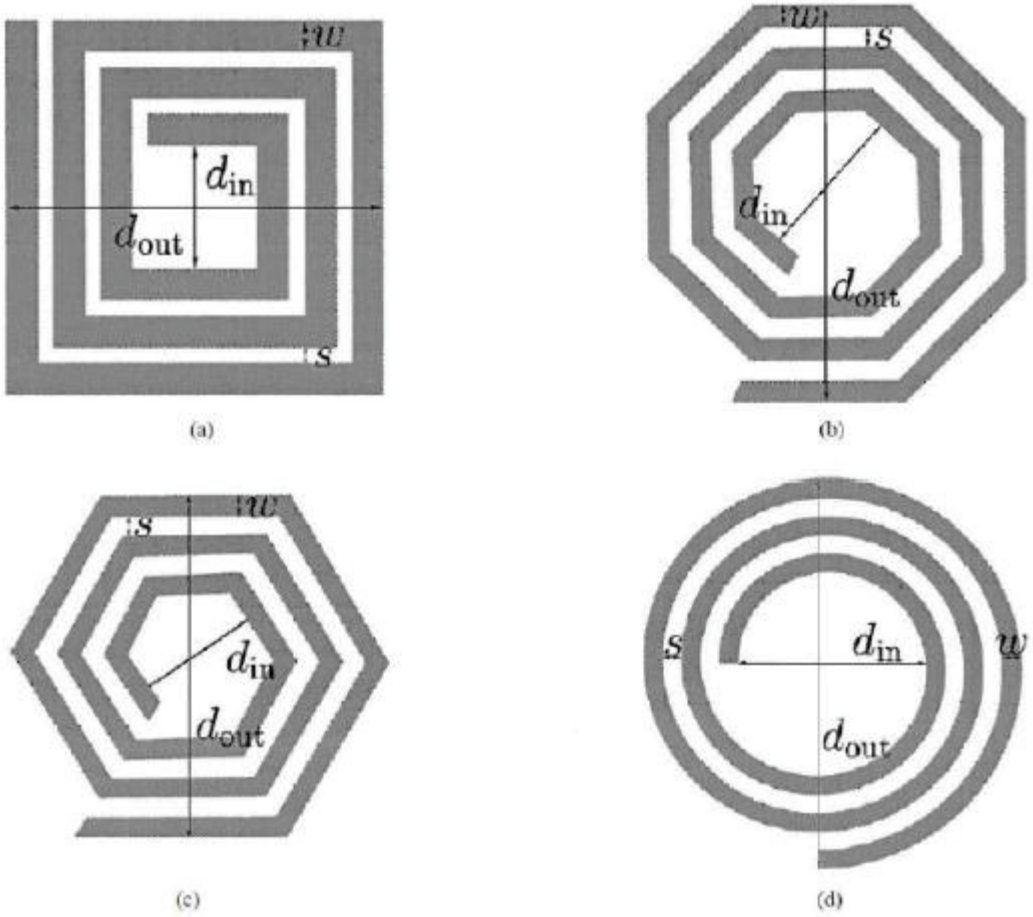

Figure 1 - (a) Squared Topology (b) Octogonal Topology (c) Hexagonal Topology (d) Circular Topology (MOHAN et al., 1999)

After determining the winding topology, the positioning between the first and second coils must be established; this positioning will dictate the magnetic coupling between the coils. The resulting magnetic coupling is determined by the magnetic flux flowing from one winding through the other, generating a current in the second winding. This relationship between magnetic flux and induced current in distinct windings is the magnetic coupling.

In the integrated circuits environment, two main types of magnetic coupling are usually described: vertical coupling, as exemplified in figure 2(a), and horizontal coupling, as illustrated in figure 2(b). In the vertical coupling each winding is segmented

in a different layer, enabling the magnetic field produced by one coil to flow directly through the other. Therefore, the vertical coupling is able to pertain a higher effective area in which the magnetic field from one coil passes through the other, which means that, typically, the vertical coupling is higher than the horizontal. Also, since each winding is located in a different layer there is a higher freedom in the design of each individual winding in the vertical coupling. If the magnetic flow in both coils follows the same direction, the mutual inductance between both windings is positive.

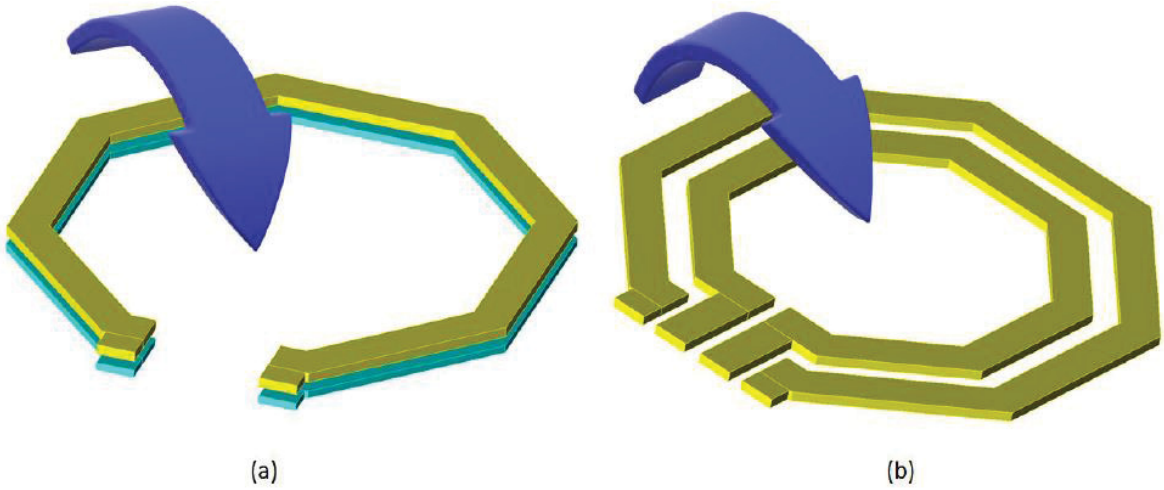

Figure 2 - (a) Example of vertical coupling (b) Example of horizontal coupling

A metric commonly utilized to assess the strength of the magnetic coupling is the magnetic coupling coefficient (k) and can be obtained by the ratio between the mutual inductance (M) and the square root of the product between the inductance of each winding (where L_p is the primary winding's inductance and L_s is the secondary's), as represented by:

$$k = \frac{M}{\sqrt{L_p . L_s}}. \tag{6}$$

Another important consideration is the capacitance between the windings. In the vertical coupling composition, the capacitance between coils is usually higher, since both windings usually are placed directly on top of each other. The design of the coils is also somewhat limited in the vertical coupling composition; if the coil placed in the top layer requires more than one turn, a cross-section in the lower layer needs to be added to the layout in order to enable said additional turns. The lower coil can be

designed around this cross-section, or simply be placed at an even lower layer (which usually reduces the overall quality factor of this winding).

The integrated transformer also presents a capacitance to the substrate in the bottom of the layer stack. This capacitance is detrimental to the transformer operation, since it reduces the self-resonant frequency of by the element. In order to reduce this capacitance, the higher layer is chosen to design the windings. In the vertical coupling, the secondary winding is located in the second highest layer, which means that it presents a higher capacitance to the substrate than the primary, being a disadvantage against the horizontal coupling with two windings placed in the top layer.

Due to the layered arrangement employed in integrated circuits, integrated transformers present inherent particular characteristics. A 130 nm BiCMOS technology is utilized in this work; this technology stacks several layers over a substrate and possesses one thick top layer, which is normally utilized to design the passive elements in the circuit, since the higher distance from the substrate reduces its parasitic capacitance to the substrate. The thickness of the layer also reduces the internal resistance of the conductors implemented in this layer, as it increases the cross-cut area of the windings. A visual representation of the layer's stacking pile is shown in figure 3.

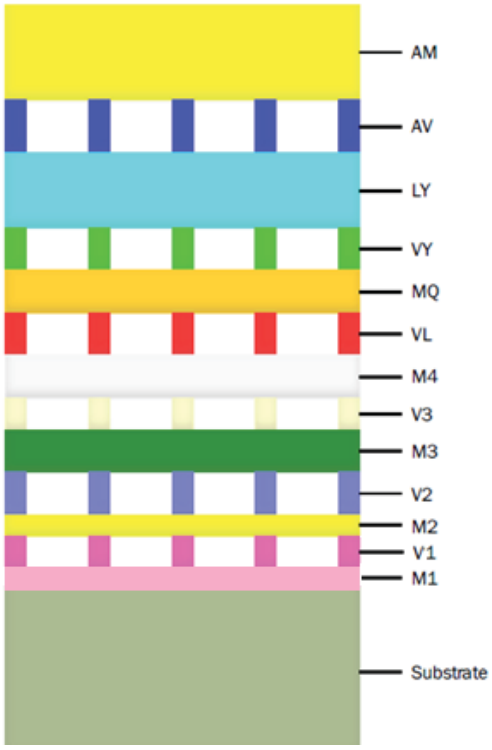

Figure 3 - Layer's representation in the 130nm biCMOS technology (dimensions not to scale)

As previously mentioned, the technology utilized in this work only provides one thick layer, which drastically reduces the quality factor of windings located in the LY layer (or lower). Add that to the fact that a winding in a lower layer present a higher capacitance to the substrate and that the vertical coupling topology exhibits a usually higher capacitance between windings, the chosen topology to work with was the one with the horizontal coupling. Finally, a patterned shield was implemented in the metal layer M1, in order to reduce substrate losses (especially due to eddy currents in the substrate)(FAKHFAKH; TLELO-CUAUTLE; SIARRY, 2015) .

2.2.1 Integrated Transformer Models

In order to better comprehend the operation of integrated transformers, compact models of this element are presented. In (LONG; DANESH, 2001), the model in Figure 4 is proposed. In this work, the winding is divided in *n* segments that are modeled and connected; for the presented model, the coil was divided in two equal parts. The model of each part is assembled in a π topology, where the internal resistance (r) and inductance (L) of the coil are connected to the technology's oxide capacitive effect (C_{OX}) and the resistive (R_{si}) and capacitive (C_{si}) effects of the substrate. The model of each coil relates to each other through their mutual inductance (M) and a capacitance representing the capacitive effect between the windings (C_O). This model utilizes a resistance that varies in relation to the operating frequency to emulate the skin effect.

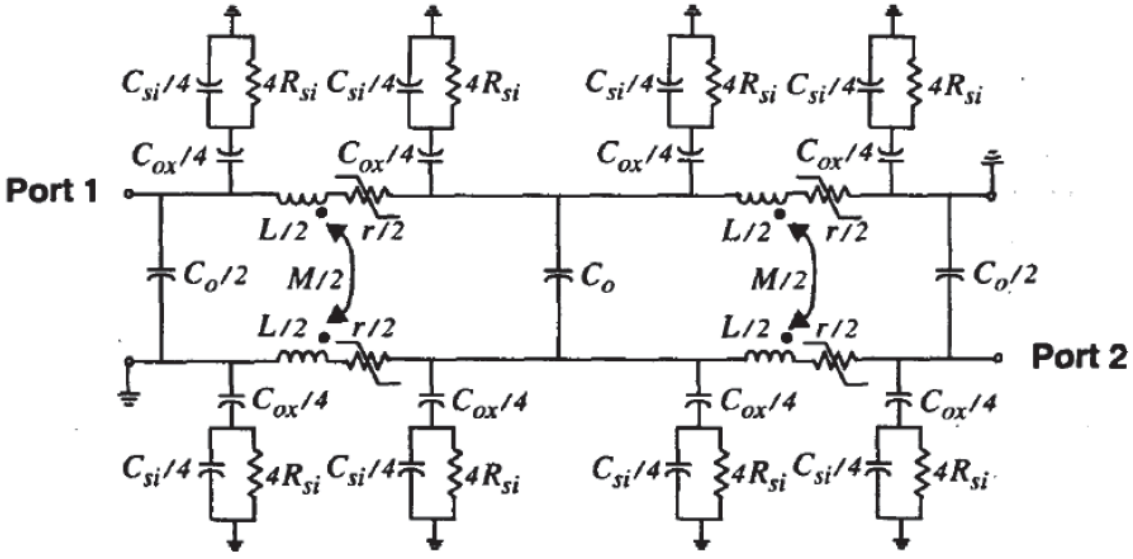

Figure 4 – Integrated transformer's model example (LONG; DANESH, 2001)

The work presented in (LEITE, 2009) proposes a physics-based predictive model of a symmetric octagonal transformer, shown in Figure 5. Through the physical characteristics of the element, the parameters are obtained. Once again, we can observe the oxide capacitance (C_{POX}), substrate capacitance (C_{PSUB}) and resistance (R_{PSUB}), the coils' inductance (L_P) and resistance (R_P), as well as the capacitance (C_{PS}) and mutual inductance (M) between the coils.

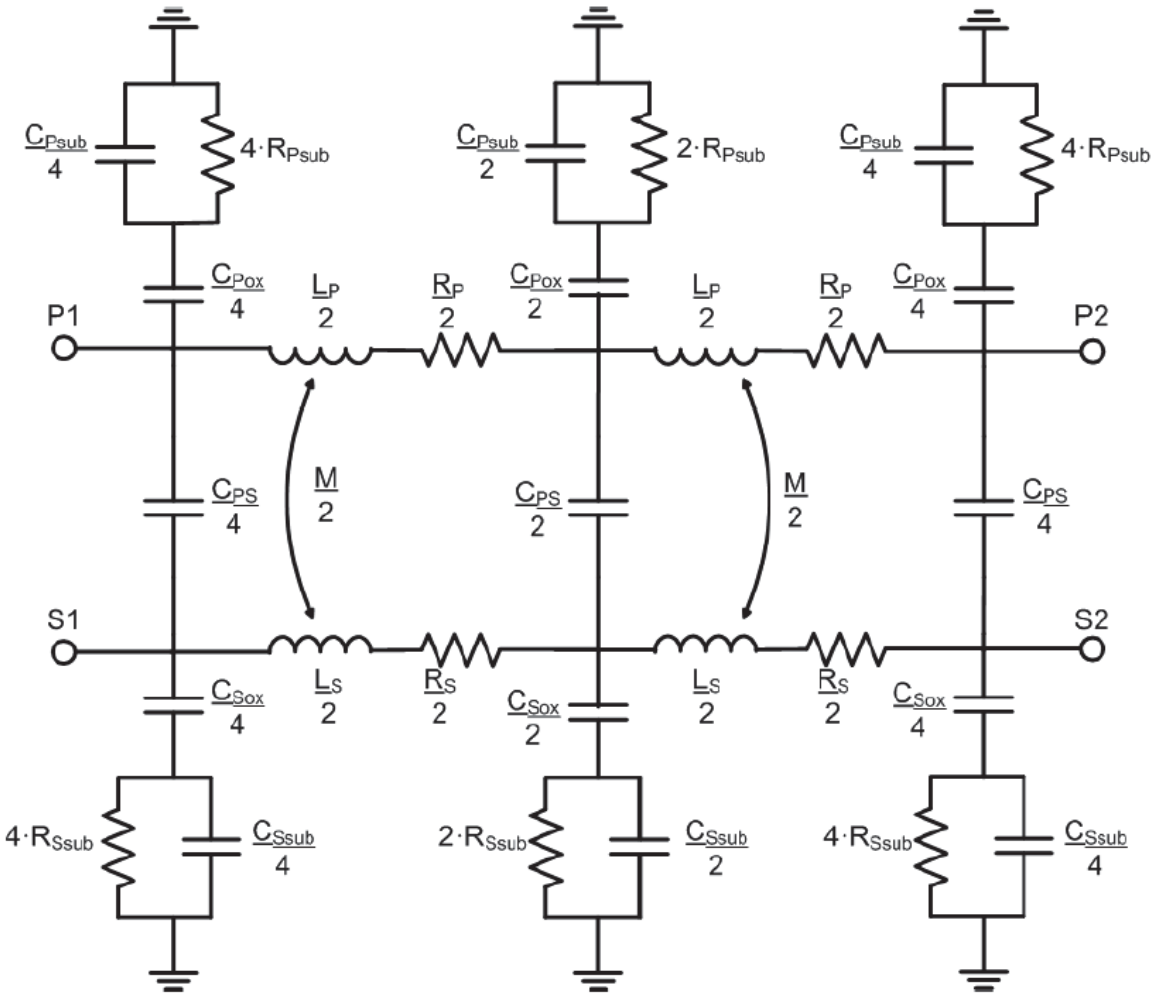

Figure 5 –Predictive model of a transformer (LEITE, 2009)

As mentioned in (LEITE, 2009), substrate capacitance is determined by the technology, the oxide capacitance depends on the coils' path surface and the distance between its layer and the substrate; the substrate resistance hinges on the substrate resistivity and the conductor's dimensions. The internal resistance and inductance depend on the coil's geometry and dimensions; more specifically, the integrated inductance can be described as:

$$L = \frac{0.42\mu_0}{\pi}.l\left(ln\left(\frac{2l}{0.2235(w+t)}\right) + \frac{0.2235(w+t)}{l} - 1\right), \quad (7)$$

where μ_0 is the material permeability and is determined by the technology, w and l refers to the width and length of the inductor, whereas t is the thickness of the layer in which the inductance is located. From there, it is possible to notice the effect of each parameter in the overall inductance delivered by each coil.

2.3 INTEGRATED VARIABLE INDUCTANCES

The implementation of variable inductances in integrated circuits can certainly be beneficial to distinct types of applications. Therefore, several works have presented diverse solutions aiming towards this type of device.

The work presented in (PARK et al., 2004) concerns a four-mode variable inductance using a multilayer inductor controlled by MOSFET switches. This solution, which is illustrated in figure 6, connects three inductors in series and is able to switch out up to two of the inductors by attaching a control switch in parallel to them. When the control switches are open, the current flows through the winding, whereas when the switches are closed, the current flows through the switch, lowering the structure's overall inductance.

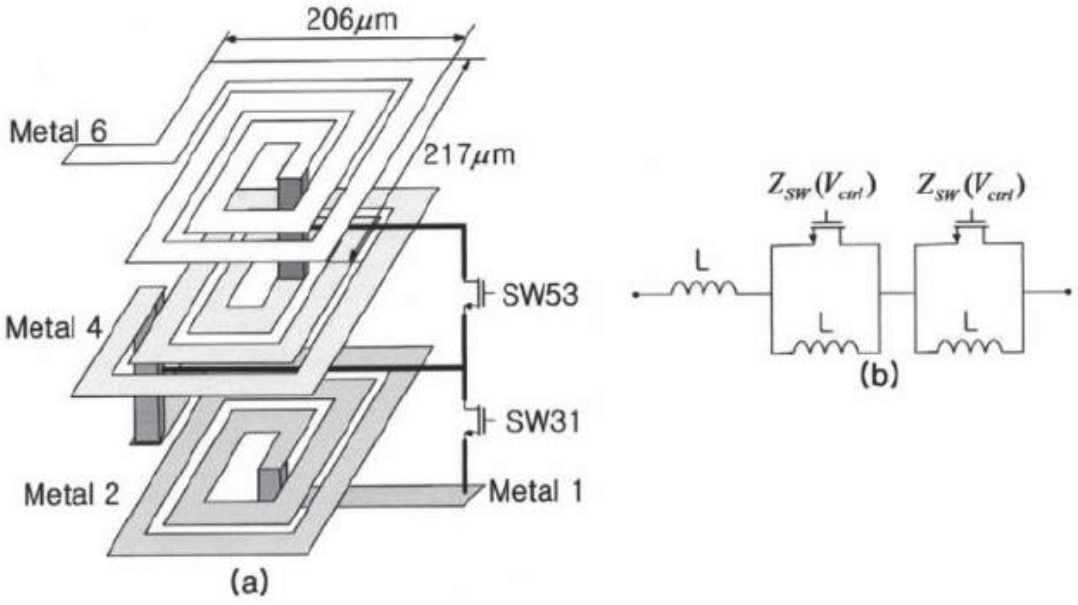

Figure 6 - Stacked inductors (a) Layout (b) Schematic (adapted from (PARK et al., 2004))

The structure proposed in (PARK et al., 2004) was developed to operate in a single frequency (2.4 GHz). Through the control of the biasing on the switches, the inductance can be continuously altered between 8 nH to 23 nH at 2.4 GHz. However, the maximum quality factor reached in this work fluctuates between 2 and 5.

Similarly, (HUANG; HSU; WANG, 2019; QING et al., 2009; YOO et al., 2009) suggest a parallel connection between the variable inductors. In (HUANG; HSU; WANG, 2019) and (YOO et al., 2009), one switch is used to disconnect the parallel inductance (as exemplified in figure 7), allowing for a two-mode variable inductance. The inductance when the switch is open corresponds to the inductance on the primary inductor (L1), while the inductance when the switch is closed corresponds to the parallel between the L1 and L2 inductances and the effect of the mutual inductances between the coils.

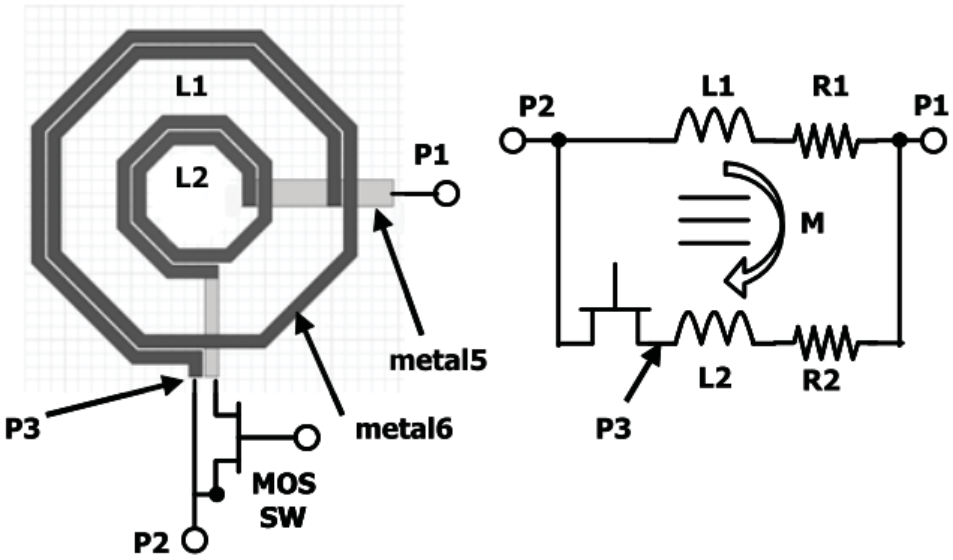

Figure 7 – Two-mode switched inductor (AHN et al., 2018)

Meanwhile, (QING et al., 2009) utilizes two different switches in order to provide a three-mode variable inductance corresponding to the primary inductance (L1), the secondary inductance (L2) and the parallel between both inductances when both switches are closed, as shown in figure 8. This configuration was utilized to design an LC-tank based wide range VCO, by taking advantage of the three distinct inductances offered by the structure.

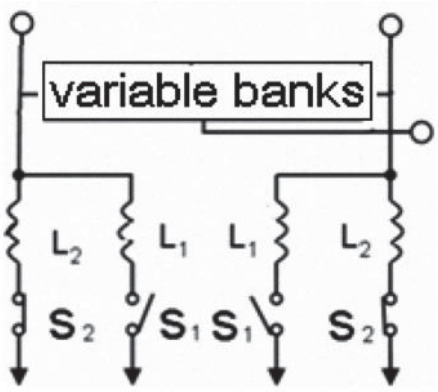

Figure 8 - LC-tank based variable inductance (adapted from (QING et al., 2009))

Another interesting option is proposed by (SADHU; OMOLE; HARJANI, 2008), where the switching allows for a shortening (or lengthening) in the current path of the structure. Figure 9 illustrates that idea; it is possible to notice that when the switch is closed, it allows the current to flow through the small internal path in the inductor; when open, the current flows through the largest internal path. It is a similar concept than the ones previously presented, but implemented in a unique manner.

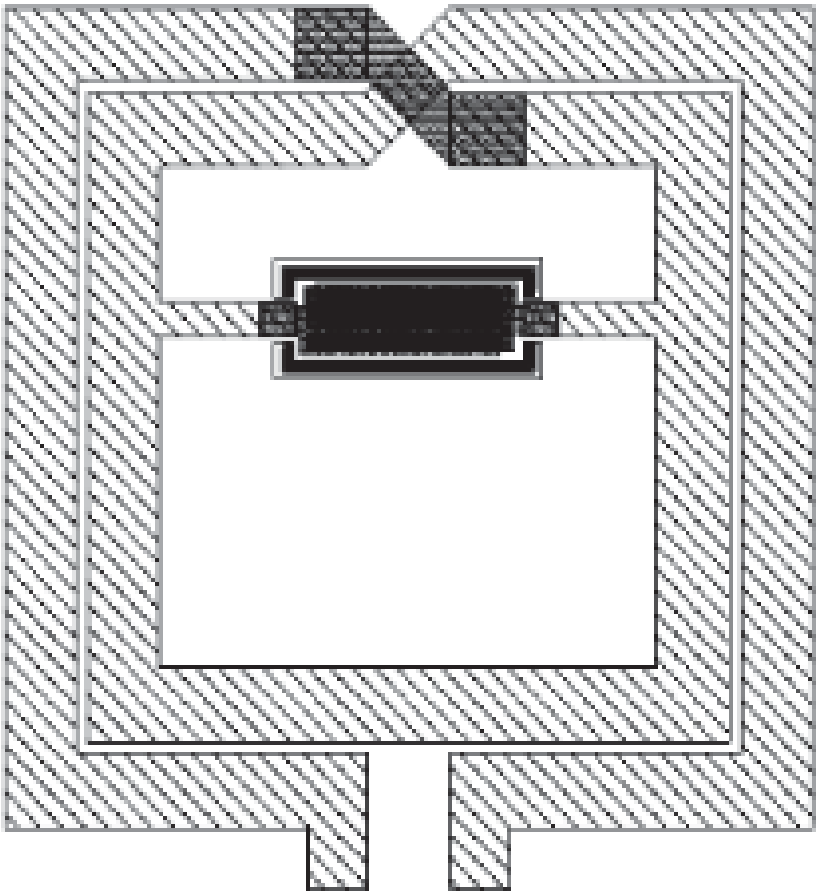

Figure 9 - Variable inductance with switchable internal path (adapted from (SADHU; OMOLE; HARJANI, 2008))

It was also proposed in (AGARWAL; PANDE; HEO, 2015; JIN; WU; XUE, 2018; YOU; HUANG, 2013) the utilization of an outside structure to influence the inductance presented by the inductor. In (AGARWAL; PANDE; HEO, 2015), a shield is switched to operate as a secondary in order to modify the main coil's inductance. When the switch is open, the secondary structure operates as a patterned shield; however, when the switch is closed, a current is induced in a opposite direction to the primary, reducing the overall inductance, as shown in figure 10. This configuration exhibits inductances of 196.2 pH and 146.4 pH, while showing a quality factor of above 15.5.

The same concept is applied in (YOU; HUANG, 2013), except that instead of the substrate shield, a grounded metal guard ring is used as secondary. Finally, (JIN; WU; XUE, 2018) proposed two different secondary coils, one internal to the inductor and the other external; similarly, by choosing the active switches, the secondary coil changes, altering the equivalent inductance presented. In (JIN; WU; XUE, 2018), three different inductances are obtained: 83 pH, 76.3 pH and 70 pH; all exhibiting a quality factor higher than 10 (at 50 GHz).

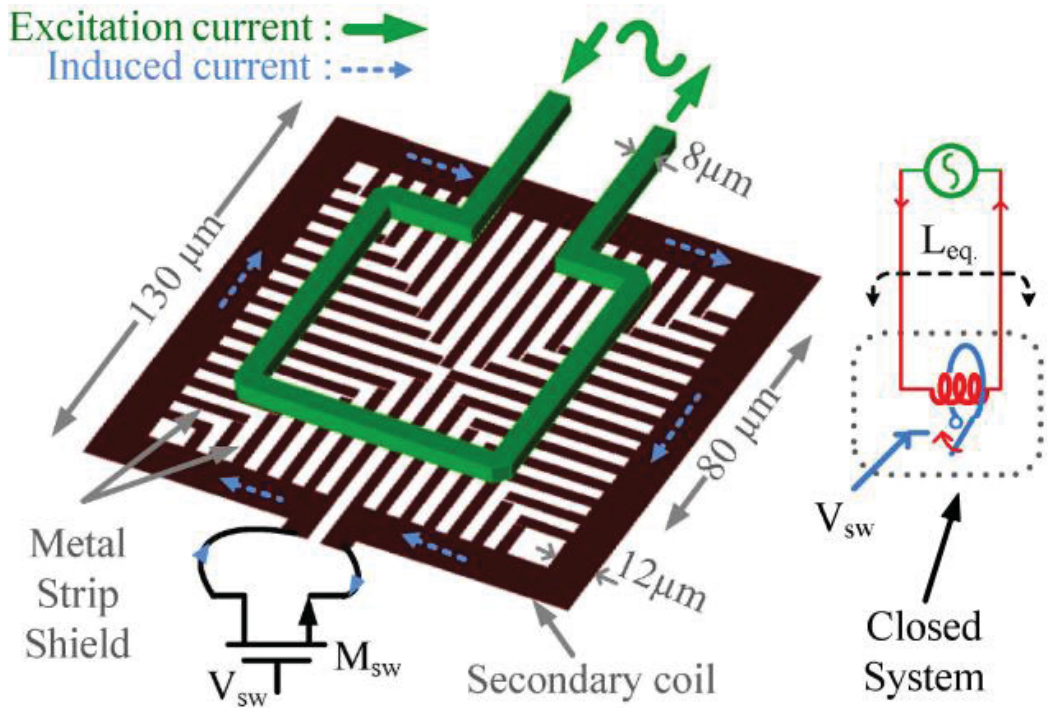

Figure 10 - Variable inductance using a substrate-shield as secondary (AGARWAL; PANDE; HEO, 2015)

Finally, (PENG et al., 2018) proposes a structure comprised of 8 inductors connected through 12 switches, which allows for the selection of different

configurations. Each configuration delivers a different equivalent inductance. Figure 11 shows two different operation modes presented in the work.

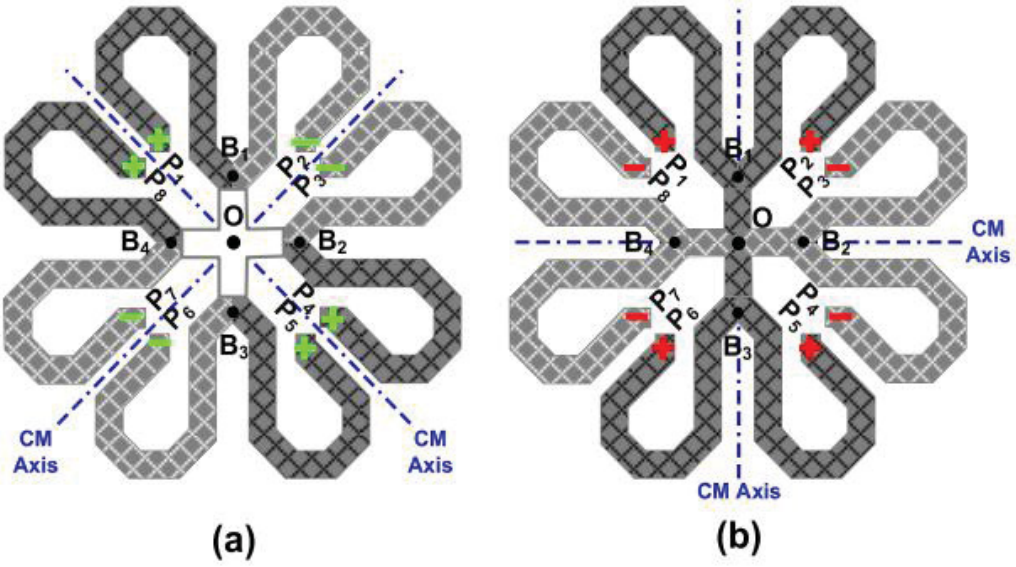

Figure 11 - (a) High inductance mode (b) Low inductance mode (PENG et al., 2018)

2.4 ELETROMAGNETIC SIMULATIONS

The passive elements' results presented in this work derives from electromagnetic simulations. The software utilized is the Advanced Design Systems (ADS) in which the back end of line (BEOL) was implemented from the design kit of the technology. The layers' physical parameters (such as height, conductivity) and placing order above the substrate were imported. Using this ambient setup, the transformers were designed using the top layers (AM and LY).

Three different simulation methods options are provided in the ADS software: finite difference time domain (FDTD), method of moments (MoM) and the finite elements method (FEM), which was the chosen method.

This method separates the full space into smaller tetrahedral regions (identified as elements) and describes the field in each element by a local function. The simulator generates an initial mesh and computes its electric fields and scattering parameters for that mesh at a defined frequency. An error estimative is generated for all of the tetrahedra and the tetrahedron with the largest estimated error is refined in order to create a new mesh that will compute the electric field and scattering parameters one more time. A comparison between the s-parameters from consecutive meshes is then realized and if the difference between the parameters is higher than a

certain threshold, the process is repeated until the difference falls below the defined threshold. In that final mesh, the simulation computes the results for all the other frequencies in the range defined by the user (TECHNOLOGIES, 2010).

The refinement frequency selected was the default suggested by the software (higher frequency simulated), and a meshed interior configuration was chosen since the low frequency range results are important to the analysis and the meshed interior presents a more accurate representation in the aforementioned scenario (SILVA, 2017).

This chapter presented figures of merit utilized to evaluate integrated inductors, shown particular characteristics to transformer implementation in an integrated setting, as well as described the technology utilized in the project. A physics-based model of transformers is presented, and the current scenario pertaining variable inductances is illustrated through exemplification of devices employed in actual circuits. Finally, the chosen electromagnetic simulations methodology procedure is delineated and the more important configuration aspects are indicated.

3 PROPOSED TRANSFORMER-BASED VARIABLE INDUCTANCES

In order to deliver a variable inductance, a switched integrated transformer was chosen. Initially, a compendium containing all the possible connections between a two-coiled transformer's terminals was compiled, followed by the estimation of the theoretical equivalent inductance each configuration would produce. Redundant or invalid configurations were discarded and the remaining were separated into categories in order to facilitate the comprehension of their inner working.

As a starting point, an ideal integrated transformer was used to inspect the formerly evaluated inductances and their practicality in this work. Figure 12 (a) illustrates said transformer and its terminals, while figure 12 (b) its corresponding schematic representation. Terminals 1 and 2 will refer to the primary winding in the transformer, while terminals 3 and 4 to the secondary.

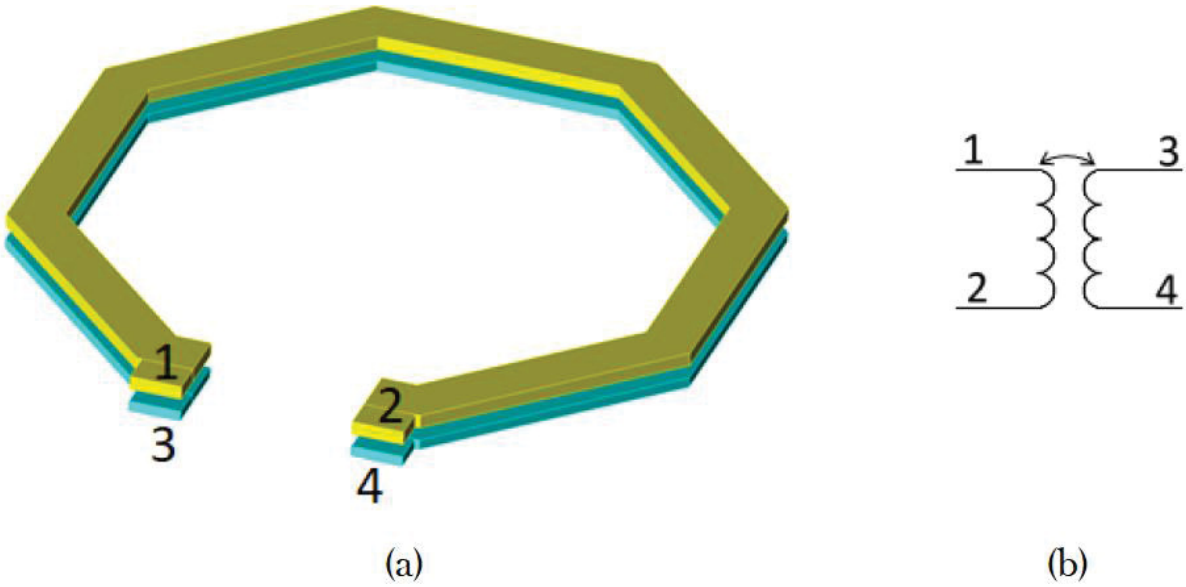

Figure 12 - (a) Layout representation of an integrated transformer (b) Schematic representation

Afterwards, theoretical formulae were proposed to describe the operation that a real transformer would present to each switching configuration. In order to evaluate the hypothesis, a set of specific transformers were designed and their scattering parameters extracted through electromagnetic simulations. In this step, the quality factor presented by the transformers scattering parameters was also analyzed. It was noticed that the lower layer in which the secondary coils is placed, presented a significantly lower quality factor than the primary.

Anticipating an eventual reduction in the overall quality factor (as well as reduction in the self-resonant frequency) caused by the introduction of the switches in

the circuit, it was opted to utilize horizontal coupling since it presents a slightly lower parasitic capacitance between coils and a higher quality factor delivered by the secondary. In order to illustrate the magnitude in the quality factor discrepancy, the transformer in Figure 13 was designed.

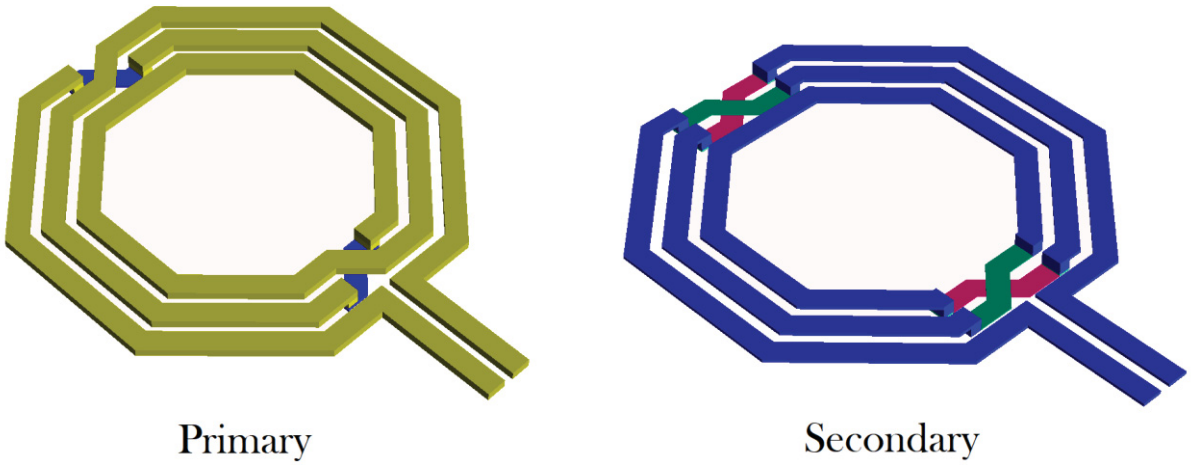

Figure 13 – Windings of the transformer utilized to illustrate quality factor discrepancies

The transformer was subjected to electromagnetic simulations and inductance and quality factor were extracted. The primary and secondary coils present essentially the same dimensions and, therefore, their inductance is practically the same. The only difference between the coils is the layer in which they are implemented. The primary winding is implemented in the AM layer (the highest of the topology), which presents a significant thicker configuration than the LY layer, where the secondary was designed. Figure 14 shows the inductance and quality factor presented by the different windings in this transformer.

The maximum quality factor shown by the primary is 11.5, while the maximum quality factor in the secondary is 7.8, a difference of approximately 32%. This degradation in the quality factor stems from the fact that the LY layer is a lot thinner than the AM layer, which reduces the cross-section of the winding, increasing its internal resistance and, finally, reducing its quality factor. It is possible to notice that there is an effect in the inductance as well, however, it is not as impactful as in the quality factor.

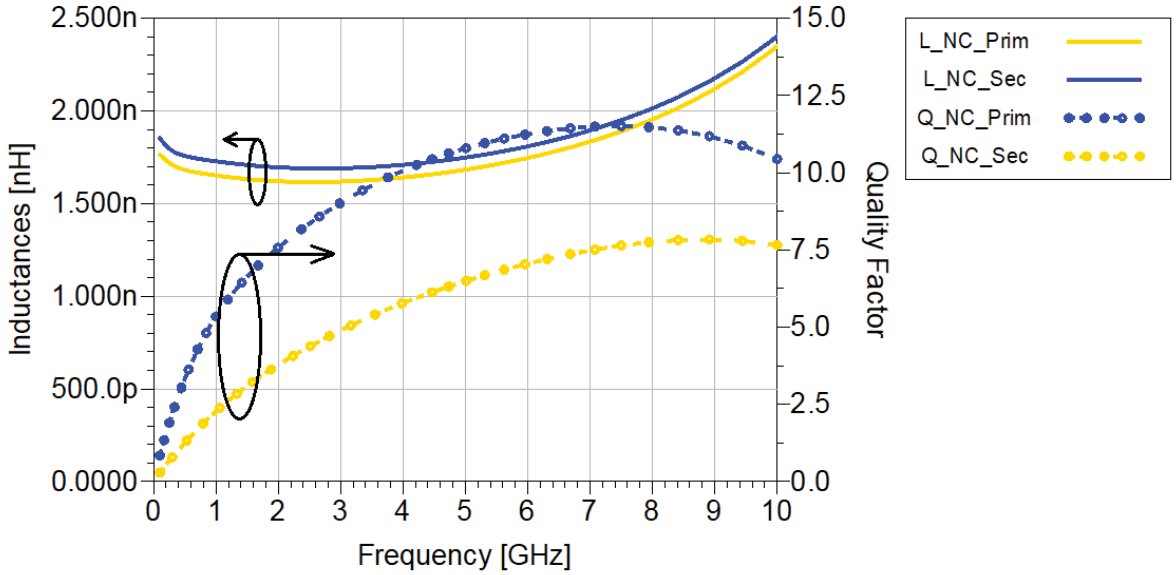

Figure 14 –Inductance and quality factor in different layers obtained from the simulated transformer

The next step was to add the switches to the transformer configuration and analyze its final equivalent inductance, quality factor and self-resonant frequency. Since the switches present a significant *ON* resistance (and *OFF* capacitance) in the context of the transformer, different topologies were studied. Finally, the switches were implemented into the overall structure.

This work proposes a variable inductance utilizing a switched transformer with at least six different configurations depending on the strength of the magnetic coupling in the particular design of the structure. Some technology limitations (such as number of thick layers to design the coils and angle between conductors) as well as theoretical propositions steered the choice for an octagonal symmetric coil configuration utilizing horizontal coupling. A ground shield was included to reduce the eddy current effects in the coils, as well as a ground plane surrounding the overall structure.

3.1 PROPOSED CONFIGURATIONS

As previously mentioned, the proposed configurations were divided into categories, which were interconnected and isolated coils. As the names suggests, interconnected coils refer to configurations that present a connection between the terminals in one of the transformers windings to the other winding. Isolated coils refer to configurations where the winding's terminals are not interconnected.

3.1.1 Interconnected coils

In order to guarantee that all options would be considered, the analysis started off from terminal 1, and all the possible connections between this terminal and the secondary winding terminals (i.e., terminal 3 and 4). Next, the connection between terminal 2 and the secondary winding terminals was also assessed. Lastly, terminals 1 and 3 were connected at the same time that terminals 2 and 4 as well as terminals 1 and 4 connected in the same configuration as 2 and 3.

Figure 15 exhibits the evaluated connections in this step. It is easy to notice that configurations 15(a) and 15(b) relate to the singular connections from terminal 1, whereas 15(d) and 15(e) refers to the singular connections from terminal 2. Finally, configurations 15(c) and 15(f) correlates to a simultaneous connection from terminal 1 and 2 to the secondary winding.

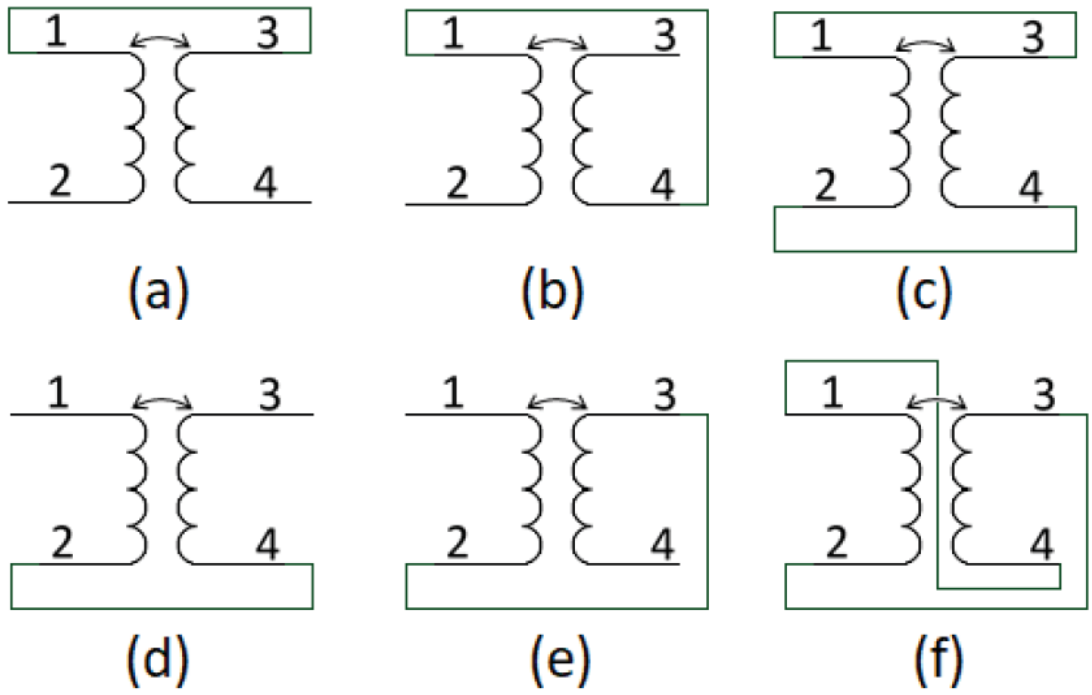

Figure 15 – Evaluated configurations of connections between the windings

In order to obtain an inductance from these configurations, an entry and exit point must be determined. By, isolating and analyzing Figure 15(a), it can be contemplated a diverse combination of entry and exit points. Since transformers are passive elements that do not usually display polarity, inverting the entry and the exit port does not exhibit significative difference in the overall result; with that said, several combinations turn out to be redundant.

The non-redundant possibilities, considering the entry (P1) and exit (P2) ports from Figure 15 (a) and 15 (b) are shown in Figure 16. Since there is not a path to the current to flow in the primary winding, the configurations 16 (a) and 16 (d) do not present a magnetic coupling (analogously, the same can be claimed about configurations 16 (c) and 16 (f). Therefore, theses pairs end up presenting the same equivalent inductance, which would be the secondary's coil inductance for the pair 16 (a) and 16 (d), and the primary's coil inductance for the pair 16 (c) and 16 (f).

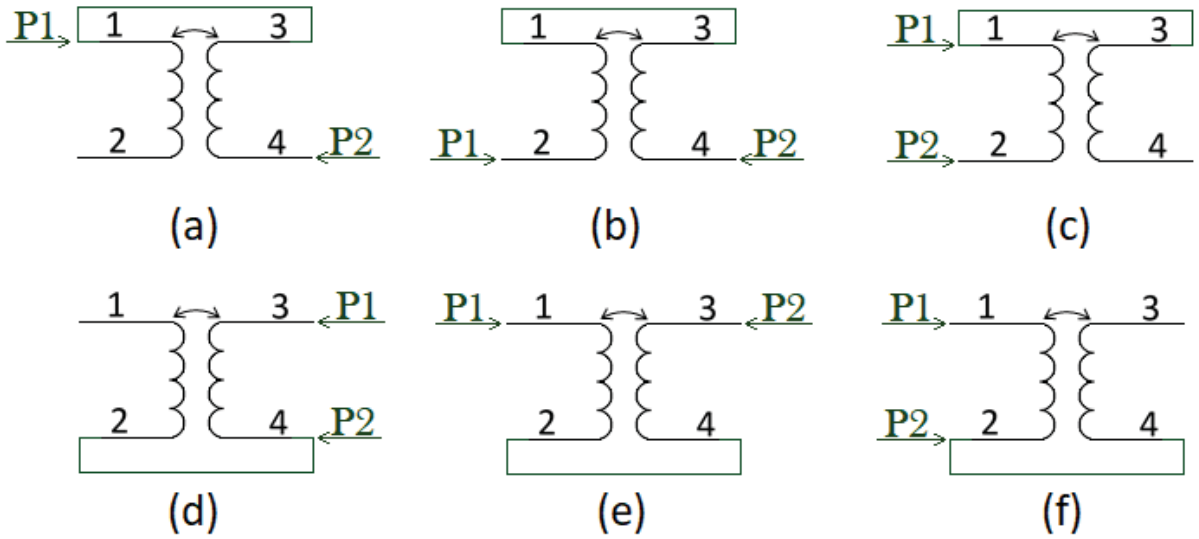

Figure 16 – Different evaluated possibilities in magnetic coupling

Therefore, the configurations that present a magnetic coupling are 16 (b) and 16 (e). Since the current will flow in opposite directions in the transformer's windings, both configurations present a negative coupling and, since they represent the same association between the coils, they ultimately deliver the same equivalent inductance. Figure 17 illustrates the current direction in both coils for both cases.

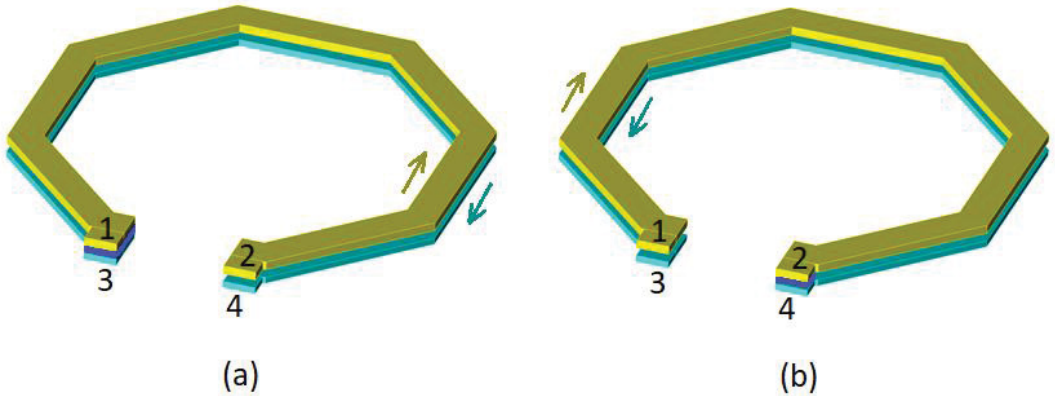

Figure 17 - Current direction in the transformer's windings.

Finally, 8 different configurations could be extracted that retains connections between the primary and secondary windings. These configurations are summarized in table I and most of the configurations presented in this section were simulated in schematic by selecting the desired interconnections between the windings utilizing scattering parameters blocks in order to confirm the expected redundancies.

Table I – Possible configurations for interconnected coils.

Connected Terminals	Input Port	Output Port
1 to 3	1	2
	2	4
	3	4
1 to 4	1	2
	2	3
	3	4
1 to 3 and 2 to 4	1	2
1 to 4 and 2 to 3	1	2

3.1.2 Isolated coils

This section presents the configurations where there is no connection between the primary and secondary windings in the transformer. Also, the redundancy (especially related to the polarity in the ports) is already applied in this case. Therefore, the resulting configurations are presented in Figure 18.

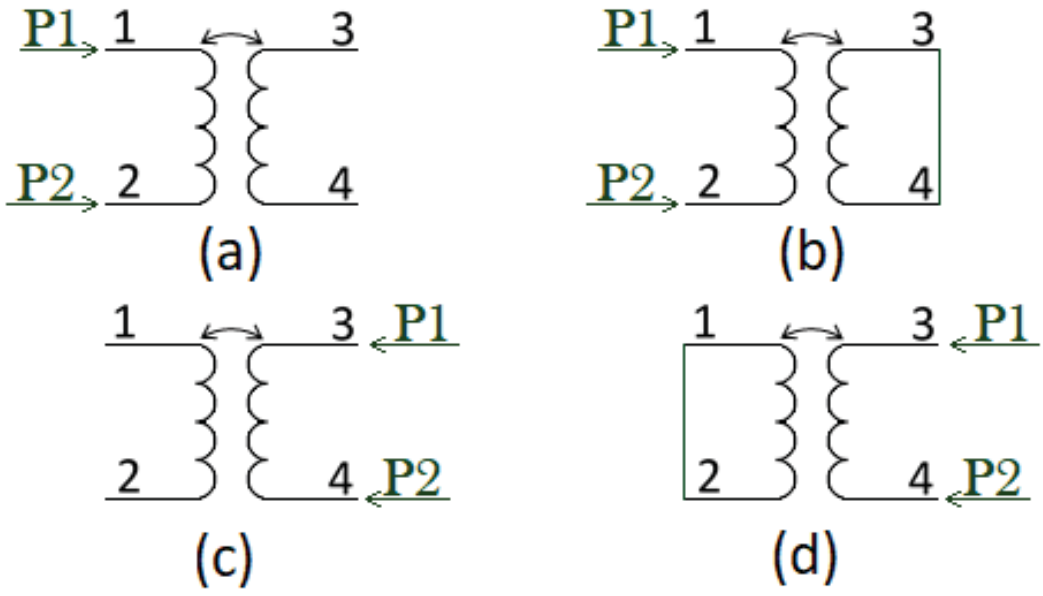

Figure 18 - Isolated coils proposed configurations

It is possible to notice that configurations 18 (a) and 18 (b) extracts the inductance in the transformer's primary winding. However, configuration 18 (b) exhibits a connection between terminals 3 and 4; this connection allows a current to flow through the secondary, which will, in turn, create a mutual inductance between the transformer's coils. This negative coupling is sufficient to produce a distinct equivalent inductance between the configurations. Similarly, configurations 18 (c) and 18 (d) presents the same relationship.

3.2 CHOSEN INDUCTANCES

Once again, a comparison between the 8 configurations with interconnected coils and the 4 with isolated coils, it is possible to eliminate even more redundant options. Specifically, in both cases an equivalent inductance corresponding to the isolated coil inductance was obtained and, therefore, were grouped in the same category. Finally, the 8 unique options displayed in Figure 19 remained. The equations pertaining the selected inductances will be presented in a subsequently section.

The configurations are identified by the type of associations between coils and magnetic coupling conveyed. Configurations 19 (a) and 19 (b) display no extra connections in the transformers, therefore are referred as NC (no connections) and differentiated by the winding they represent (primary or secondary). Similarly, configurations 19 (c) and 19 (d) present a shorted winding and are identified as SC (shorted coil). Once again, both options are differentiated by the winding in which the input and output ports are connected and are labeled Prim_SC or Sec_SC for the primary and secondary winding options.

Next, configurations 19 (e) and 19 (f) connects the primary and secondary winding in a series fashion; in this case, the main difference between the alternatives is the magnetic coupling between coils. Configuration 19 (e) displays a negative coupling, while configuration 19 (f) displays a positive coupling due to the direction of the current flowing through the coils. Therefore, configuration 19 (e) is labeled as Series_N and 19 (f) as Series_P.

Finally, the configurations 19 (g) and 19 (h) associate the primary and secondary as a parallel connection, once again, both configurations are differentiated by their magnetic coupling. Configurations 19 (g) is identified as Parallel_P and 19 (h) is identified as Parallel_N.

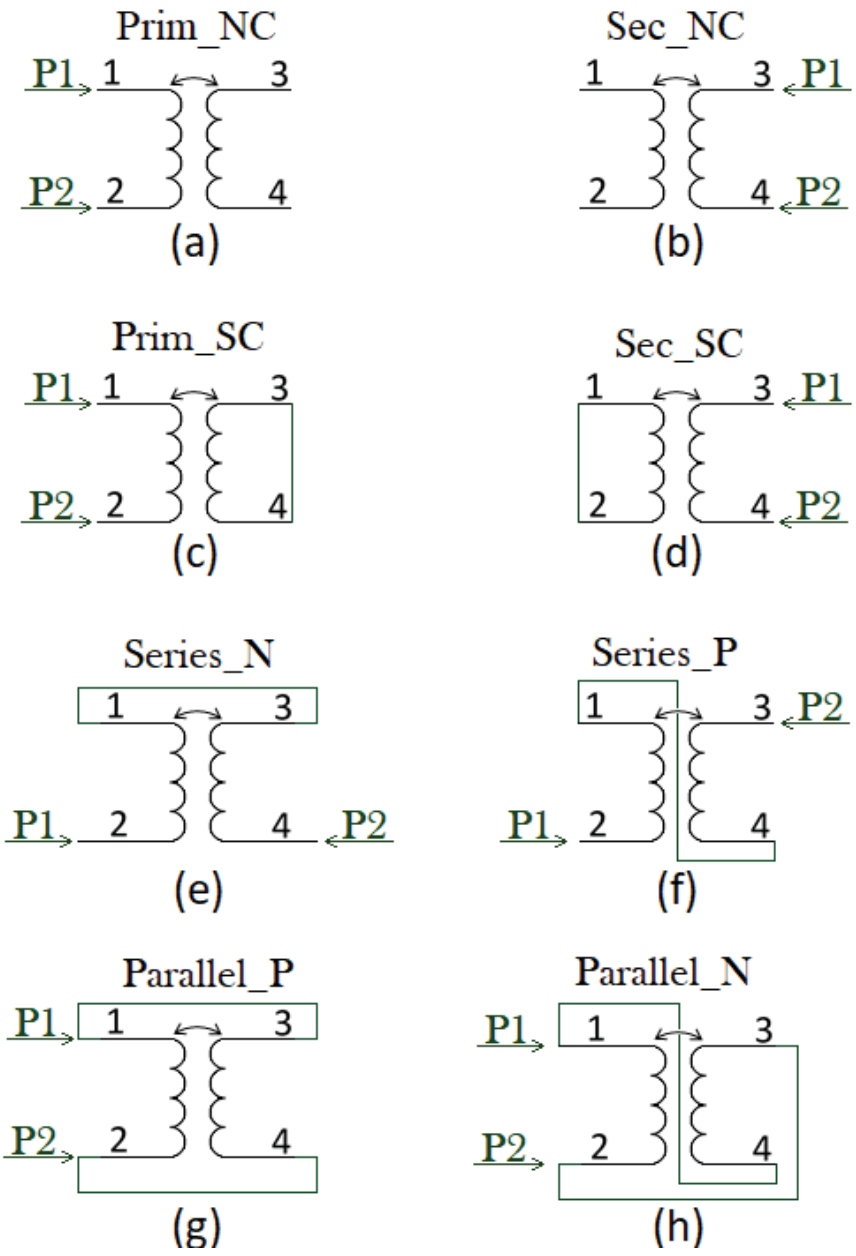

Figure 19 – Proposed configurations

Following the identifications of the configurations, the equivalent inductance calculation was realized and is presented in the next section.

3.3 RESULTING EQUIVALENT INDUCTANCES

In order to evaluate the formulae proposed in this section, an integrated transformer was designed. This transformer (labeled as Transformer 1) was designed with distinct primary and secondary inductances, and a relative weak magnetic coupling due to the horizontal coupling. The designed element is presented in Figure 20, and is formed by an external primary winding with two turns, exhibiting an external

diameter of 300 μm, with a width of 12 μm and spacing between turns of 3 μm; the primary winding refers to terminals 1 and 2 of the transformer. The internal secondary coil also presents two turns, an external diameter of 215 μm, width of 17 μm and spacing between turns of 3 μm; the secondary refers to terminal 3 and 4 of the transformer. Both windings are located in the AM layer, employing a horizontal coupling between the coils. A metallic patterned shield was placed in the lower metal layer (M1) in order to better isolate the substrate to the element. Finally, the transformer was encircled by a reference plane comprised of all the layers in the technology.

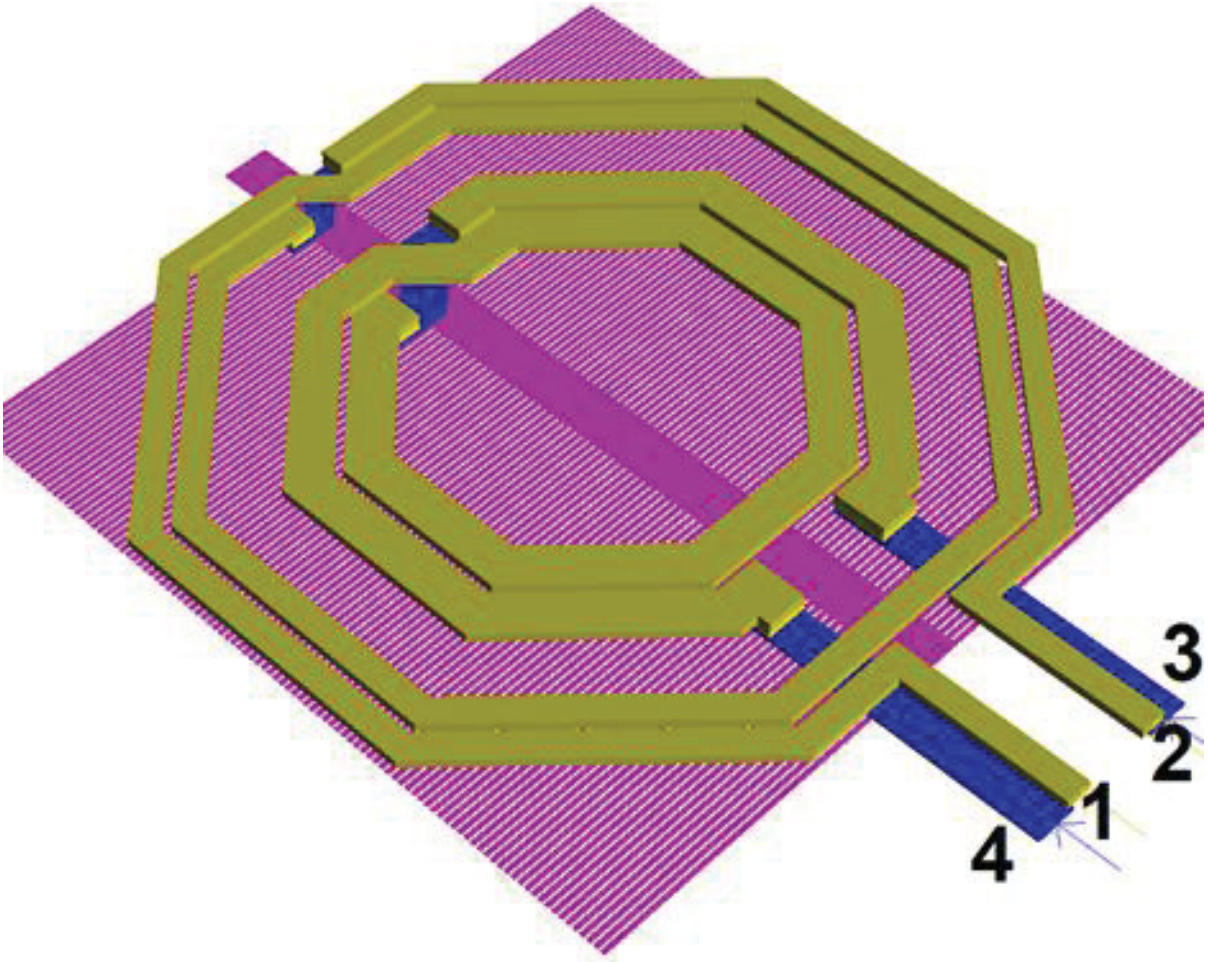

Figure 20 - Designed transformer to evaluate the proposed equivalent inductance formulae

The scattering parameters were extracted from electromagnetic simulations and integrated in a schematic window through an S-parameters block. The self and mutual inductances were extracted and utilized to calculate the equivalent inductance from each configuration; the schematic setup is illustrated in Figure 21. The circuit's ports possess a 50 Ω standard impedance.

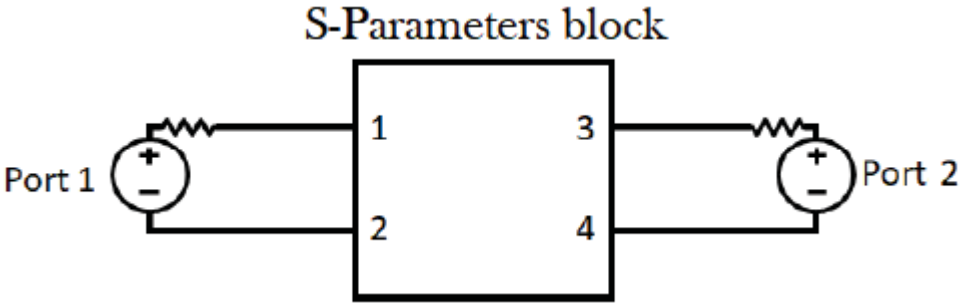

Figure 21 – Schematic simulation configurations setup

The self and mutual inductances were extracted from the simulation results as described by equations (8) through (10):

$$L_{primary} = \frac{imag(Z_{11})}{\omega}, \tag{8}$$

$$L_{secondary} = \frac{imag(Z_{22})}{\omega}, \tag{9}$$

$$M = \frac{imag(Z_{21})}{\omega}. \tag{10}$$

In order to evaluate the equivalent inductance, we refer to the diagram presented in Figure 22.

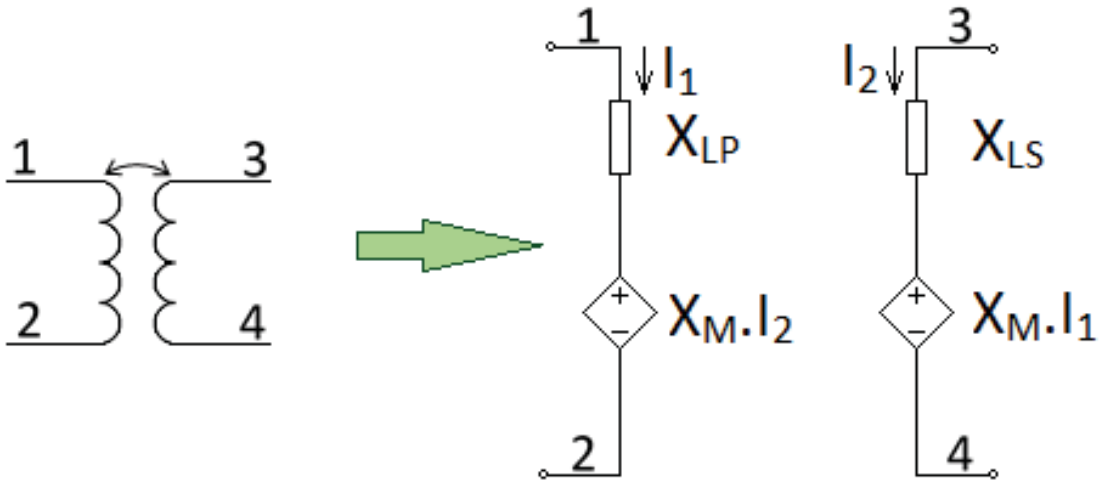

Figure 22 - Diagram illustrating the effect caused by the mutual inductance between coils

We considered the transformer coil as an inductance (represented by its reactance X_L) and the mutual inductance is represented by a voltage source controlled by the current flowing in the adjacent winding (in practical terms, the mutual inductance

corresponds to an inductance relative to the current flowing in the adjacent coil). The magnetic coupling type (positive or negative) rules the polarity in the voltage source in the windings; in case of a positive coupling, the voltage generated by the source follows the currents direction. This diagram is the basis used to determine the equivalent inductance in all of the proposed configurations.

3.3.1 NC configurations

The first set of configurations is the not connected (NC) configurations that sports exactly the diagram presented in Figure 22, where X_{LP} and X_{LS} corresponds to the reactance from the primary and secondary windings respectively, whereas the X_M refers to the reactance corresponding to the mutual inductance. Since there is no current flowing in the adjacent winding, the mutual reactance has no influence in the equivalent inductance presented by this configuration. Since the relationship between inductances and reactances is limited to the multiplication of $j\omega$, extracting the inductance from the denominated reactances is straightforward and, the analysis will observe the inductances directly.

Therefore, the inductance obtained from both NC configurations corresponds solely to the inductance of the winding under analysis, as described in equations (11) and (12):

$$L_{Prim\_NC} = L_{Primary}, \tag{11}$$

$$L_{Sec\_NC} = L_{Secondary} \tag{12}$$

Where $L_{Primary}$ corresponds to the inductance of the primary winding of the transformer and $L_{Secondary}$ corresponds to the inductance of the secondary winding. Consequently, the inductances extracted from the coils in the transformer can easily be plotted against the inductances produced by equations (11) and (12) in Figure 23, where the data obtained through direct simulation (i.e, simulating the s-parameters block in the variable inductance's structure configuration under analysis) is identified by the _FEM label. The data obtained through the formulae presented in this work in conjunction to the parameters extracted from the transformer's electromagnetic simulations are labeled as _calc (as in calculated). Obviously, in this case, there is an 100% accuracy, since the configuration's inductance is exactly the same as the primary (or secondary) inductances.

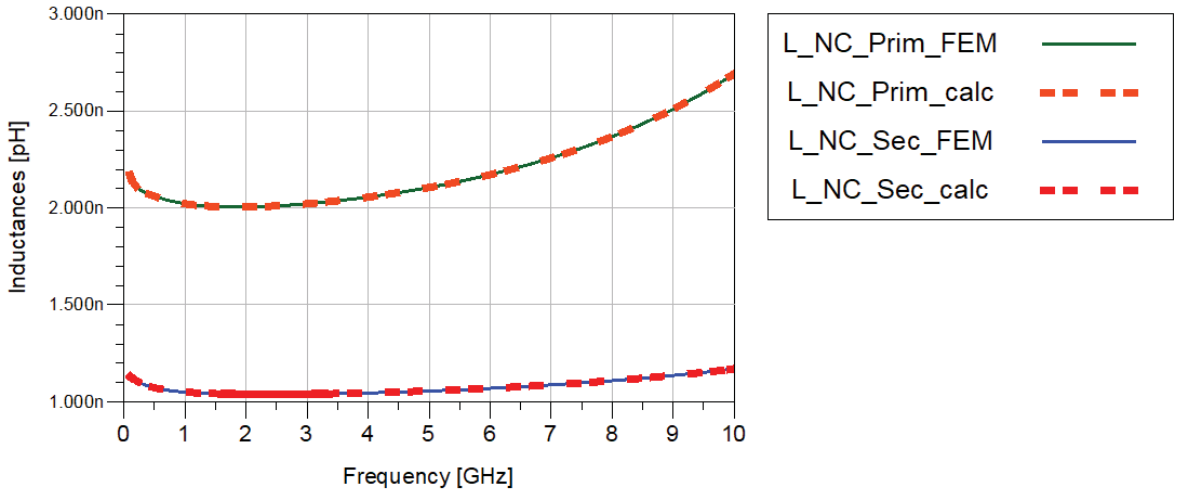

Figure 23 - Calculated vs simulated inductances for the NC configurations

3.3.2 SC configurations

This configuration connects both terminals in the adjacent coil, as illustrated in Figure 24. In this case, the current in the secondary winding has a path to flow, which causes the magnetic flow to appear in the secondary, which affects the equivalent inductance presented in the primary. The mutual inductance effect is illustrated by the voltage-controlled source present in each winding. The voltage generated is a function of the mutual reactance between the transformer's coils.

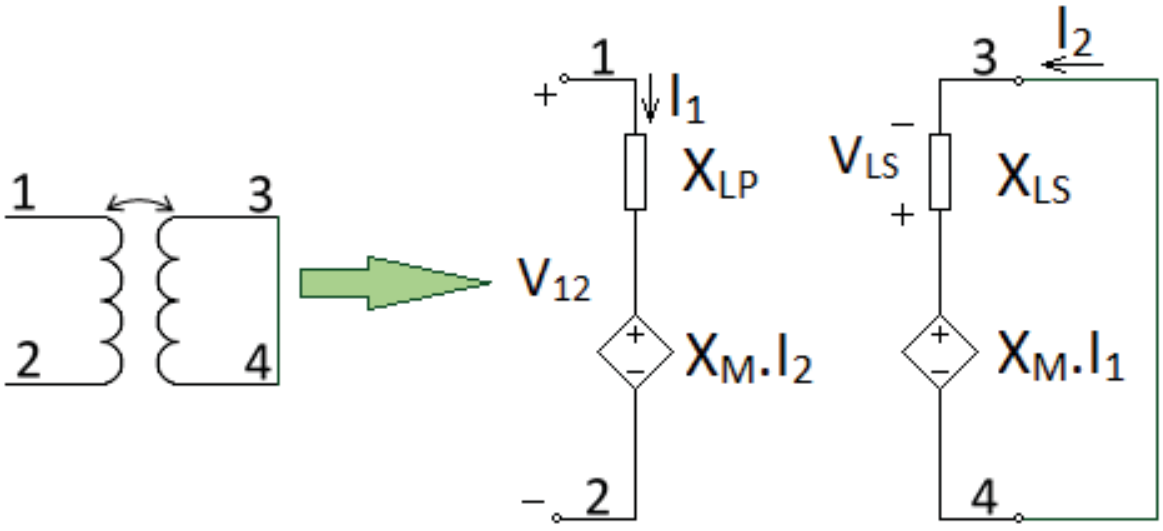

Figure 24 - SC configurations diagram

Through circuit analysis, it is possible to infer that the voltage in X_{LS} is the same voltage generated by the controlled source. In the primary, the voltage between

terminals 1 and 2 is the sum of the voltage over X_{LP} and the controlled source voltage. Therefore, we reach equations (13) and (14):

$$V_{LS} = X_{LS}.I_2 = X_M.I_1, \quad (13)$$

$$V_{12} = X_{LP}.I_1 - X_M.I_2 \quad (14)$$

Isolating the current flowing in the secondary I_2 in equation (13) and replacing it in equation (14) allows us to reach the resulting inductance for this configuration (Prim_SC), shown in equation (15). Analogously, equation (16) shows us the inductance presented in the configuration Sec_SC.

$$L_{Prim\_SC} = L_{Primary} - {M^2}/{L_{Secondary}}, \quad (15)$$

$$L_{Sec\_SC} = L_{Secondary} - {M^2}/{L_{Primary}}. \quad (16)$$

Once again, the calculated inductances for both configurations were plotted against the extracted from the schematic, which is shown in Figure 25. The calculated inductance is identified as L_SC_Prim_calc (for the primary winding) and L_SC_Sec_calc (for the secondary). Similarly, the extracted data from the electromagnetic simulation s-parameters block schematic configuration is labeled as L_SC_Prim_FEM for the primary winding and L_SC_Sec_FEM for the secondary.

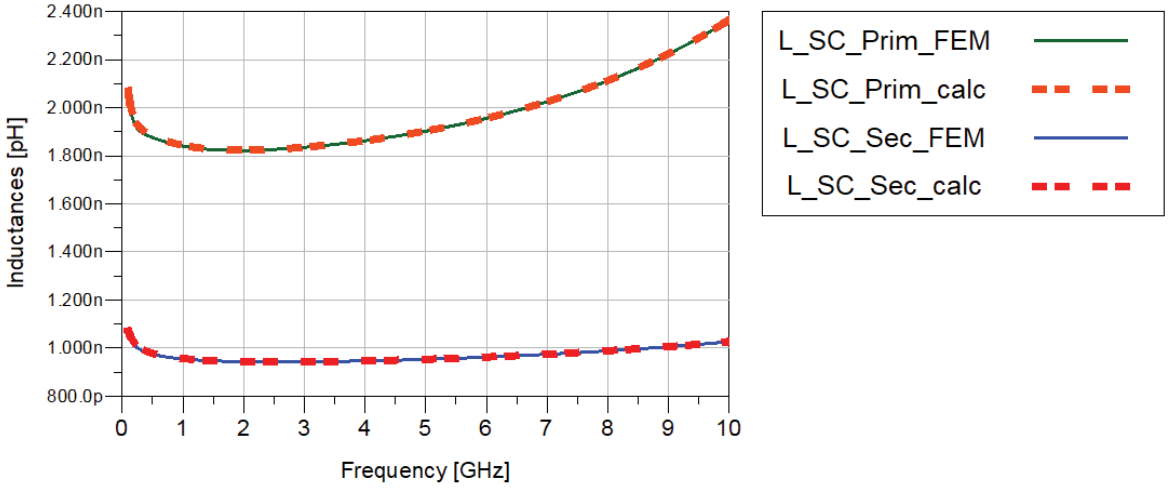

Figure 25 - Calculated vs simulated inductances for the SC configurations

3.3.3 Series Configuration

As with other configurations, the series structure allows for two different types of configurations. In this case, however, the difference between both series configurations is not the winding from where the inductance is extracted, but the type of magnetic coupling between the coils. Depending on the terminals connected it is possible to generate a positive or negative magnetic coupling between the transformer's windings. Figure 26 exhibits the Series_N configuration (i.e., the one with a negative magnetic coupling); the same principles can be applied to Series_P, however the magnetic coupling must be adjusted.

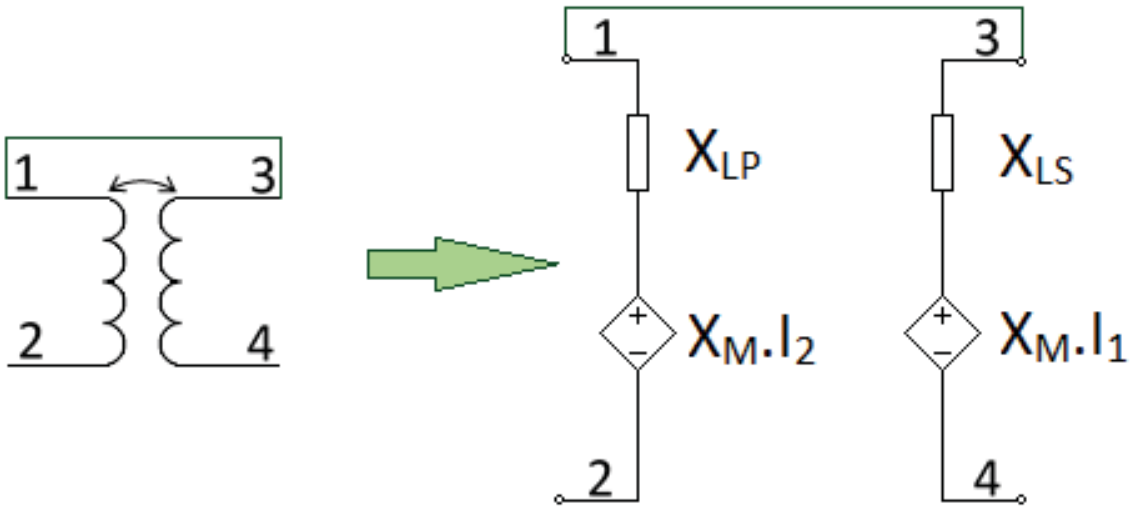

Figure 26 -Series_N configuration diagram

Since both coils are connected in series, the current that flows through the primary winding is the same as the current flowing through the secondary; therefore, the resulting inductance is simply the sum between all of the inductances present in the element, which gives us equations (17) and (18) that describes the series configurations equivalent inductance:

$$L_{Series\_N} = L_{Primary} + L_{Secondary} - 2M, \quad (17)$$

$$L_{Series\_P} = L_{Primary} + L_{Secondary} + 2M. \quad (18)$$

Easily enough, the only difference between the positive and negative coupling in this case is the mutual inductance signal, where the positive coupling contributes positively to the total inductance of the configuration while the negative coupling

configurations exhibits a negative contribution to the equivalent inductance from the mutual inductance.

The calculated and simulated inductances for the series configurations are presented in Figure 27. It is easy to notice that the proposed formulae describe the operation of the aforementioned configuration quite accurately. However, in the positive coupling scenario, a noteworthy divergence between the proposed formula and the extracted data starts to arise. This is mainly explained by the lower self-resonant frequency this configuration exhibits and, since the configuration formula does not account for the parasitic capacitance present in the transformer, it is natural for this discrepancy to appear. Nevertheless, the presented formula does a satisfactory job in predicting the operation in the final structure.

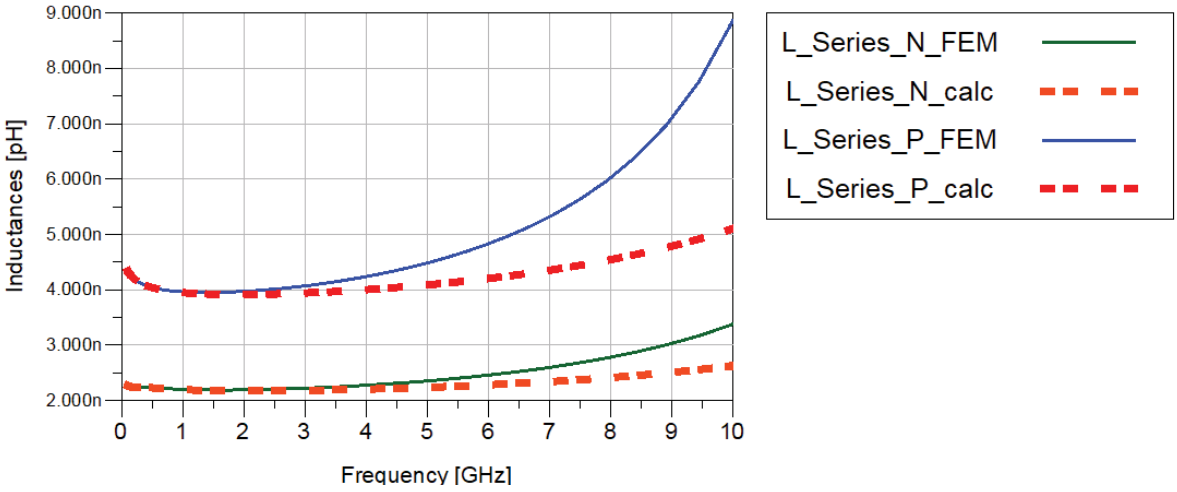

Figure 27 - Calculated vs simulated inductances for the Series configurations

3.3.4 Parallel Configurations

Lastly, the parallel configurations diagram is presented in Figure 28. This configuration requires two connections between the windings; as with the series configurations, the parallel case exhibits two distinct modes differentiated by the magnetic coupling generated from the connections between the windings. For this example, the Parallel_P configuration is represented.

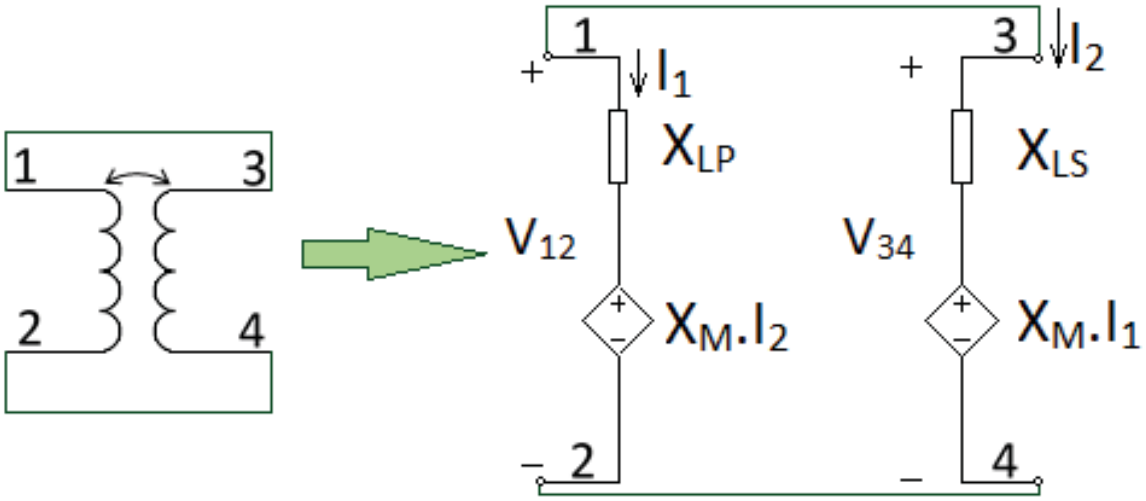

Figure 28 -Parallel_P configuration diagram

Due to the parallel structure this configuration exhibits, the voltage between terminal 1 and 2 is the same as between terminals 3 and 4. This voltage is represented by the sum of the voltage drop in the winding reactance and the voltage generated by the controlled voltage source as illustrated by equation (19):

$$V_{12} = X_{LP}.I_1 + X_M.I_2 = V_{34} = X_{LS}.I_2 + X_M.I_1. \quad (19)$$

The primary winding reactance (referred as X_{LPrim}) can be extracted from equation (19), by dividing V_{12} by the current flowing in the path of the terminals 1 and 2 (I_1). Through algebraic manipulations, we can infer not only the primary winding reactance, but also the secondary winding resulting reactance (reffered as X_{LSec}) as in equations (20) and (21):

$$X_{LPrim} = \frac{X_{LPrimary}.X_{LSecondary} - {X_M}^2}{X_{LSecondary} - X_M}, \quad (20)$$

$$X_{LSec} = \frac{X_{LPrimary}.X_{LSecondary} - {X_M}^2}{X_{LPrimary} - X_M}. \quad (21)$$

In order to obtain the configuration's equivalent inductance, the parallel operation is realized between both reactances and, finally, the Parallel_P, as well as Parallel_N, configurations' inductances can be described by equations (22) and (23) as:

$$L_{Parallel\_P} = \frac{L_{Primary} . L_{Secondary} - M^2}{L_{Primary} + L_{Secondary} - 2M}, \quad (22)$$

$$L_{Parallel\_N} = \frac{L_{Primary} . L_{Secondary} - M^2}{L_{Primary} + L_{Secondary} + 2M}, \quad (23)$$

It is possible to notice that the only difference between the equivalent inductances presented is the signal in the 2M factor in the equation's denominator. The calculated and simulated inductances from the parallel configurations were also plotted for the aforementioned transformer. These results are presented in Figure 29.

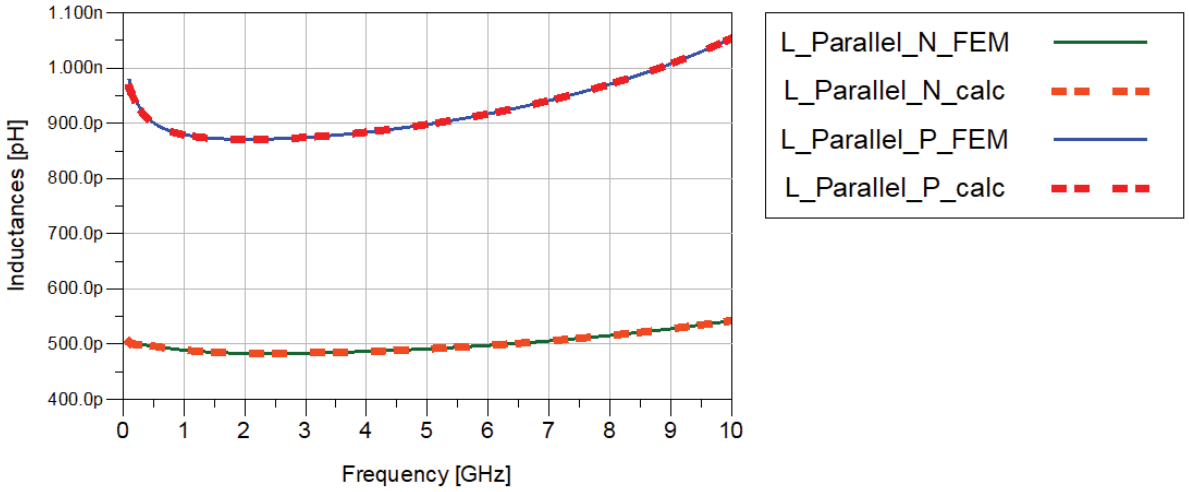

Figure 29 - Calculated vs simulated inductances for the Parallel configurations

In some instances, it may be possible to notice a significative discrepancy in the Parallel_N simulated and calculated inductance, this happens due to the simplicity of the model utilized to describe the parallel behavior of the transformer (a simple reactance for each winding and the magnetic coupling).

In this case, the utilization of a slightly more complex model (such as considering each winding as an inductance in series with the internal resistance of the coil) can improve the accuracy of the model, which results in the more complex equation (24):

$$L_{Parallel\_N} = \frac{imag\left[\frac{(R_{Prim}+j.\omega.L_{Prim}).(R_{Sec}+j.\omega.L_{sec})+M^2\omega^2}{R_{Sec}+R_{Prim}+(L_{sec}+L_{Prim}+2.M).j.\omega}\right]}{\omega} \quad (24)$$

All of the presented curves confirm that the proposed formulae deliver a satisfying accuracy to the extracted transformer data. However, designing the coils and magnetic coupling of the transformer could be a laborious task, since the results depend on electromagnetic simulations in order to evaluate the operation of the overall structure. The utilization of a predictive model of the transformer could easily help to alleviate this task. Also, by inspecting the presented formulae, it is possible to extract valuable information about the operation of each configuration.

Despite presenting 8 possible configurations, in order to take advantage of all of them in one single structure would require a significant number of switches. As aforementioned, the inclusion of switches significantly degrades the quality factor (by adding a parasitic resistance) and the self-resonant frequency (by adding a parasitic capacitance). It was weighted that utilizing 3 different switches in order to access 6 valid configurations was the best compromise in this case. The overall switching structure is presented in the next section.

3.4 PROPOSED STRUCTURE

The main focus of this work is to propose a transformer-based variable inductance. As previously mentioned, a switching composition between different terminals of the transformers is used to control the equivalent inductance presented by the proposed structure. Also, 8 different possible configurations were presented; however, in the proposed structure, only 6 of them achievable. The overall switching diagram is presented in Figure 30.

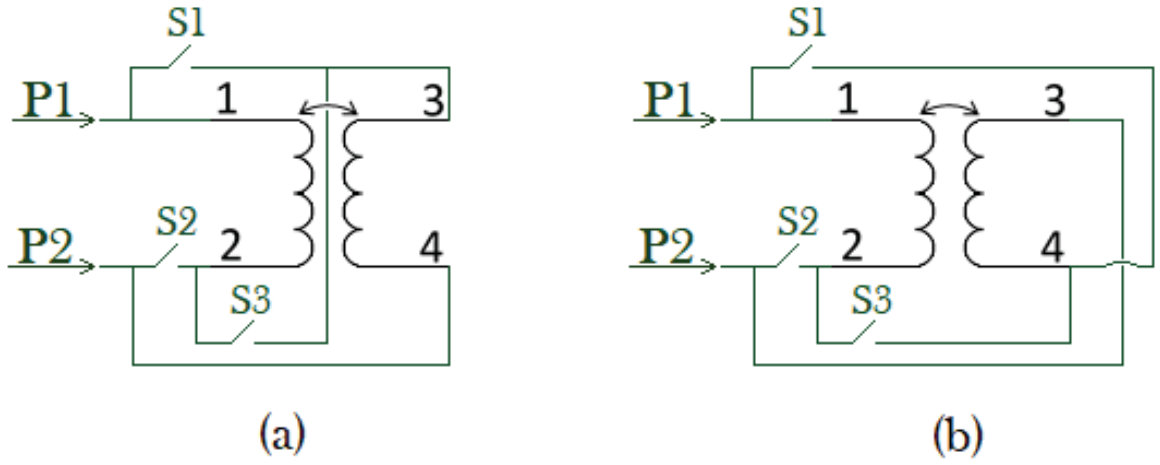

Figure 30 - Proposed variable structures (a) Positive Coupling Structure (b) Negative Coupling Structure

The main difference between the structures presented in Figure 30 is the magnetic coupling between the transformer's coils. In Figure 30 (a), the structure presents a positive magnetic coupling, while in Figure 30 (b) the magnetic coupling is negative. A visual representation of the magnetic coupling from the structure shown in Figure 30 (a) is detailed in Figure 31.

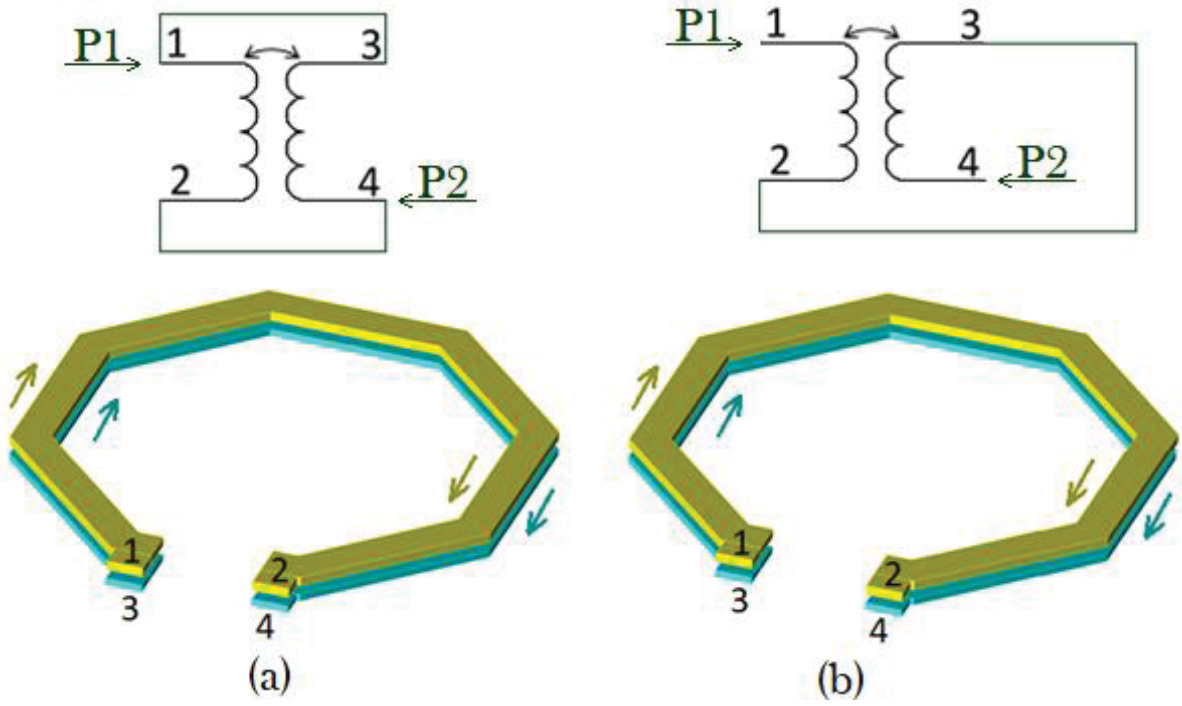

Figure 31 – Positive Coupling Structure current flow (a) Parallel Configuration (b) Series Configuration

In the parallel configuration exemplified in Figure 31 (a), terminals 1 and 3 are connected to each other and correspond to the input terminal of the overall structure, while terminals 2 and 4 are interconnected and represent the output terminal of the structure; this configuration equates to switches S1 and S2 being closed and switch S3 being open. It is noticeable that the current flowing in both windings has the same direction, which implies in a positive magnetic coupling.

In the series configuration, terminals 2 and 3 are connected to each other, while terminals 1 and 4 corresponds to the input and output terminals in the configuration. This setup has switches S1 and S2 being open and switch S3 being closed. Once again, a simple analysis of the current flow direction in each coil shows us the positive magnetic coupling in the structure. Therefore, the possible modes that the structures can achieve and the switching arrangement are summarized in table II.

Table II – Possible configurations attainable to each structure

Switch 1	Switch 2	Switch 3	Configuration
OPEN	OPEN	OPEN	Non-functional
OPEN	OPEN	CLOSED	Series
OPEN	CLOSED	OPEN	Prim_NC
OPEN	CLOSED	CLOSED	Prim_SC
CLOSED	OPEN	OPEN	Sec_NC
CLOSED	OPEN	CLOSED	Sec_SC
CLOSED	CLOSED	OPEN	Parallel
CLOSED	CLOSED	CLOSED	Non-functional

It is important to reiterate that, both switching structures can deliver all six configurations from table II; however, depending on the chosen structure, the magnetic coupling delivered by the Series and Parallel configurations will differ.

In order to illustrate the results obtained in each structure, the equivalent inductance from each configuration was plotted and is shown in Figure 32. The solid line curves represent configurations that can be reached by both structures, the dotted curves represent configurations that can only be delivered by the negative coupling structure and the curves with circle identifications represent the configurations present in the positive coupling structure.

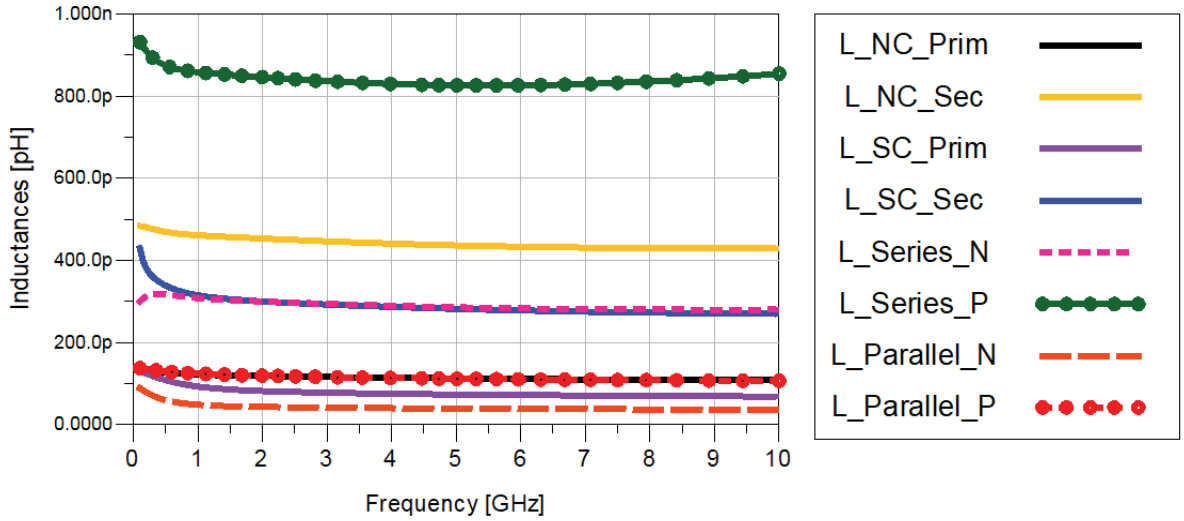

Figure 32 – Finite Elements Method's simulated equivalent inductances from transformer 1 employed in the proposed structure.

Analyzing the curves, it is possible to notice that some configurations present a very similar value of inductances. This can be altered by changing the magnetic coupling in a structure. A transformer with a relative higher magnetic coupling (such as

transformer 1) also can present similar inductances in different configurations; one example is the configurations L_Series_N and L_SC_Sec, as well as L_NC_Prim and L_Parallel_P in transformer 1.

Usually, transformers with low magnetic coupling presents a similar inductance between L_NC_Prim and L_SC_Prim, and also L_NC_Sec and L_SC_Sec (which is expected due to the nature of these configurations). In order to illustrate this, Figure 33 shows the possible equivalent inductances in a transformer with a very low magnetic coupling. It is also noticeable that, in this case, the magnetic coupling does not impact as much the Series and Parallel configurations, since they appear much closer than in the previous case.

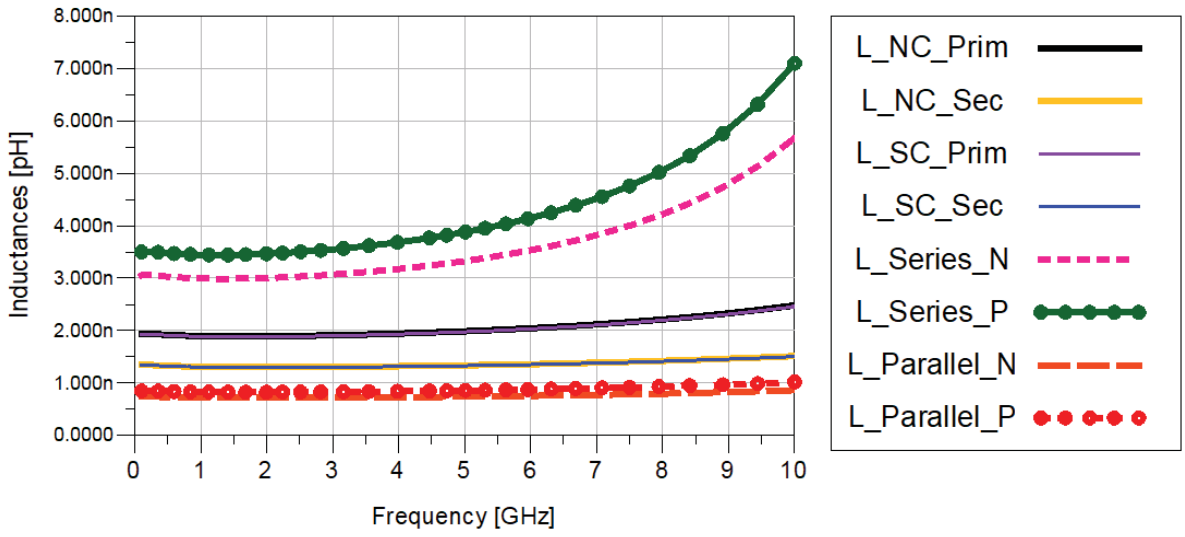

Figure 33 – Example of low a magnetic coupling transformer's equivalent inductance

The magnetic coupling is not the only factor that influences the correlation between the equivalent inductance in distinct configurations. These similarities can also spring from the relationship between the inductance of the primary and secondary coils.

Taking in consideration the previously mentioned formulae that describes the equivalent inductance in each configuration, it is possible to predict the resulting inductance from each configuration analyzing the relationship between the transformer's primary and secondary coils inductances and magnetic coupling. In order to illustrate this, it is plotted in Figure 34 the calculated equivalent inductance for each configuration employing the aforementioned equations and considering the transformer's parameters (i.e., $L_{Primary}$=2 nH and k=0.3). By varying the ratio between

the secondary and primary coils inductance, we can infer the equivalent inductance for each mode of operation.

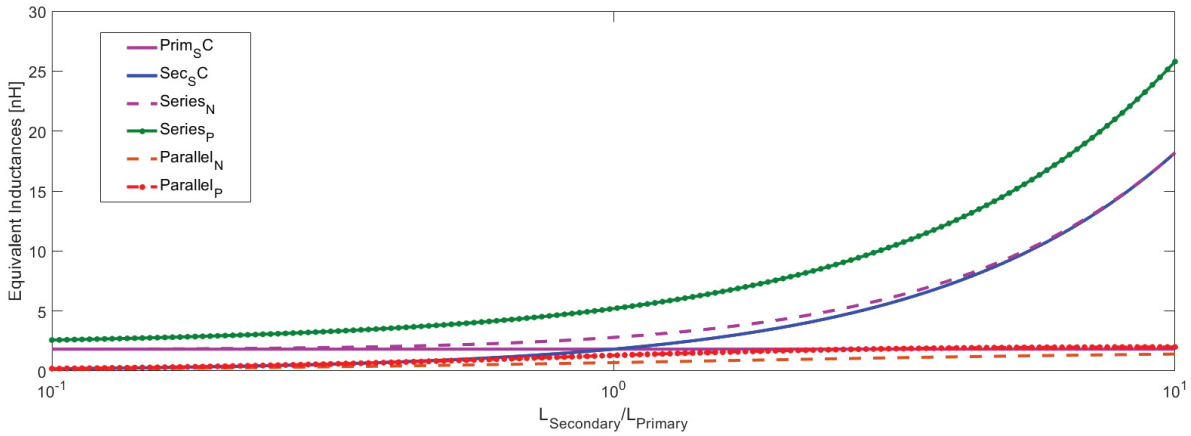

Figure 34 - Transformer 1 configuration's equivalent inductances vs windings inductance ratio

In this case, the ratio ranged from 0.1 to 10, in order to presume the best inductance in the secondary winding to fit the desired application. It is possible to notice that when the ratio $L_{Secondary}/L_{Primary}$ is close to 1, several configurations coincide their equivalent inductance which limits the possible variations delivered by the transformer.

Obviously, this analysis lacks some criteria, especially since that altering the secondary coil will fatally modify the magnetic coupling between the windings. However, it can shed some light into the overall operation of the proposed configurations. Moreover, it is possible to speculate a fixed ratio between the secondary and primary inductances, design those coils separately and, finally, adjust the magnetic coupling by moving said inductances in relation to each other in order to fit the desired magnetic coupling.

By utilizing transformer's 1 primary and secondary coils inductances (2 nH and 1.038 nH, respectively), it is possible to calculate the equivalent inductance for each configuration versus the magnetic coupling factor, which is presented in Figure 35. This analysis illustrates the range of equivalent inductances available in the proposed structures.

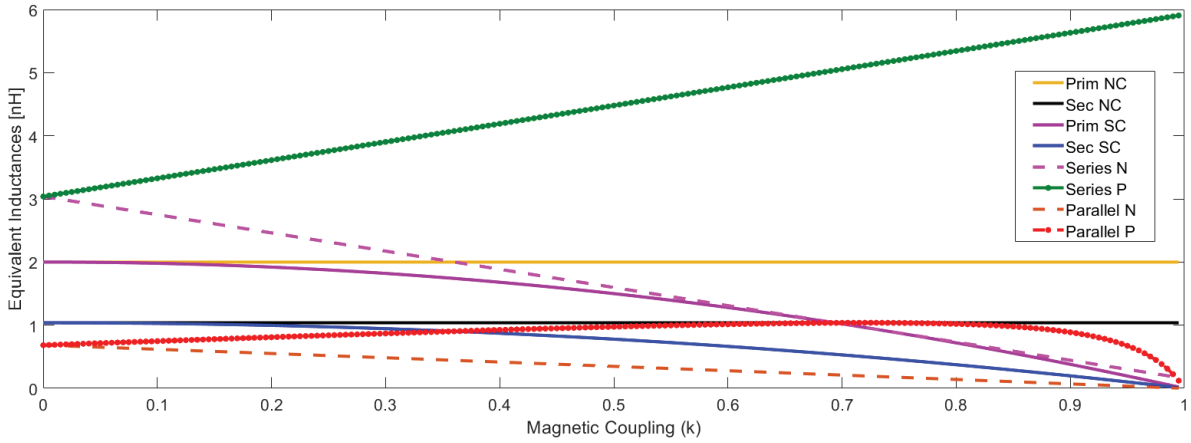

Figure 35 – Transformer 1 equivalent inductances vs magnetic coupling

This analysis shows all the potential equivalent inductances in a magnetic coupling ranging from 0 to 1 (the theoretical maximum range). As a side note, there is an advantage to utilizing vertical coupling in this case, since it would allow for a higher coupling factor than the 0.3 presented by the horizontal coupling topology, which limits the range of possible magnetic coupling factors to work with. However, as previously mentioned, the vertical coupling was discarded due to other technology limitations.

It is also possible to normalize the equivalent inductances from $L_{Primary}$ and analyze the equivalent inductance directly as the ratio (A) between $L_{Secondary}$ and $L_{Primary}$. The formulae presented in section 3.3 can be modified and be described as:

$$L_{Prim\_SC\_norm} = 1 - k^2, \tag{25}$$

$$L_{Sec\_SC\_norm} = A.(1 - k^2), \tag{26}$$

$$L_{Series\_N\_norm} = 1 + A - 2.k.\sqrt{A}, \tag{27}$$

$$L_{Series\_P\_norm} = 1 + A + 2.k.\sqrt{A}, \tag{28}$$

$$L_{Parallel\_N\_norm} = \frac{A.(1 - k^2)}{1 + A + 2.k.\sqrt{A}}, \tag{29}$$

$$L_{Parallel\_P\_norm} = \frac{A.(1 - k^2)}{1 + A - 2.k.\sqrt{A}}, \tag{30}$$

This analysis clarifies the dependence that the proposed configurations have between one another; also, these equations can be assimilated in a contour plot to present an overall picture of the equivalent inductances delivered by each configuration, measuring from the magnetic coupling factor and the ratio between both coils' inductances.

Figure 36 presents a colored mapping of the resulting inductances for configurations PRIM_SC and SEC_SC. Simply enough, it is possible to notice in Figure 36 (a) that the ratio between the inductances does not play any part in the PRIM equivalent inductance, only the magnetic coupling. Moreover, the coupling factor is seen heavily affecting the equivalent inductance in the PRIM_SC and SEC_SC configurations.

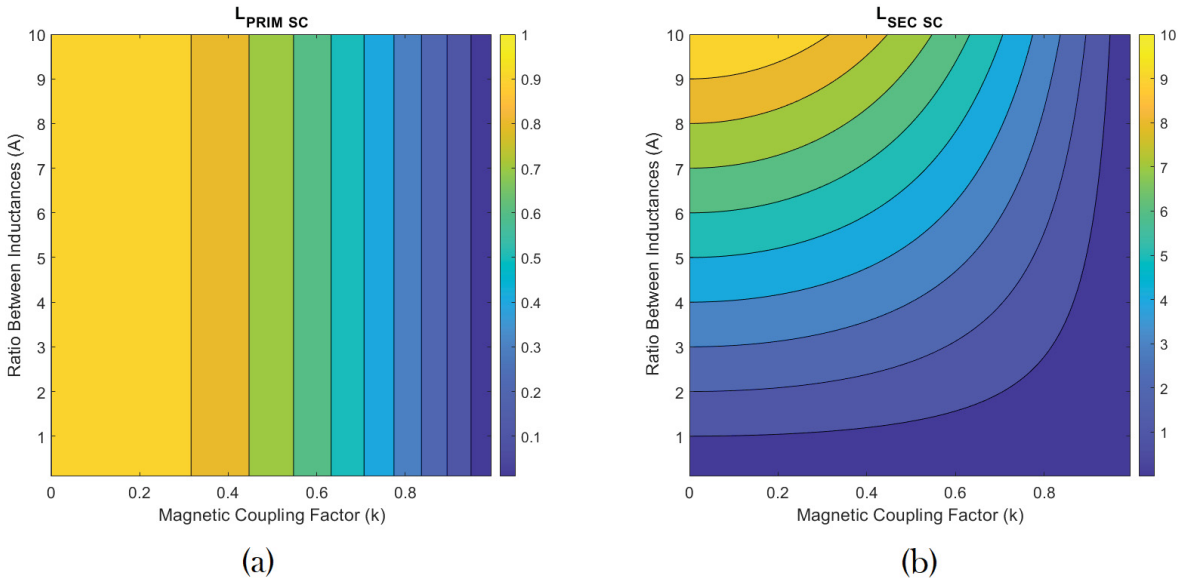

Figure 36 – Colormap representation of the equivalent inductances delivered by PRIM_SC and SEC_SC configurations

A colored mapping of the series configurations is shown in Figure 37. Once again, it is easy to visualize the effects of the magnetic coupling and inductance ratio between coils in each configuration. Since the Series_N configuration possess a negative magnetic coupling, reducing its coupling increases the equivalent inductance. Analogously, by increasing the magnetic coupling in the Series_P configuration, raises the equivalent inductance provided.

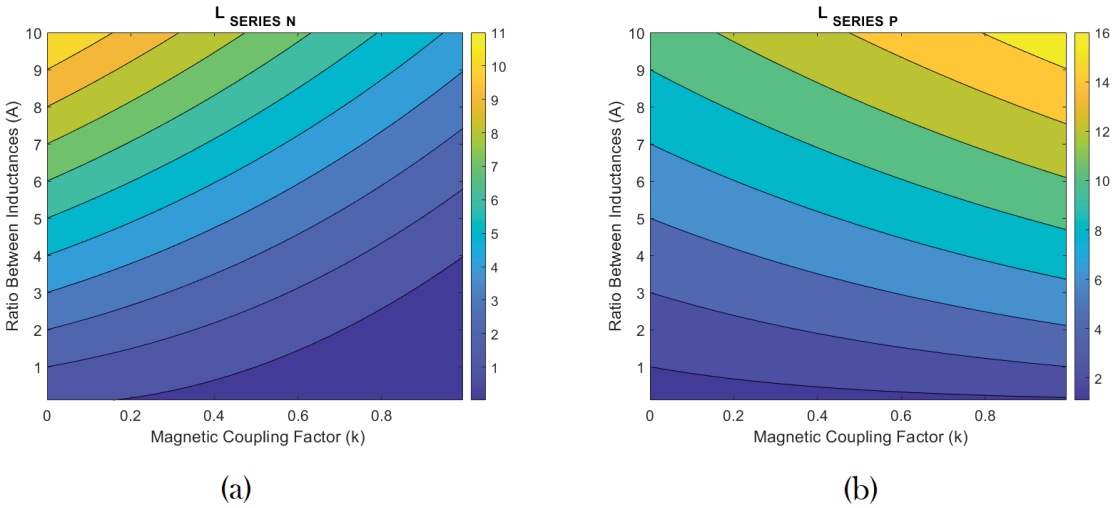

Figure 37 - Colormap representation of the equivalent inductance delivered by Series_N and Series_P configurations

Finally, Figure 38 exhibits the colored mapping of the parallel configuration. An important point to highlight is the inability to reach an inductance higher than the primary inductance in these configurations. The Parallel_P present a large range in which it comes close to 0.9 times the primary inductance, but never surpasses it. Moreover, an interesting response is identified in the colormap of the Parallel_P configuration: from a certain point, maintaining the magnetic coupling factor and increasing the ratio between coil inductances, reduces the equivalent result presented by this configuration.

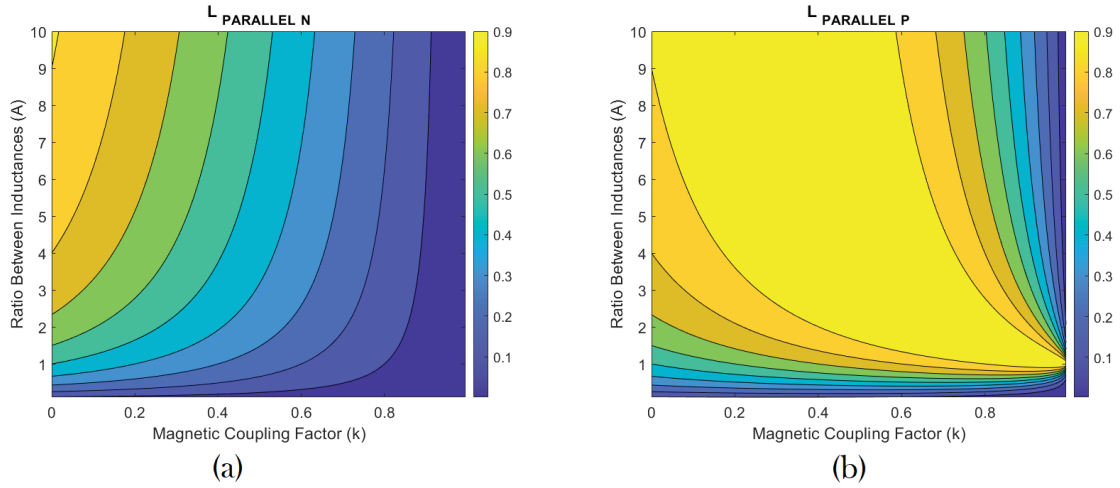

Figure 38 - Colormap representation of the equivalent inductance delivered by Parallel_N and Parallel_P configurations

The overall decision for which structure to use, depends on application and necessity in the inductances range among other factors, such as quality factor and

self-resonant frequency. One important characteristic to highlight is the higher quality factor delivered by the series and parallel configurations in the positive magnetic coupling structure when compared to the negative coupling composition, due to the higher inductance reached by the magnetic coupling effect. Moreover, for the same reason, the self-resonant frequency in the positive coupling composition tends to be lower than the alternative. The magnitude of the effects in these metrics depends on the magnetic coupling between the coils.

The overall quality factor and self-resonant frequency delivered by the structures are discussed in the next section, since they suffer the most influence from the switching in the structures.

3.5 SWITCHES

Both proposed structures feature three switches placed according to the desired configurations. Typically, CMOS switches are composed of an association of integrated transistors that, depending on its biasing, allows current to flow from its terminals; the elementary switch structure is an NMOS transistor, as presented in 39; in this case, the Drain terminal is usually the input terminal, the Source is the output and the gate terminal is utilized to control the current circulation between the terminals.

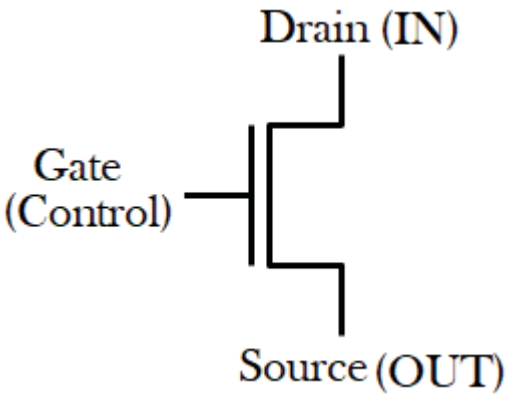

Figure 39 - Basic NMOS switch structure

Therefore, this element presents two distinct modes of operations depending on the transistor bias. When the gate voltage is high, the switch conducts current and ideally operates as a short-circuit. However, a parasitic resistance (usually known as R_{ON}) arises, and the switch operates as a resistor. The parasitic resistance depends on the switch transistor's width; where the higher width the lower is the associated

parasitic resistance. Similarly, when the switch operates as an open circuit (when the gate voltage is low) a parasitic capacitance, referred as C_{OFF}, appears. The parasitic capacitance also depends on the transistor's width; however, it increases proportionally to the element's width. These parasitics can be more precisely modeled (one example is shown in (YEH et al., 2006)), but for the context of this section, the on switch is treated as a resistance while the off switch is treated as a capacitance.

These parasitics added to the proposed structure significantly affects the quality factor and self-resonant frequencies delivered by the transformer. Since the quality factor measures the ratio between the imaginary and real portions of the element, any significant addition to the real portion of the inductances can influence heavily in the quality factor of the element. Similarly, the self-resonant frequency depends on the inductance and capacitance present in the structure and, introducing a considerable capacitance to the structure directly impacts the self-resonant frequency presented by the element.

Figure 40 illustrates the effect of introducing real switches to a Series_N structure utilizing transformer 1 as the electromagnetic element. The curve shows the effects in the L_{PRIM_NC} configuration; as this configuration does not suffer from magnetic coupling interference, is the best choice to analyze the switch's effects. This configuration possesses 2 closed and 1 open switches. The degradation in the configuration quality factor is apparent (as can be seen in the red curves), reducing from approximately 6 to around 2 (at 3 GHz). The self-resonant frequency also suffers a significant impact from the open switch, reducing from over 10 GHz, to approximately 6.2 GHz.

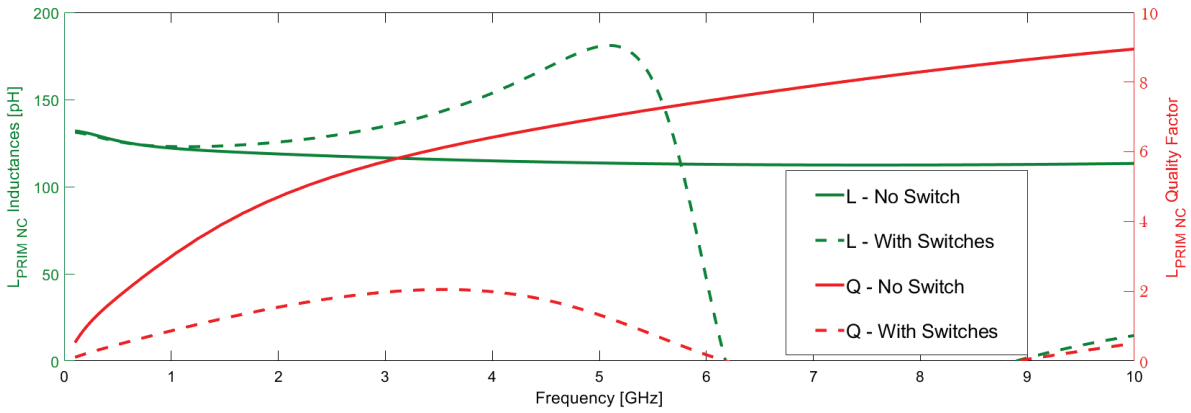

Figure 40 - L_{PRIM_NC} configuration switch's effects analysis

Since the parasitic resistance and capacitance directly depend on the width of the switch, it is expected that altering the width in the transistor could mitigate the parasitic effects in the quality factor and self-resonant frequency presented by the configuration. However, as previously mentioned, improving the design to reduce the resistance fatally increases the capacitance; this is where a tradeoff must be implemented, in order to allow the satisfactory operation of the proposed structure, a compromise in quality factor and self-resonant frequency has to be reached. Figure 41 shows the variation in quality factor and self-resonant frequency, depending on the width (ranging from 100 to 1000μm) of the switch's transistor.

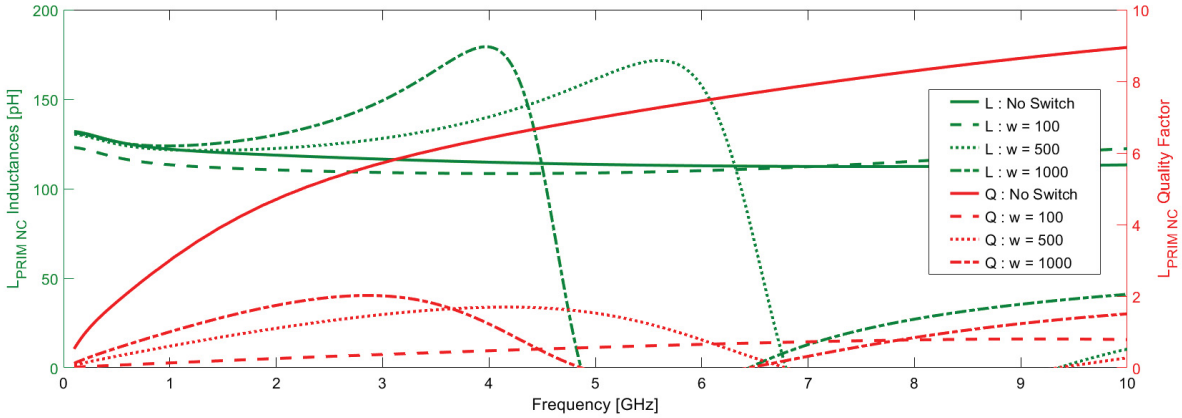

Figure 41 - Transistor's width influence in quality factor and self-resonant frequency.

From Figure 41, it is possible to notice that the maximum quality factor delivered by the configuration decreases as the transistor's width increases; meanwhile the self-resonant frequency is increased. In order to improve the overall quality factor and self-resonant frequency delivered by the structure, a study of different switch configurations was realized.

In this step, four different switch topologies were analyzed and the fundamental switch delivered the most consistent results (allied to an added simplicity to its design). The analyzed topologies are presented in Figure 42.

In order to keep a similar capacitance in the switches, the transistor's width in the parallel configuration, Figure 42 (b), is half the size of the single transistor. Similarly, the series configuration, Figure 42 (c) is twice the size of the single transistor. For the differential configuration (RAZAVI, 1998), all transistors width equates to one third of the width utilized in the single transistor.

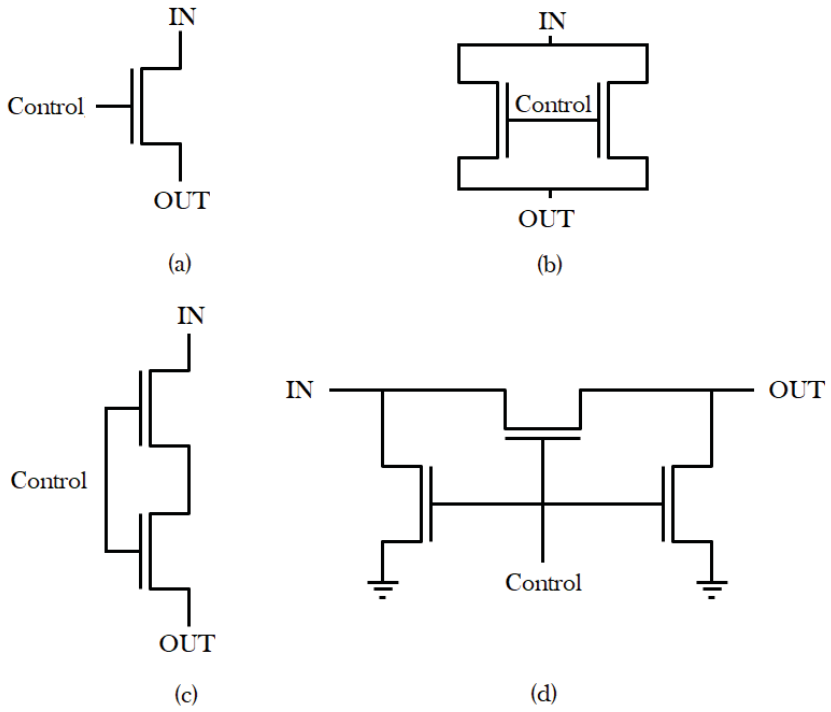

Figure 42 - (a) Single Transistor (b) Parallel (c) Series (d) Differential

Topologies similar to the differential configuration were also considered, such as (SHU et al., 2015, 2017), however due to the requirement of a coupling inductor in these topologies, they were discarded. Figure 43 shows the inductance and quality factor of the effects that these switches promote in the transformer under analysis for the configuration NC Prim.

It is possible to notice that all topologies presented a comparable self-resonant frequency, therefore, the capacitance added by all topologies are similar. The single transistor and parallel configurations showed very similar results with the higher maximum quality factor. As the simpler design of the single transistor switch could bring some advantages in the layout of the switch, the improvement of this configuration was researched.

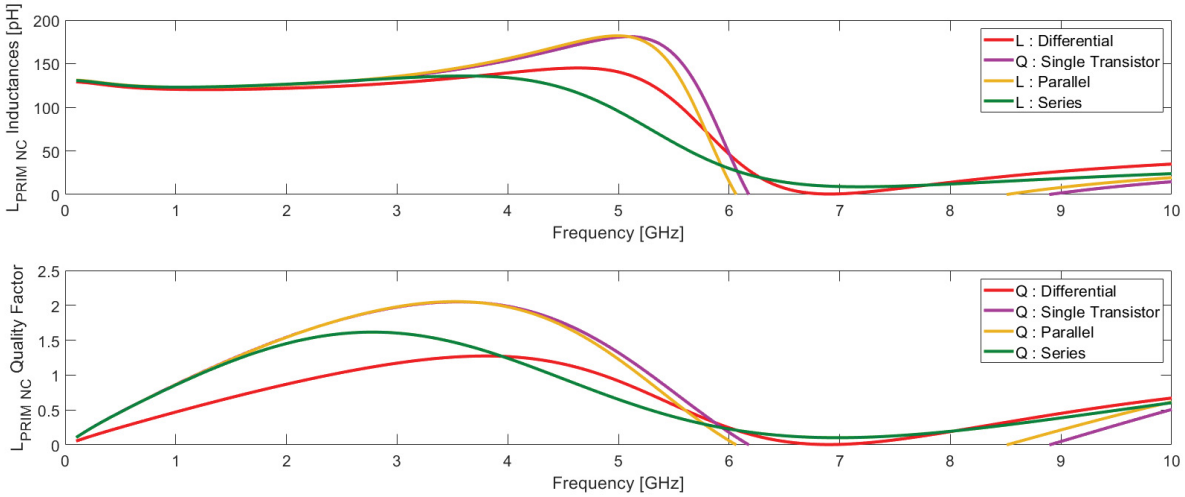

Figure 43 – Inductance and quality factor presented by the transformer when utilizing different switch topologies.

Some alterations to the single transistor switch were realized that slightly improved the overall performance of the proposed structure, as exhibited in Figure 44. A body floating technique was employed by adding a 20 kΩ resistor to the body terminal (YEH et al., 2006) and a 20 kΩ biasing resistor (MIN; REBEIZ, 2007) was also added to the transistor's gate. These techniques reduced the overall parasitics on the switch, ameliorating its performance.

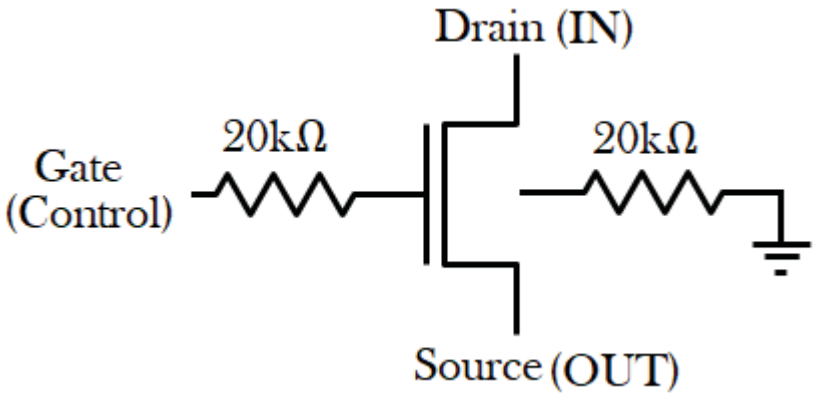

Figure 44 - Final switch design utilized in the structure.

Figure 45 shows the overall difference between switch topologies in the transformer 1 structure. It is noticeable that the body floating and biasing resistors are able to slightly improve the quality factor and that their effect adds to the improvement in the quality factor on the switch.

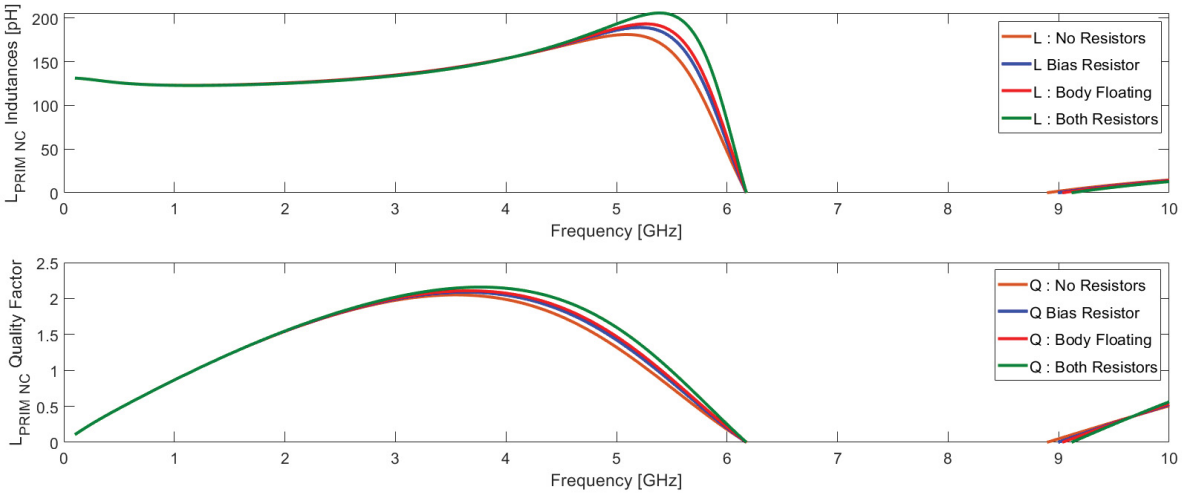

Figure 45 - Topologies' effect in the quality factor and self-resonant frequency

It is possible to point out that despite improving on the quality factor, the self-resonant frequency stayed the same for the four configurations, which means that these modifications in the switch topologies do not impact significantly the *OFF* capacitance on the switch.

In order to design the proposed structure accordingly, the switches must be taken into consideration, and not only for one of the configurations, since the mode of operation in each switch is different depending on the chosen configuration. Moreover, a compromise in the width of the switch must be found in order for all configurations to perform appropriately. A suggestion in this case, is to determine the maximum operating frequency required from the structure, and try to optimize the quality factor from there. Another important discussion is the possibility to utilize different width (or even topologies) for the switches, depending on more sensible configurations.

Since the quality factor and self-resonant frequencies depend on the *ON* resistance and *OFF* capacitance of the switches and, some configurations tend to naturally deploy a higher inductance or internal resistance, each configuration is more susceptible to each mode on the switches. A clear example is the series configuration, since it delivers a higher inductance, it is more affected to decreasing its self-resonant frequency due to the *OFF* capacitance of the switch. The *ON* resistance, however, has a lower impact in the overall resistance of the structure, since its internal resistance accounts for the internal resistance of both windings on the transformer.

This chapter presented a study on the possible equivalent inductances topologies that interconnecting a two-coil transformer's terminals could deliver,

categorizing and analyzing the resulting inductance. The proposed structure is also shown, which present two different options: one that sports a positive magnetic coupling and the second that exhibits a negative magnetic coupling. Finally, the effects of the switches in the structure are analyzed, such as transistor width, switch topology and, finally, some improvements to the single transistor switch are suggested.

4 USE CASE

In order to validate the structure proposed in this work, it was decided to implement said structure into a radiofrequency circuit. An LC tank voltage controller oscillator was chosen, as the controllable inductance can be utilized such as varactors are commonly utilized in several wide range oscillators.

Firstly, a work was developed with Leonardo Nakatani Moretti (LEONARDO NAKATANI MORETTI, 2021), which utilized Transformer 1 as its core transformer; the structure aforementioned was employed utilizing a negative magnetic coupling and the SC Prim, SC Sec and Series configurations were utilized in order to guarantee a wide range operation. The circuit however, presented a relative elevated power consumption.

This work's oscillator aims to deliver a significant tuning range while maintaining a relative low power consumption. Ideally, the 5G sub-6GHz operation band should be covered. This operation band was standardized by 3GPP under the new radio (NR) indentation, which is designed to meet requirements recommended by the International Telecommunication Union. This standard defines two applicable frequency ranges, denominated FR1 and FR2; the sub-6GHz frequency range relates to the FR1, and ranges from 450 MHz to 7.125 GHz (KIM et al., 2019).

Since the full spectrum of frequencies in the FR1 band is exceedingly large, the main target to the developed VCO was the deliver a percentual tunning range higher than 65% (which is a metric already obtained in the literature). The full range of frequencies depends on distinct inductances with different quality factors and self-resonant frequencies; therefore, the oscillator's actual frequency range will be determined by these chosen inductances.

A differential topology was employed in the VCO and is represented in Figure 46; formed by two cross-coupled complementary transistors pairs (i.e., an NMOS and a PMOS pair) connected to a LC Tank. The LC tank is comprised of a voltage-controlled capacitance, a variable inductance and a capacitor bank.

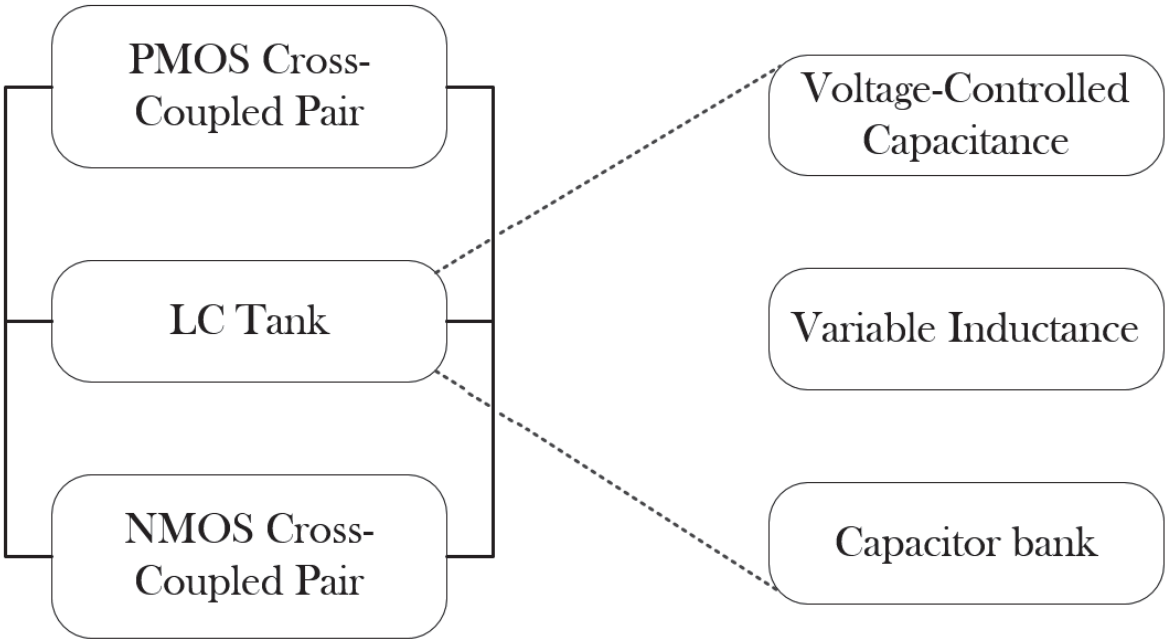

Figure 46 - VCO's block diagram

The frequency in which the circuit will oscillate will depend on the combination of the capacitances and inductances present in the circuit, as described by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L.C}}. \quad (31)$$

By altering the capacitances and inductance of the LC tank, the VCO will oscillate in a different frequency. The tank's building blocks are: a voltage-controlled capacitance, the capacitor bank and a variable inductance. The voltage-controlled capacitance is composed of a pair of differentially connected varactors whose gate voltage determines its overall capacitance; this element is responsible for fine tuning the oscillating frequency. The capacitor bank refers to a bank of capacitors that are switched in and out of the circuit, allowing for a coarse tuning of the oscillator's frequency. Finally, the variable inductance corresponds to this work's proposed structure, which provides an even higher coarse tuning of the oscillating frequency.

The VCO's initial design is divided into four steps, as shown in Figure 47. The first step was to design the variable inductances, as the higher and lower inductances would ultimately govern the lower and higher oscillating frequencies in the circuit. In order to limit the power consumption, a voltage source of 1.2 V was chosen. At the same time, since the parameters utilized in the cross-coupled pair would heavily

influence the current flowing through the circuit and also the oscillating frequency, these parameters were estimated.

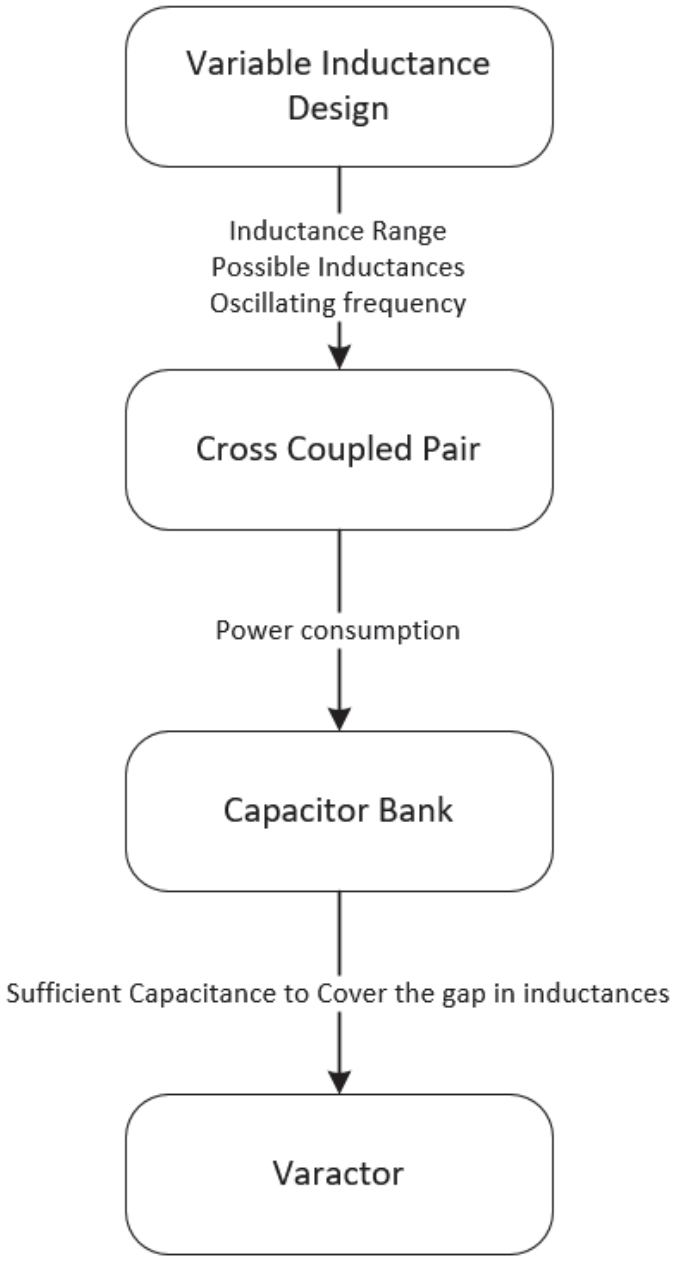

Figure 47 - Flow diagram of the VCO project

After the state-of-the-art research, a dissipated power lower than 5 mW was chosen as target to ensure the competitivity of the circuit; therefore, a maximum width was set, seeking to comply with the proposed target. Next, the capacitances were designed; these elements needed to guarantee that no gap in the frequency range would appear. In this case, the capacitor bank and varactor operate in tandem, with

the capacitor bank providing the aforementioned coarse tuning and the varactor fine tuning the oscillating frequency.

This chapter is subdivided into the different steps in the VCO design, starting with the design choices pertaining the variable inductance, followed by the cross-coupled pair parameters decision, then the capacitive bank design flow and, finally, the varactor. Lastly, the layout developed will also be described and the final results presented.

4.1 VARIABLE INDUCTANCE STRUCTURE

4.1.1 Design of the inductances

From the VCO point of view, the equivalent inductances design can be separated into three main aspects: the inductance delivered by structure, which would determine the oscillation frequencies, the quality factor that is crucial to the element's oscillation and the self-resonant frequencies that governs the range of frequencies in which the delivered inductances are applicable. All of these parameters are intertwined and dependent directly to the proposed structure's design.

Firstly, it was decided that a 1 nH and a 2 nH inductances would be utilized in the oscillator. This estimation was based in an example given by Razavi at a practical example shown in (RAZAVI, 1998). In order to analyze the viability of the two separate inductances, an ideal VCO was designed, with a large switched capacitor to allow both modes to operate through a frequency range of around 2 to 3 GHz.

In order to maintain the same capacitances and fully utilize the proposed structure, the ratio between the primary and secondary coils should be maintained to the other configurations. Since the VCO's oscillating frequency is proportional to the inverse of the product between the capacitance and inductances in the circuit; the capacitance-inductance product resulting from the minimum and maximum capacitance generates the frequency range delivered by a determined inductance. Ideally, in this case, by designing the minimum and maximum capacitances to present the same ratio as the adjacent inductances' ratios, the equivalent inductances of each configuration should present frequency ranges that complement each other, without frequency gaps.

For the structure's design, this meant that an eventual series configuration should deliver a 4 nH equivalent inductance, and a parallel configuration should deliver

a 0.5 nH. However, this ideal scenario was not possible. As shown in Figure 48, in order to reach 4 nH, a Series_P configuration should be utilized, with a magnetic coupling factor of approximately 0.37; this would deliver a 0.88 nH inductance to the associated parallel_P configuration (both points circled in red). Another option (circled in dark blue) was to utilize the Parallel_N configuration that displayed a 0.5 nH inductance at a k = 0.28; once again, the Series_N configuration would deliver an inductance similar to the inductance presented by one of the coils (approximately 2.2 nH).

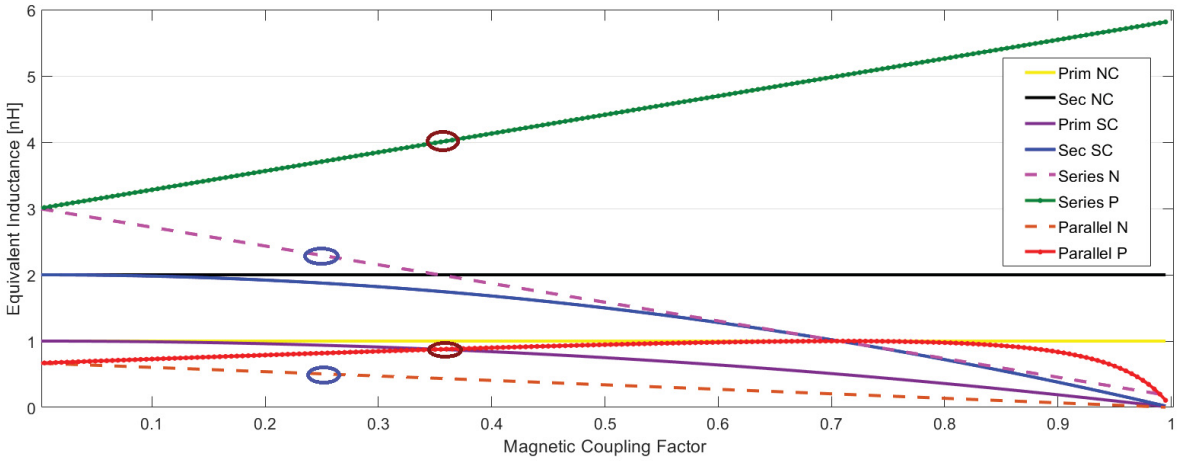

Figure 48 – Inductance's possibilities for $L_{Primary}$ = 2 nH and $L_{Secondary}$ = 1 nH

While both configurations could be utilized, a third option was envisioned: to reduce the ratio between the primary and secondary inductances. This would ultimately diminish the frequency range obtained by the oscillator; however, since the gap between inductances would also decrease, a smaller capacitor bank could be employed to cover all frequencies between different configurations, giving more leeway into the parasitic added by the remaining elements.

Since the 2 nH inductance presented an interesting middle ground in the ideal VCO frequency range, it was decided to adjust the 1 nH inductance. Since the ratio between the winding's inductances was revised to be 1.4, the secondary coil's inductance new target was 1.4 nH. Once again, the inductances' curves were plotted, and are displayed in Figure 49. Once again, it was not possible to extract a magnetic coupling that would grant a locked 1.4 ratio from both inductances; in this case, the magnetic coupling that Parallel_P configuration that would maintain the ratio was 0.215 (with Parallel_P inductance as 1 nH). However, Series_P configuration would deliver

4 nH of inductance, pertaining a ratio of 2; these points are circled in red. The same logic applied to the negative magnetic coupling configuration (highlighted in blue), where Series_N delivered a 2.82 nH inductance at 0.175 magnetic coupling factor. In this scenario, the Parallel_N configuration presented a 0.68 nH inductance (resulting in a ratio of approximately 2 as well). In both cases, the ratio was maintained for one configuration, but not for the other.

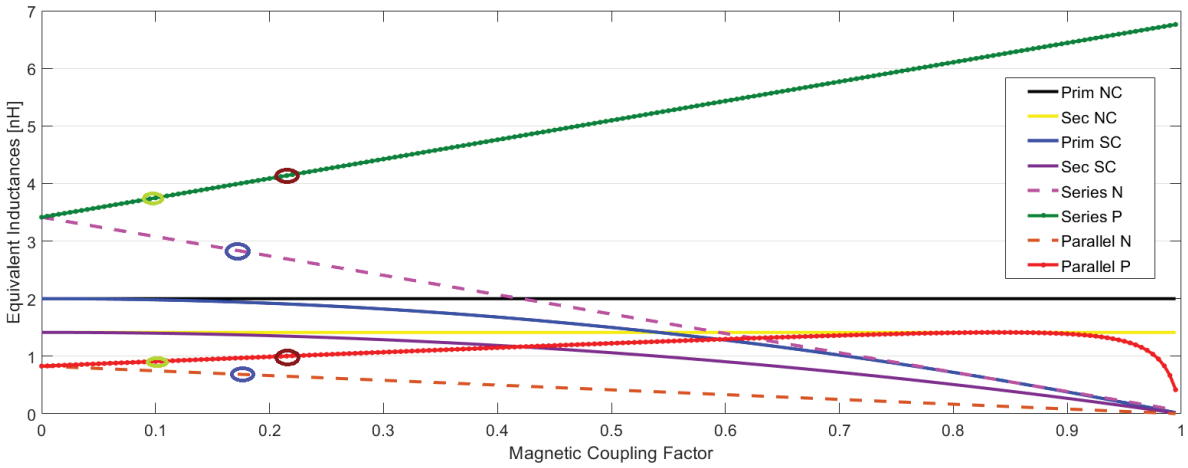

Figure 49 - Inductance's possibilities for $L_{Primary}$ = 2 nH and $L_{Secondary}$ = 1.4 nH

At this point, it was pondered to utilize a configuration with no magnetic coupling at all (i.e., magnetically isolated coils), which would deliver a 3.4 and 0.83 nH for the series and parallel configurations respectively. However, in order to explore the slight improvement in quality factor that a positive coupling causes to the structure, it was decided to employ a 0.1 magnetic coupling factor in the transformer's layout (highlighted in lime green at Figure 49).

The next step was to design the transformer's layout. Since this technology does not possess more than one thick layer to fully implement passive RF elements, placing one of the coils in the LY layer would greatly impair the quality factor of said coil; therefore, a horizontal coupling between windings was chosen as the best option for this technology.

The transformer's design started from the standard inductor cell provided in the technology library by the foundry. A maximum external diameter of 300 µm was established since that is the maximum diameter possible to implement in the library's inductor cell. From there, adjustments to the external diameter, turn separation, width and number of turns were proposed in order to approximate the coils inductances from the aforementioned targets.

The transformer's layout is presented in Figure 50. A reference plane is inserted encircling the transformer and possess a width of 25 µm. A distance of 30 µm and 45 µm separates the transformer's coils to the reference plane. In order to reach the desired 0.1 magnetic coupling, the distance between the primary (shown in the left) and the secondary is kept to a minimum (12.75 µm). A patterned ground shield, similar to the one utilized in (SILVA, 2017), was implemented in layer M1 (the lowest metal layer above the substrate) and connected to the reference plane, which is composed of all metallic layers. The reference plane has an opening in the higher layers so the transformer could be accessed.

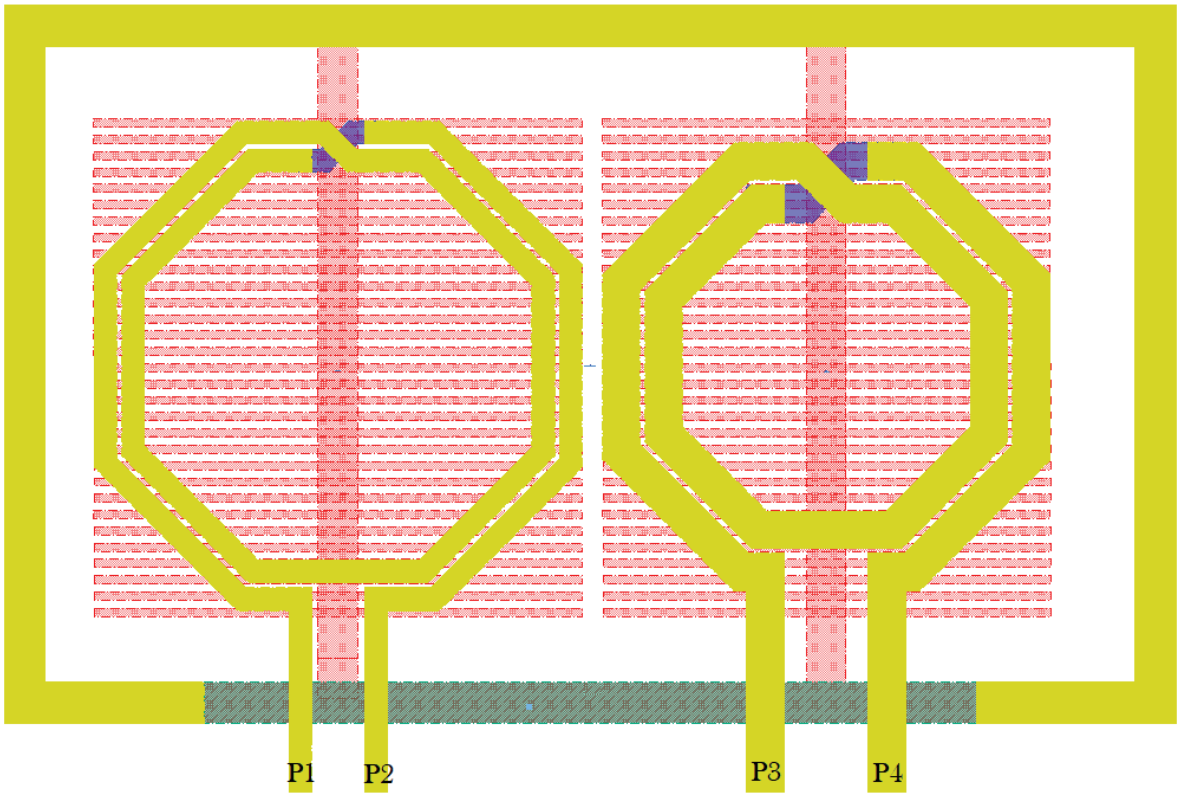

Figure 50 - Transformer's Layout

The coils parameters are summarized in table III. The primary coil exhibits a higher diameter and lower width in order to reach the designated 2 nH inductance, whereas the secondary employs a higher width and lower diameter aiming to deliver a 1.4 nH inductance. Both windings are designed in the higher layer (AM).

Table III – Transformer's dimensions

	Primary	**Secondary**
Diameter	300 µm	275 µm
Width	14 µm	23 µm
Separation	3 µm	3 µm
Number of Turns	2	2
Feed length	110 µm	123 µm
Feed Separation	33 µm	52 µm

Electromagnetic simulations utilizing a FEM (finite element method) were realized into this structure. Through the obtained scattering parameters, the coil's inductances and magnetic coupling were extracted, and are shown in Figure 51. The primary inductance resulted in around 2 nH and the secondary at around 1.4 nH, as expected. The magnetic coupling factor obtained was of around 0.07, slightly lower than the desired 0.1; this parameter could be increased by approaching the transformer coils, however, further approaching the coils would require an adjustment to one of the transformer's windings, since a contact between the conductors would occur, this scenario would require an alteration (the migration of a portion of one of the coils to a lower layer) to the transformer's coils in order to maintain the device's operation as two separate windings magnetically coupled. Since the difference in the magnetic coupling was not significant, and the equivalent inductances presented by the configurations were within expectations, the layout was not further modified.

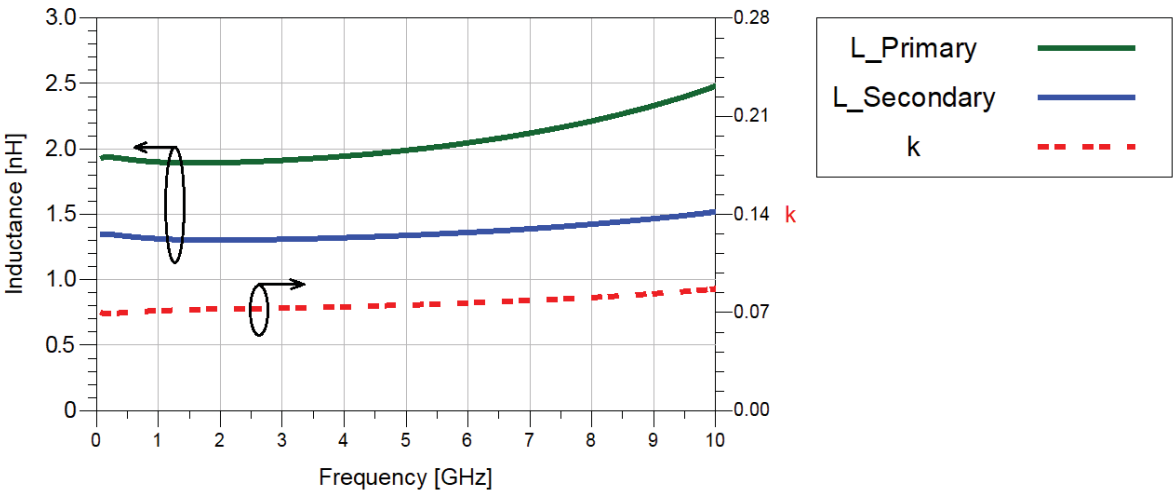

Figure 51 - Transformer's winding inductances and magnetic coupling coefficient (k)

As previously mentioned, a positive magnetic coupling structure was chosen for the variable inductance's design since it could benefit the series and parallel configuration's quality factor if compared to structure without magnetic coupling and is represented in Figure 52.

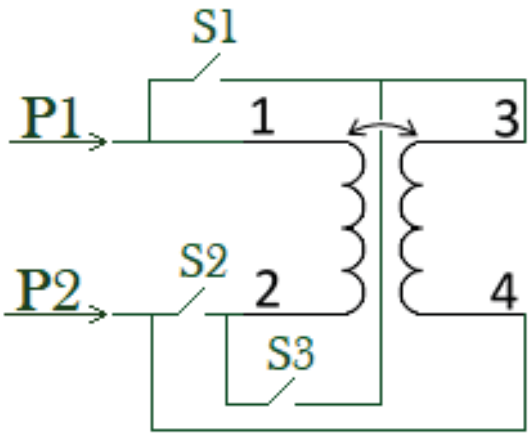

Figure 52 - Switching structure utilized in the variable inductance

Figure 53 presents the equivalent inductances delivered by each configuration in the designed structure based in ideal interconnections. It is possible to notice that the NC_Prim and SC_Prim inductances are practically equal; the same can be said about NC_Sec and SC_Sec.

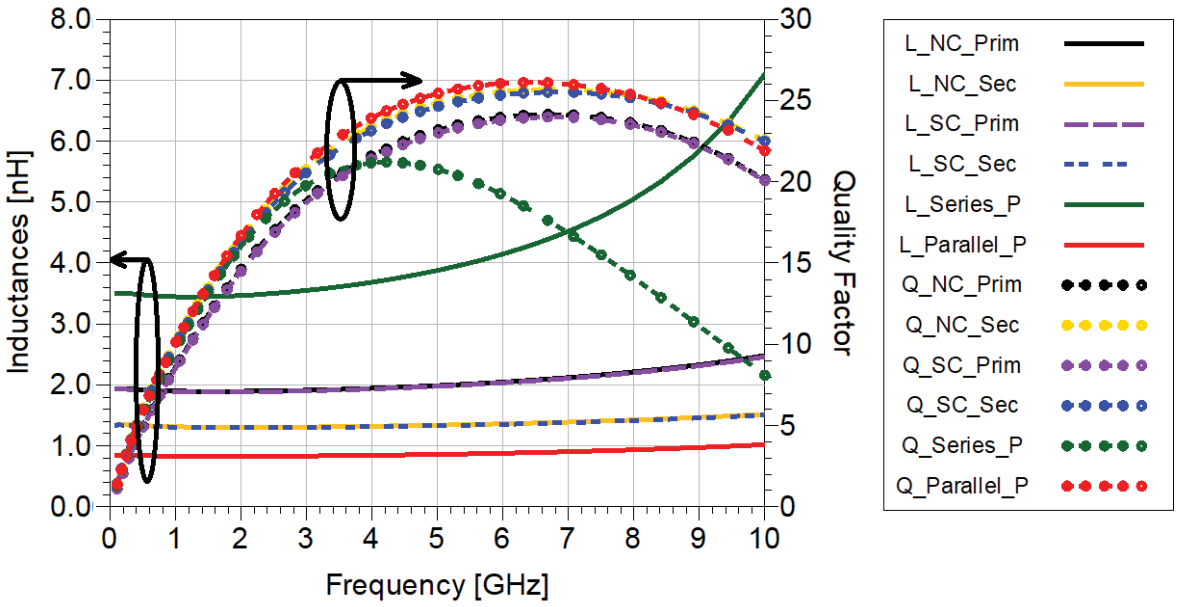

Figure 53 – Transformer's equivalent inductance and quality factor options considering ideal interconnections and switches.

This result was expected since the magnetic coupling is so low. Finally, the inductance delivered by the series configuration is represented in green, at around 3.5 nH, the NC_Prim and SC_Prim are presented in black and purple, respectively and amounts to approximately 2 nH. The parallel configuration is shown in red at roughly 0.8 nH and, finally, delineated in blue and yellow, are the inductances delivered by SC_Sec and NC_Sec respectively, at around 1.4 nH, as expected.

The overall maximum quality factor for all configurations is over 20. The Series_P shows the lower quality factor, which is explained by the lower self-resonant frequency associated to a higher inductance and the fact that the internal resistance in both coils is considered in the quality factor calculation. These parameters were obtained through simulations utilizing the scattering parameters matrix of the transformer. In none of the curves, the switches are considered; since the switches impair considerably the quality factor and self-resonant frequency of the structure; this analysis will be presented in the next sub-section.

4.1.2 Quality factor and self-resonant frequency

As already mentioned, the switches employed in the transformer's coils impact directly in the overall performance of the structure, more specifically in the quality factor and self-resonant frequency. The self-resonance frequency represents the point where the inductance reaches zero and starts operating as a capacitance.

Each switch functions in one of two possible states: open or closed. Open switches block the flow of current; since transistors implemented as switches are usually modeled as capacitances (SHU et al., 2015), the overall self-resonant frequency is reduced due to the combination between the inductances in the transformer's windings and the switch capacitance. Closed switches allow the current to flow and, usually end up belonging to the current flow path and, therefore, to the coils path; integrated transistors are modeled as resistances in this instance (SHU et al., 2015); inserting a resistance to an inductance's current path increases its series resistance and ultimately reduces the quality factor.

The switch topology utilized in this circuit is shown in Figure 54 and is composed of an NMOS transistor with a bias resistor connected to its gate and utilizing a body floating technique by attaching a resistor to its body. The switch's state is controlled by a voltage applied in the gate of the transistor. When the voltage in the switch's gate is 1.2 V the switch is closed and, when the voltage is 0 V, it is open. The

width in the transistor will determine the *ON* resistance and *OFF* capacitance on the switch and, therefore, the impact of this element in the structure performance.

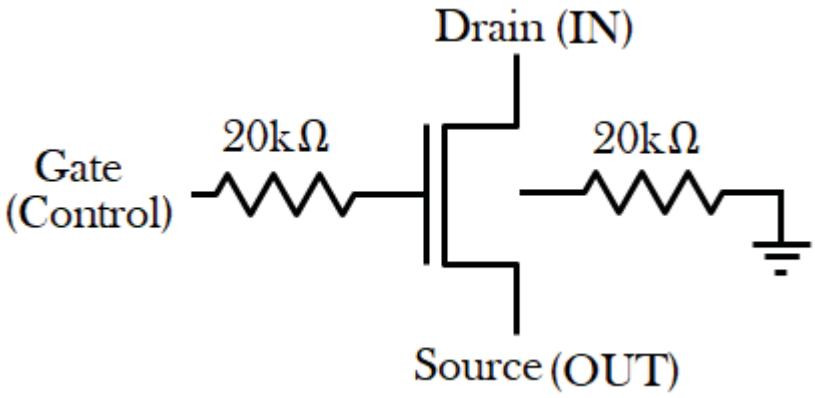

Figure 54 - Switch utilized in the VCO

A preliminary analysis was realized utilizing a 500 µm width for the switch; the quality factor of the structure was extracted and is presented in Figure 55. Since the inductance of the NC_Prim and SC_Prim configurations were the same, a comparison between the quality factor for these two configurations was decisive to determine which configuration would be utilized.

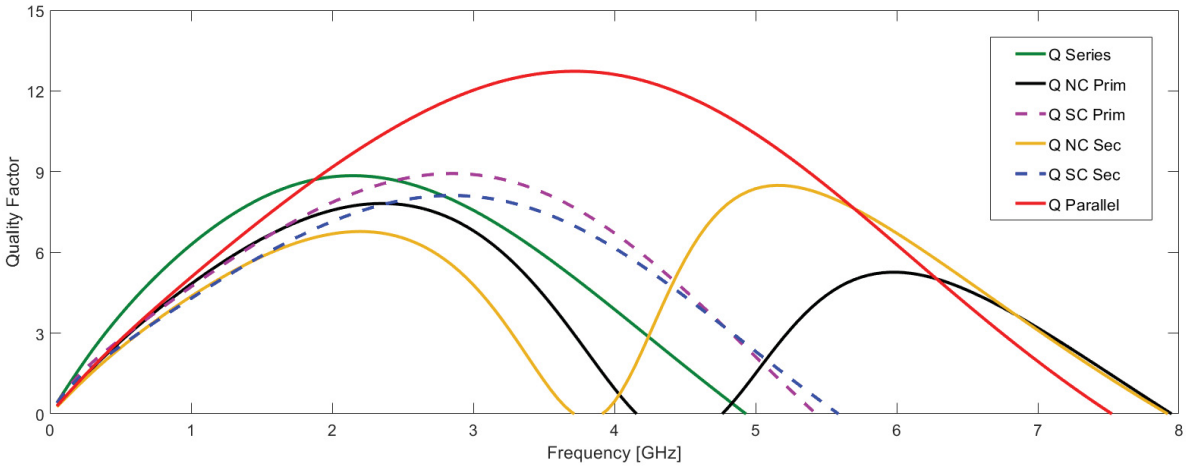

Figure 55 - Quality factor for all configurations in the structure

The NC_Prim configuration shows a lower self-resonant frequency, which is expected since this configuration sports two open switches (switch 1 and 3) versus only one in the SC_Prim configuration (switch 1), as illustrated in Figure 56. Since the closed switch in the secondary is not part of the inductance portion of the circuit, the fact that switch 3 is closed does not contribute to the detriment of the quality factor in

the SC_Prim configurations. The same parallel can be traced in the NC_Sec and SC_Sec configurations. Therefore, since the chosen magnetic coupling delivered practically the same inductance for configurations NC and SC, and the SC configurations present an overall higher quality factor and self-resonant frequency than the NC configurations, the NC configuration was not utilized in the VCO's operation.

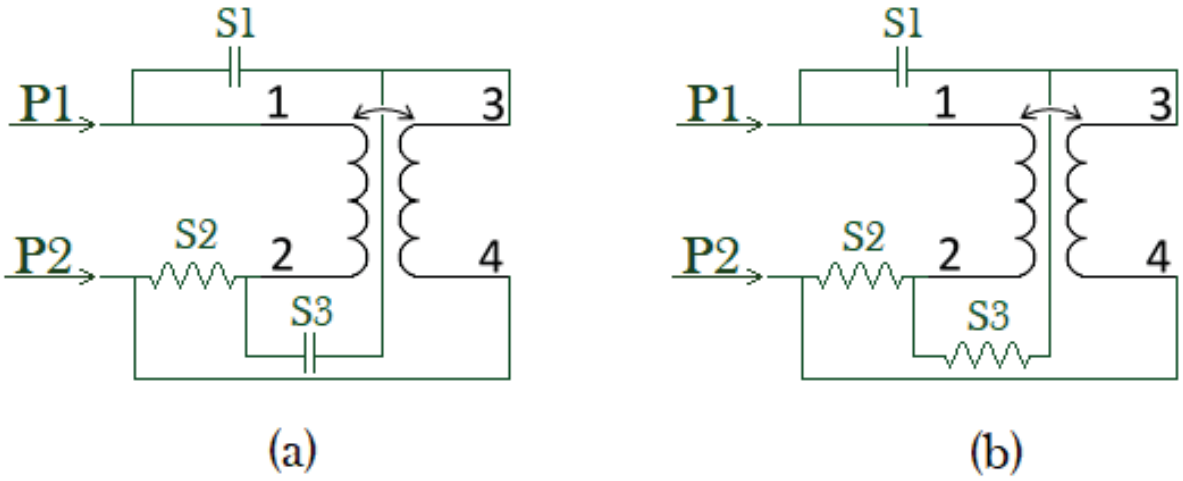

Figure 56 - (a) NC_Prim configuration (b) SC_Prim configuration

Finally, 4 different configurations were chosen to be utilized in the oscillator: SC_Prim, SC_Sec, Series_P and Parallel_P. Next, the width on the transistor's switch should be decided. Since there were three switches utilized in four different configurations operating in distinct frequencies, it was decided to employ a graphical analysis through parametric simulations to design the width of each switch in the structure. Figure 57 shows the quality factor for a width of 100 µm, 500 µm and 1 mm for each switch in all configurations.

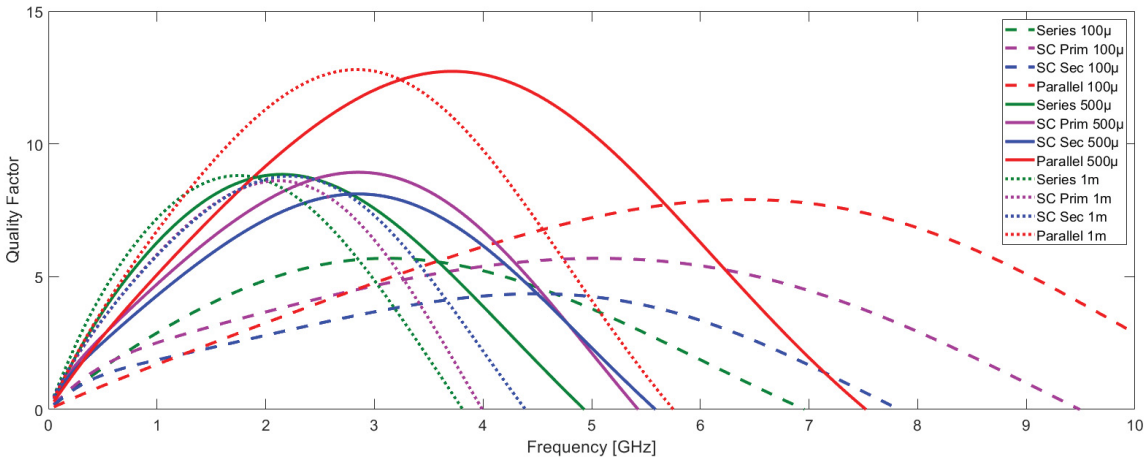

Figure 57 - Quality factor for a width of 100 µm, 500 µm and 1mm in the switches' transistors.

It is possible to notice that, in general, as all the transistor's width increases, so does the maximum quality factor of the structure; however, the self-resonant frequency is reduced. Furthermore, from a certain point, the maximum quality factor stops improving as consistently (which can be seen by the practically equal quality factors delivered by the parallel configuration with a width of 500 µ and 1mm) regarding the width; meanwhile, the self-resonant frequency keeps reducing, which limits the operating frequency of each configuration. In this case, it was assumed that a width at around 500 µm for the switches' transistors would be an interesting design point to explore.

Several parametric simulations were realized sweeping different width for the three switches and the best results were obtained for a width of 500 µm in the switch 1, 700 µm in switch 2 and 600 µm in switch 3. Finally, the selected widths were distributed into fingers to produce better results. Figure 58 shows the difference in quality factor between the all 500 µm switches, the developed switches without utilizing fingers and the final composition utilizing 20 fingers to distribute the effective widths.

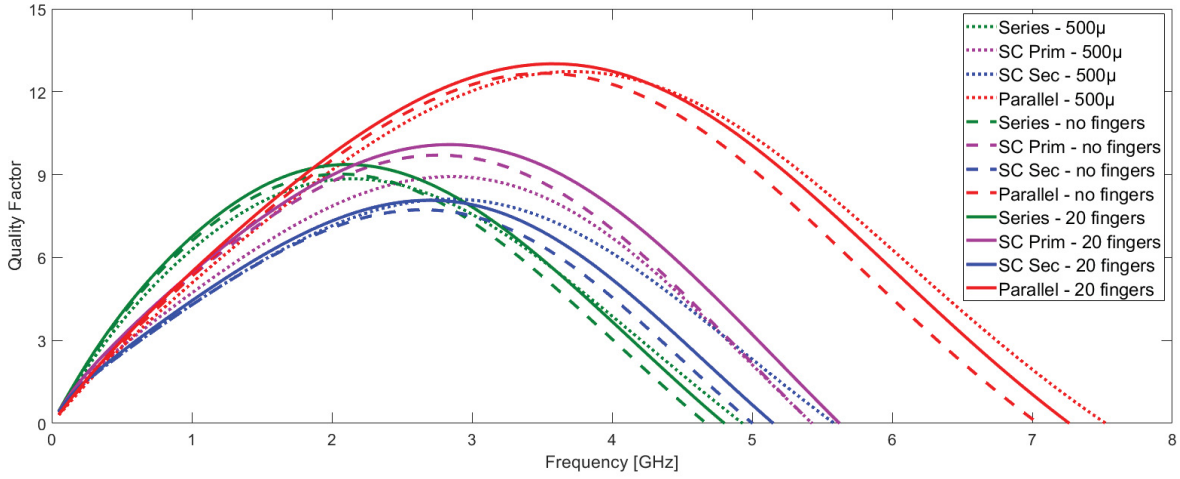

Figure 58 – Quality factor after parametric analysis and distributing the transistor width among fingers.

With this composition, a quality factor higher than 6 is expected in all the operating frequency of the configurations.

4.1.3 Designed inductances results

As previously mentioned, the SC Prim, SC Sec, Parallel and Series configurations were chosen to be utilized in the VCO; Figure 59 illustrates these

configurations and the switches effects (as *ON* resistance or *OFF* capacitances) in each case.

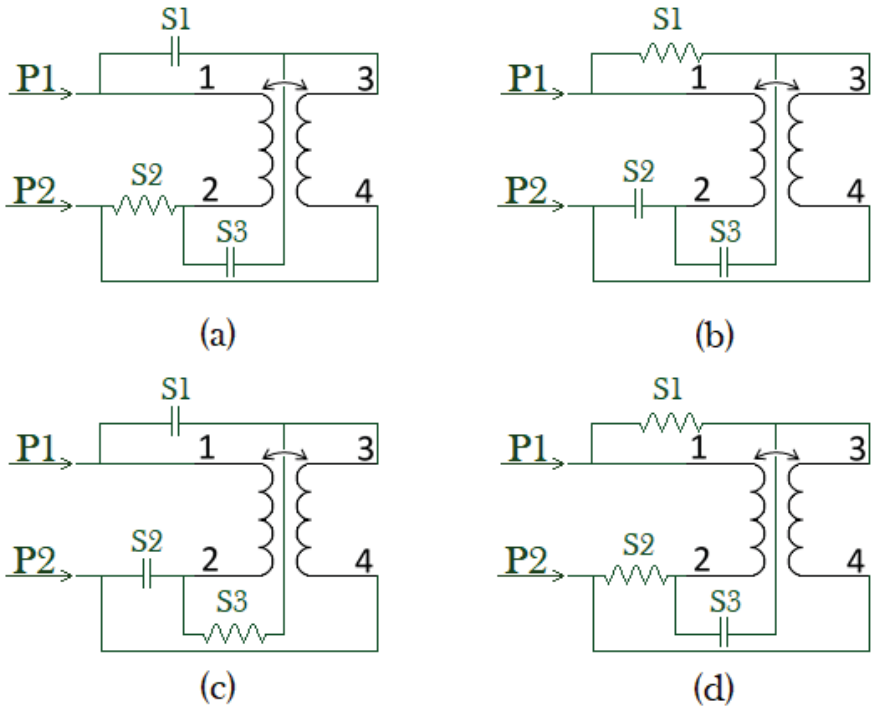

Figure 59 – Designed structure's chosen configurations: (a) SC Prim (b) SC Sec (c) Series (d) Parallel

Finally, Figure 60 shows the inductance and quality factor delivered by the selected configurations of the designed structure. In green, the series configuration sports a 3.5 nH inductance, a maximum quality factor of 9.31 at 2 GHz and operates up to 4.8 GHz. In yellow, the SC Prim configuration delivers an inductance of 1.95 nH, a maximum quality factor of 10 at 2.85 GHz and presents a self-resonant frequency of 5.6 GHz. The blue curve represents the SC Sec configuration that provides a 1.36 nH inductance, an 8.1 maximum quality factor at 2.7 GHz and a self-resonant frequency of 5.2 GHz. Finally, the parallel configuration shows a 0.85 nH inductance, a 13 maximum quality factor at 3.5 GHz and a self-resonant frequency of 7.3 GHz.

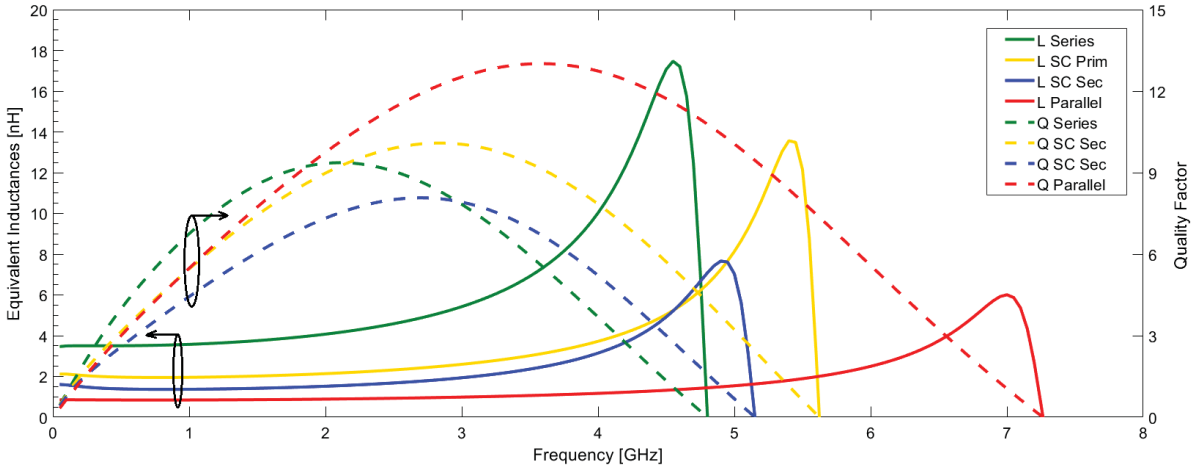

Figure 60 - Designed structure Inductances and Quality Factor results

4.2 CROSS COUPLED PAIR

The utilized VCO topology employs two complementary cross-coupled transistor pairs attached to the variable inductance structure as shown in Figure 61. The differential complementary VCO topology was chosen as it usually delivers a lower current consumption, an important operational criterion in this design. In green, the PMOS pair is highlighted while the NMOS pair is highlighted in red. Since the VCO topology is a differential one, both transistors in the pair possess the same design parameters.

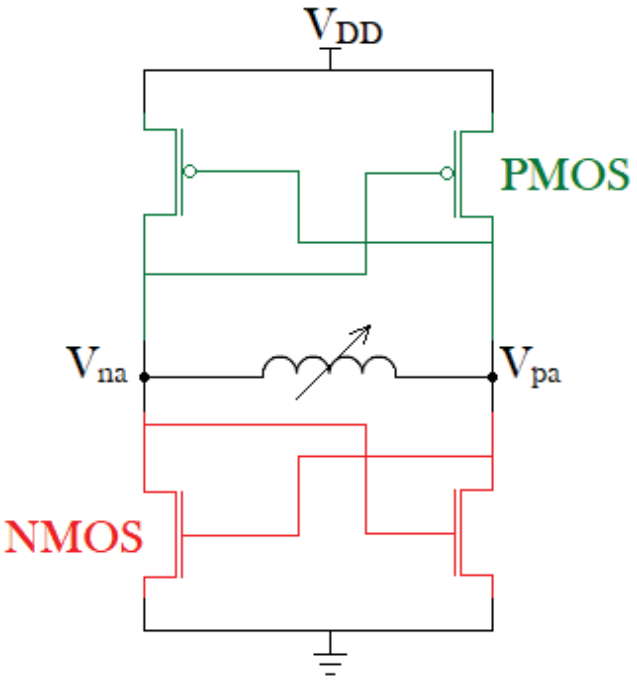

Figure 61 - Complementary cross coupled VCO

This topology oscillates due to the relationship between the inductance and capacitance of the VCO's elements, forming an oscillating LC network. However, when dealing with real components, the parasitic resistance of the devices is added to network, damping the oscillation of the now RLC network. The main purpose of the cross-coupled pairs is to deliver a negative resistance that eliminates the damping caused by the parasitic of the VCO's components.

In order for the circuit to oscillate, the cross-coupled pairs need to exhibit a gm that counters the parasitics added by the oscillator elements, allowing the oscillation. The resistance provided by the cross-coupled pairs can be described as:

$$R_{NMOS} = -{}^{2}/_{g_{mNMOS}}, \tag{32}$$

$$R_{PMOS} = -{}^{2}/_{g_{mPMOS}}. \tag{33}$$

For the complementary cross-coupled transistor pairs, the parallel between the resistance delivered by each pair should be the same as the parasitic added by the oscillator elements. Therefore, it is possible to declare that the required gm for the oscillation of the circuit is:

$$gm_{NMOS} + gm_{PMOS} = {}^{2}/_{R_{parasitics}}, \tag{34}$$

where gm_{NMOS} is the gm delivered by the NMOS pair, gm_{PMOS} is the gm of the PMOS pair and $R_{parasitics}$ is the resistance added by the circuit's parasitics. This is the main condition that the VCO needs to comply to, in order to oscillate, being one of the starting points to define the circuit's parameters.

The cross-coupled pair constructive parameters (width, length, number of fingers, etc) will determine the transistors gm, the DC voltage in the output terminals of the VCO (V_{na} and V_{pa}), the current flowing in each side of the oscillator and, therefore, the power consumption in the oscillator. Also, the parasitic capacitances (gate-source, gate-drain, drain-body capacitances) in the transistor will influence the oscillating frequency (and also frequency range) of the circuit.

Firstly, a ratio between the width in the PMOS transistors pair and NMOS transistors pair was stipulated. The main objective was to maintain the DC voltage in the V_{na} and V_{pa} nodes at 0.5V; this decision relates directly to the varactor design, and will be detailed in a subsequent section. In order to obtain the desired DC voltage at

nodes V_{na} and V_{pa}, the PMOS and NMOS transistors should have a specific gm ratio; an initial circuit was simulated and, from there, the parameters in the corresponding transistors were adjusted in order to guarantee the predetermined gm ratio for both transistors and, consequently, the 0.5 V at each node.

From these initial parameters, the oscillation frequency of the circuit was extracted and, the contribution to the capacitance from the transistor pairs was estimated. These parameters, however, were not definitive, since the VCO operation would also heavily depend on the capacitor bank and varactors employed in the circuit.

4.3 CAPACITOR BANK AND VARACTOR

After estimating the capacitance on the cross-coupled pairs (of around 340 fF at 3.8 GHz), the capacitor bank desired minimum and maximum capacitances were calculated in order to prevent any gap in the possible oscillating frequencies range between the structure configurations by taking into consideration the equivalent inductance presented in each configuration. Upon initial inspection, the most critical inductance gap would be between Series and SC Prim configuration (that presents an inductance ratio of 1.8), followed by the SC Sec and Parallel configurations (with an inductance ratio of 1.6) and, finally the SC Prim and SC Sec configurations (with an inductance ratio of 1.4).

A 3-bit capacitor bank, controlled by differential switches was chosen to cover the full frequency between Series and SC Prim configurations. Figure 62 (a) shows the 3-bit capacitor bank, whereas Figure 62 (b) shows the topology of the differential switch employed in the bank. The capacitors are labeled from the lowest to highest capacitances, likewise, the switches implemented in the circuit present different parameters and are labeled as such. The difference comes from the open state capacitance that rules the minimal capacitance on the bank. The switch is controlled by an external voltage applied to the interconnected gates of the switch’s transistors; when a high voltage (1.2 V) is applied, the switch closes, when a low voltage (0 V) is applied, the switch opens.

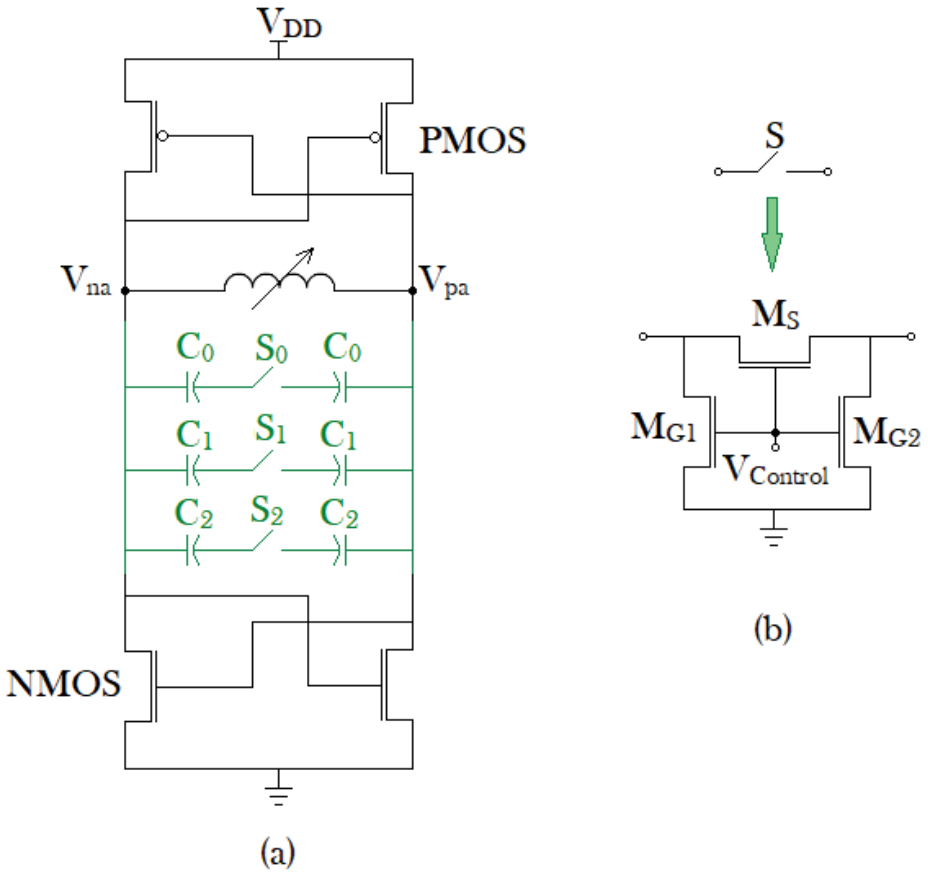

Figure 62 - (a) VCO considering a 3-bit Capacitor Bank (b) Differential switch employed

As previously mentioned, when the switch is open it operates as a capacitance and, in this case, the equivalent capacitance in a specific portion of the bank corresponds to the series association of both capacitors and the switch capacitance. Since the capacitance delivered by the switches is considerably lower than the capacitance of the capacitors in each portion of the bank, the equivalent capacitance in each portion when the switch is open approximately the same as the switch's capacitance.

When the switch is closed, the equivalent capacitance equates to half of each capacitance in that portion of the bank. Consequently, the maximum and minimum capacitances delivered by the capacitor bank corresponds to:

$$C_{max} = (C_0 + C_1 + C_2)/2\,, \tag{35}$$

$$C_{min} = C_{S_0} + C_{S_1} + C_{S_2}\,. \tag{36}$$

From this point on, it is possible to determine the maximum and minimum frequency that each inductance configuration should allow the circuit to oscillate on. It was chosen a 10% overlap zone between each configuration frequency limits aiming

to prevent blind zones in the oscillating frequency range. It is also imperative to take account of the blind zones that can occur from the portions of the bank; in this case, a 10% overlap zone was also envisioned. Therefore, the relationship between the capacitances of each capacitor and switch is described by:

$$C_0/_2 > 0.9\left(C_{S_1}\right), \tag{37}$$

$$C_1/_2 > 0.9\left(C_{S_2}\right). \tag{38}$$

A similar approach must be applied to the varactor capacitance excursion; the utilized varactor is a standard thin oxide NMOS varactor whose capacitance fluctuation will dictate the maximum and minimum capacitance each portion of the capacitor bank will be able to deliver. Once again, the blind zones must be avoided and a 10% overlap was set.

According to the technology manual, the ideal DC voltage drop applied to the varactor to fully explore the possible capacitances it can deliver should vary between - 0.5 and 1 V. Since the DC voltage at nodes V_{pa} and V_{na} were set to 0.5 V in the cross-coupled pair parameter design, an applied voltage from 0 to 1.2 V at the varactor's anode (drain/source) would effectively provide a - 0.5 to 0.7 V variation, which was sufficient to cover the capacitance range desired.

Figure 63 shows the schematic of the VCO including all elements, highlighted in green are the varactors. The capacitance C_T is dependent on the voltage applied to the capacitors through V_{Tune}. As with the capacitor bank, the minimum and maximum capacitances delivered by the varactor must cover the bank's capacitances. Therefore, the relationship between the capacitances on the varactor and the banks are described by:

$$C_{S_0} + {C_{T_{max}}}/_2 > 0.9\left({C_0}/_2 + {C_{T_{min}}}/_2\right), \tag{39}$$

$$2C_{S_1} + C_{T_{max}} > 0.9\left(C_1 + C_{T_{min}}\right), \tag{40}$$

$$2C_{S_2} + C_{T_{max}} > 0.9\left(C_2 + C_{T_{min}}\right). \tag{41}$$

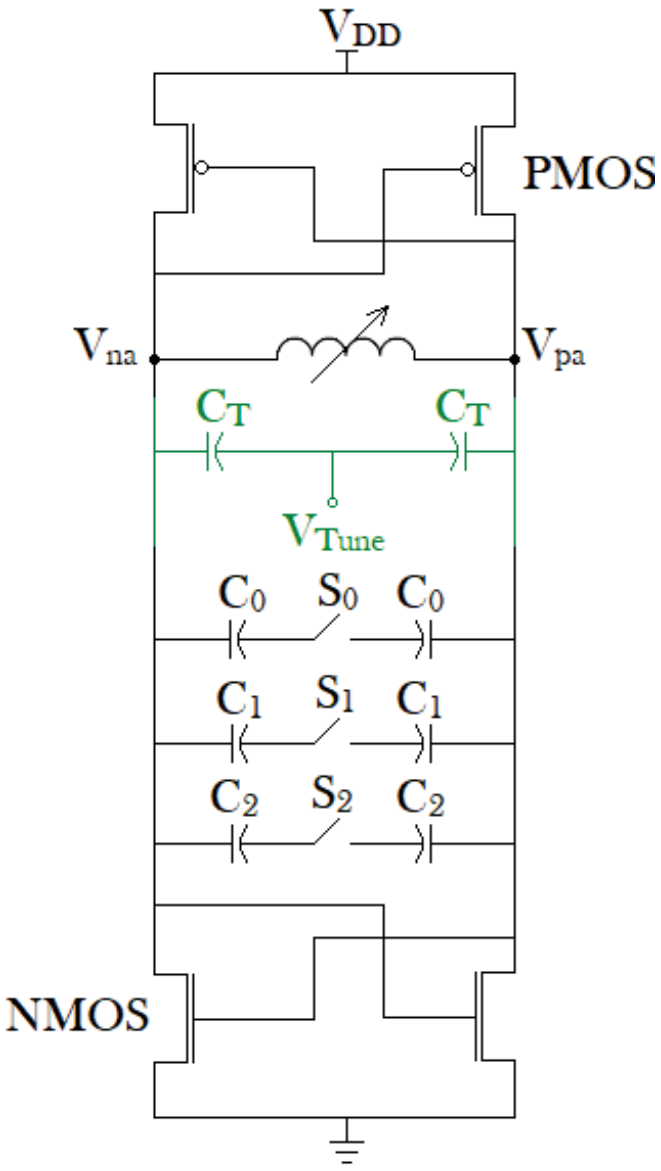

Figure 63 – LC-Tank VCO considering variable capacitances

Finally, the minimum capacitances obtained in the VCO corresponds to the cross-coupled pair parasitic capacitance, the minimum capacitance delivered by the capacitor bank and the varactor's minimum capacitance. Similarly, the maximum capacitance present in the VCO corresponds to the, once again, cross-coupled pair parasitic capacitance and the maximum capacitance delivered by the capacitor bank and varactors. These capacitances can be broken down as:

$$C_{min} = C_{Trans} + \frac{C_{T_{min}}}{2} + C_{S_0} + C_{S_1} + C_{S_2}\,, \tag{42}$$

$$C_{max} = C_{Trans} + \frac{C_{T_{max}}}{2} + \frac{(C_0 + C_1 + C_2)}{2}\,. \tag{43}$$

From there, the maximum frequency that an inductance configuration could reach should be the same as the minimum frequency attainable by the subsequent inductance configuration; therefore, since the relationship between frequencies depends on the product between the inductance and capacitance of the VCO, in order to avoid the blind zones, it can be characterized as:

$$L_{config1}C_{max} > 0.9L_{config2}C_{min} . \quad (44)$$

This relationship should be respected for the Series-SC Prim, SC Prim-SC Sec and SC Sec-Parallel inductance configurations, which would guarantee a full range of oscillating frequencies without any blind zones. After compiling all these relationships, the first step was to design the differential switches, since their *OFF* capacitance depends directly to their *ON* resistance, which should be taken into consideration in order to keep the quality factor of the VCO tank as high as possible (guaranteeing its oscillation).

With the switches designed, the varactor and the capacitor bank parameters were defined and the schematic was simulated. Since the estimated capacitance of the cross-coupled pair would vary depending on the oscillating frequency, several adjustments to the calculated parameters were required. Including in the cross-coupled pair widths and, consequently, its gm. The 0.5 V between transistor pairs should be maintained to keep the varactor's operating point. The new widths on the cross-coupled pairs were adjusted and, the capacitors and varactors were accordingly adapted (through simulations and result analysis), guaranteeing that no blind zones would appear. After these adjustments, the schematic of the VCO was deemed complete.

4.4 VCO SCHEMATIC

The schematic of the designed VCO is shown in Figure 64 and the parameters of each component are compiled in table IV. The PMOS cross-coupled pair (identified as M_P) shows transistors with 5 fingers and 5 µm width (for an effective width of 25 µm), whereas the NMOS coupled-pair (labeled as M_N) presents 8 fingered transistors with 6 µm width in each finger for an effective width of 48 µm. The varactors each exhibit a width of 4.2 µm and a length of 1.1 µm repeated in 6 gates, delivering a nominal effective capacitance from 71 fF to 303fF (considering a voltage ranging from -0.5 V to 1.0 V).

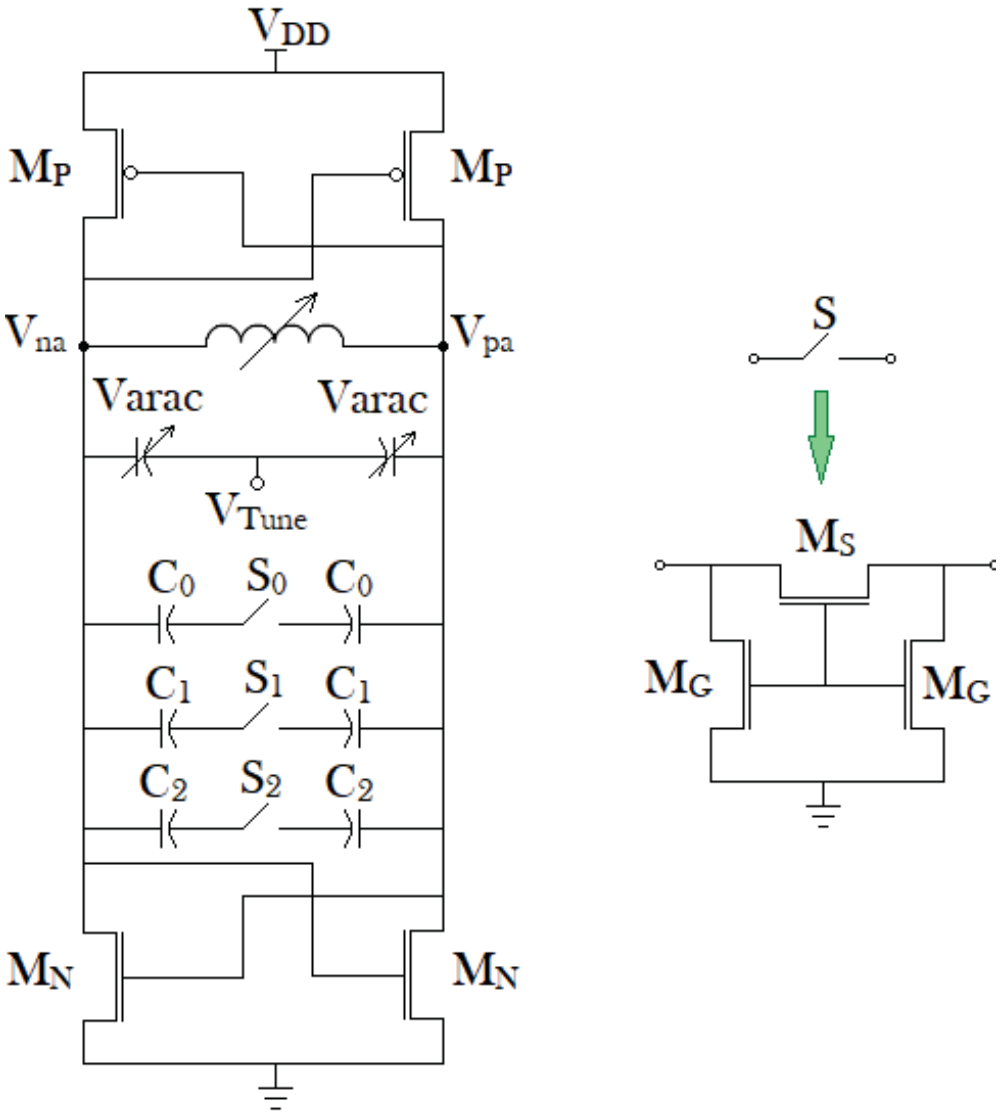

Figure 64 - Designed VCO

The capacitor bank is formed by three portions with capacitances C_0, C_1 and C_2. Each capacitance if formed by an association of identical capacitors exhibiting 7.5 µm of width and 6.6 µm of length, the difference between the capacitances is the number of capacitors associated. Their nominal capacitances are: 239fF, 478fF and 956fF to capacitors C_0, C_1 and C_2, respectively. Finally, each capacitor bank's switches are formed by one M_S and two M_G transistors. All of the switches' transistors presents the same width and length, which are 5 µm and 120nm respectively. The main difference between the transistors in the capacitor bank switches are their number of fingers. The M_S transistors sports twice the fingers as the M_G transistors, likewise, the number of fingers from each portion of the bank is twice of the previous portion. This

generates a higher minimum capacitance to accompany the capacitors bank increase in capacitance at each portion.

Table IV - VCO devices' parameters

Device	Width	Length	Fingers/Multiplicity	Element
M_P	5 µm	120 nm	5 (fingers)	Pfet_RF
M_N	6 µm	120 nm	8 (fingers)	Nfet_RF
Varactors	4.2 µm	1.1 µm	6 (gates)	ncap
C_0	7.5 µm	6.6 µm	1 (multiplicity)	Dualmim
C_1	7.5 µm	6.6 µm	2 (multiplicity)	Dualmim
C_2	7.5 µm	6.6 µm	4 (multiplicity)	Dualmim
M_{S0}	5 µm	120 nm	6 (fingers)	Nfet_RF
M_{S1}	5 µm	120 nm	3 (fingers)	Nfet_RF
M_{S2}	5 µm	120 nm	12 (fingers)	Nfet_RF
M_{G0}	5 µm	120 nm	6 (fingers)	Nfet_RF
M_{G1}	5 µm	120 nm	24 (fingers)	Nfet_RF
M_{G2}	5 µm	120 nm	12 (fingers)	Nfet_RF

After the completion of the schematic's design, and confirmation of the VCO's operation through simulations, the next step was to realize the layout of the circuit, which will be covered in the next section.

4.5 LAYOUT AND POST LAYOUT RESULTS

In order to maintain the operating point from the schematic, the layout aims to reduce the insertion of parasitics from the connections between the devices on the VCO. Firstly, a node in the schematic was separated into two different nodes in the layout. In this case, the cross-coupled pair is connected to the inductor at a different physical point than its actual output (which would be connected to a separate circuit, or pads for measurement). The inductor connection nodes are labeled as VPAL and VNAL, whereas the original V_{pa} and V_{na} nodes are positioned at the circuit's output in order to better emulate the VCO operation.

Figure 65 shows the final layout considering the inductor, its reference plane and the VCO elements and connections. The layout occupies an area of 0.447 mm², most of it is the horizontal coupled transformer. In order to extract the parasites added by the layout, a parasite extraction simulation was performed. However, since the transformer's parasitics are already included in the electromagnetic simulations, the circuit's parasitic extraction simulation does not include the transformer. The

transformer's scattering parameters are added after the parasitic simulation, through an s-parameter block in a schematic simulation, extracting the full VCO performance.

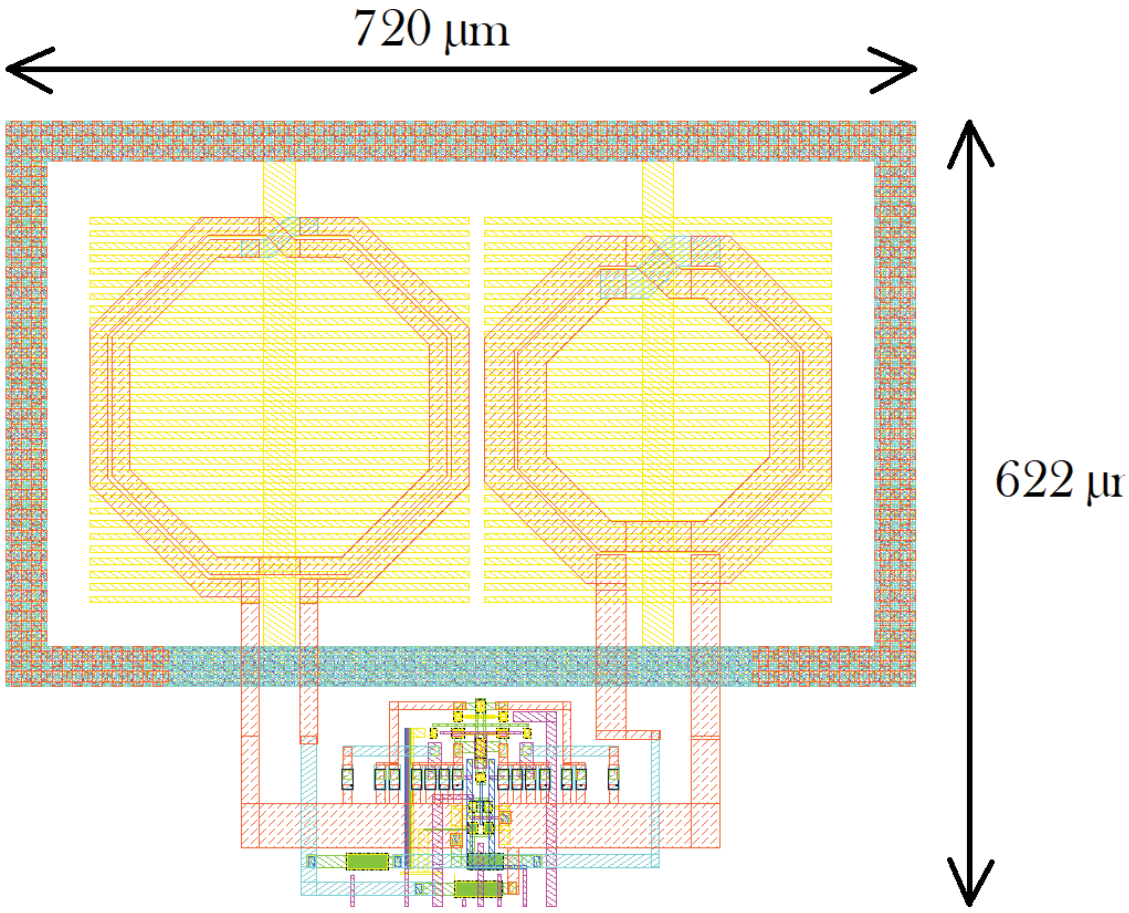

Figure 65 - Designed VCO complete layout

A zoom in the layout by removing the inductor in shown in Figure 66. It is possible to notice the different points of connections VPAL/VNAL and Vpa/Vna, as well as the switches and varactor voltage control and vdd. The capacitive bank is highlighted in black, while the cross-coupled pair are marked in red. The varactors are located inside the green rectangle. The ground is directly connected to the inductors ground plane; finally, the connection points to the inductor are VPAL, P2, P3 and VNAL.

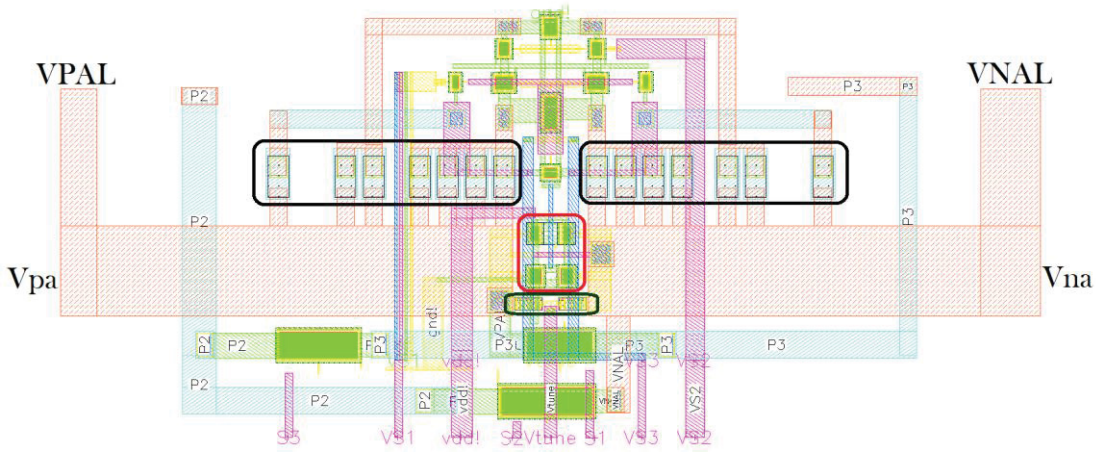

Figure 66 - VCO zoomed in

From the VCO post-layout and the transformer's electromagnetic simulations, the following results were obtained. In order to identify the capacitor bank's modes, Figure 67 is presented. It represents the color associated to each capacitor activation in the bank, where VC0, VC1 and VC2 represents the voltage applied to the switches in the bank. When the voltage is high, the switch is closed, resulting in a capacitance of half of the capacitors in that portion of the bank. When zero is applied to the switch, it opens and the equivalent capacitance corresponds to approximately the switch's capacitance.

	VC0	VC1	VC2
	1.2	1.2	1.2
	1.2	1.2	0
	1.2	0	1.2
	0	0	1.2
	0	1.2	1.2
	0	1.2	0
	0	0	1.2
	0	0	0

Figure 67 - Capacitor bank's color code identification

A transient analysis was performed and the differential signal Vpa-Vna was utilized to obtain the oscillating frequency of the circuit. The designed VCO's oscillation frequencies are shown in Figure 68. The analysis is separated by the variable

inductance structure's configurations, and V_{Tune} represents the voltage applied to the varactors. Considering each configuration separately, it is possible to notice that there is no gap between the capacitor bank's modes, which assures the full operating range in the interval.

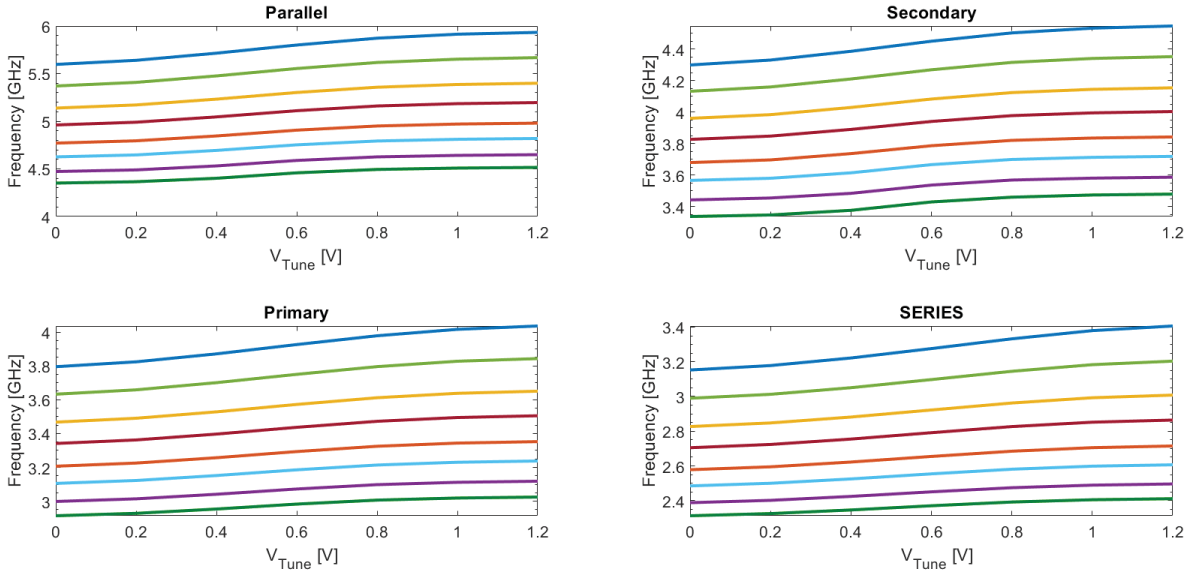

Figure 68 – VCO's oscillating frequencies

The parallel configuration is able of oscillate in the range of 4.35 GHz to 5.93 GHz, the secondary oscillates from 3.34 GHz to 4.54 GHz, the primary configuration is able to oscillate from 2.91 GHz to 4.03 GHz and, finally, the series configuration oscillates from 2.31 GHz to 3.41 GHz. From the plotted data, it is possible to notice that there are no blind zones between each configuration, and the circuit oscillates from 2.31 GHz to 5.93 GHz with a central frequency of 4.12 GHz and a percentual tunning range of 87.86%.

It is also possible to notice that the primary configuration is fully covered by the secondary and series configurations and, at first glance, could be discarded. However, as it will be shown subsequently, the lower band in each configuration presents a higher power consumption, and overall worst phase noise; therefore, this configuration can be utilized to deliver a better performance in most of its range. Moreover, its utilization, albeit recommended, is completely optional and is already implemented in the oscillator's design.

The voltage signal delivered by the oscillator in each frequency presents a singular amplitude due to the varying characteristics of the circuit, especially since the quality factor of the different inductances are dependent on the selected configurations.

The same can be said about the quality factor of the capacitor banks; as an example, Figure 69 shows the differential voltage between the oscillator outputs (i.e, Vpa – Vna) in the maximum and minimum operating frequency (5.93 GHz and 2.31 GHz, respectively).

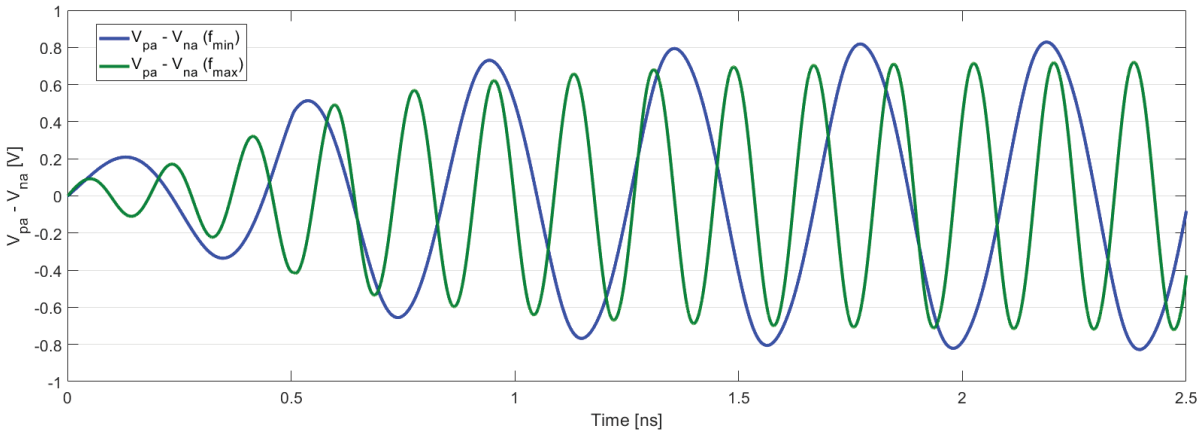

Figure 69 - Differential output voltage delivered by the oscillator at the maximum and minimum operating frequency.

The voltage amplitude in the f_{max} case is: 724 mW while the amplitude in the minimum operating frequency is 836 mV. This amplitude can be altered by increasing the VDD voltage applied to the circuit, however, it would alter the oscillating frequency and also increase the consumed power. It is important to mention that the lower amplitude delivered by the oscillator is of 360 mV, when utilizing the primary configuration. Albeit the discrepancy in the amplitude of the output signal being significant, it was decided to maintain the same VDD in all cases.

Figure 70 shows the quality factor of each configuration related to the operating frequency in the VCO. In red, the parallel configuration's quality factor ranges from 5.8 to 12.1, meanwhile, the secondary configuration (in yellow) delivers a quality factor ranging from 5.5 to 9.7. The primary configuration is represented in blue and shows a quality factor from 5.2 to 8 and, finally, the series configuration is shown in green and exhibits a quality factor varying from 6.4 to 9.3. In a nutshell, the quality factors employed by the variable structure in their frequency range of operation, albeit quite low, are in a similar range from all configurations. Therefore, a similar performance is expected from all configurations; obviously, some discrepancies are expected, but limited. This is the result of careful consideration when designing the switches utilized in the variable inductance structure, since altering the width in any

transistor reflects directly in the maximum quality factor and self-resonant frequency delivered by all configurations.

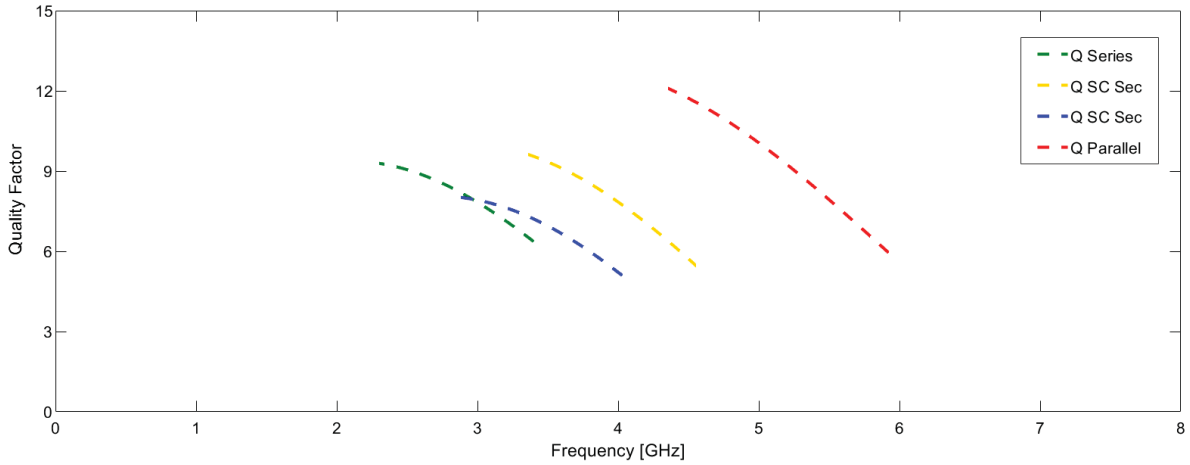

Figure 70 - Quality factor at the frequency range applied in each configuration

A harmonic balance analysis (at around 3.7 GHz) was realized to extract the phase noise and power consumed with a sweep in V_{Tune} (from 0 to 1.2 V with steps of 0.1 V) in order to better evaluate the varactor variable capacitance. The Phase Noise is shown in Figure 71. Once again, aiming to better illustrate VCO's operation, the analysis is separated by the structure's configurations. The parallel configuration exhibits a Phase Noise @ 1 MHz with a worst-case scenario of -109.9 dBc/GHz and a best-case scenario of -116 dBc/GHz, the overall phase noise delivered by this configuration ranges from -108 dBc/GHz to -114 dBc/GHz. The primary configuration shows a phase noise from -110.3 dBc/GHz to -116.6 dBc/GHz. Lastly, the series configuration presents a phase noise ranging from -109.7 dBc/GHz to -117.7 dBc/GHz.

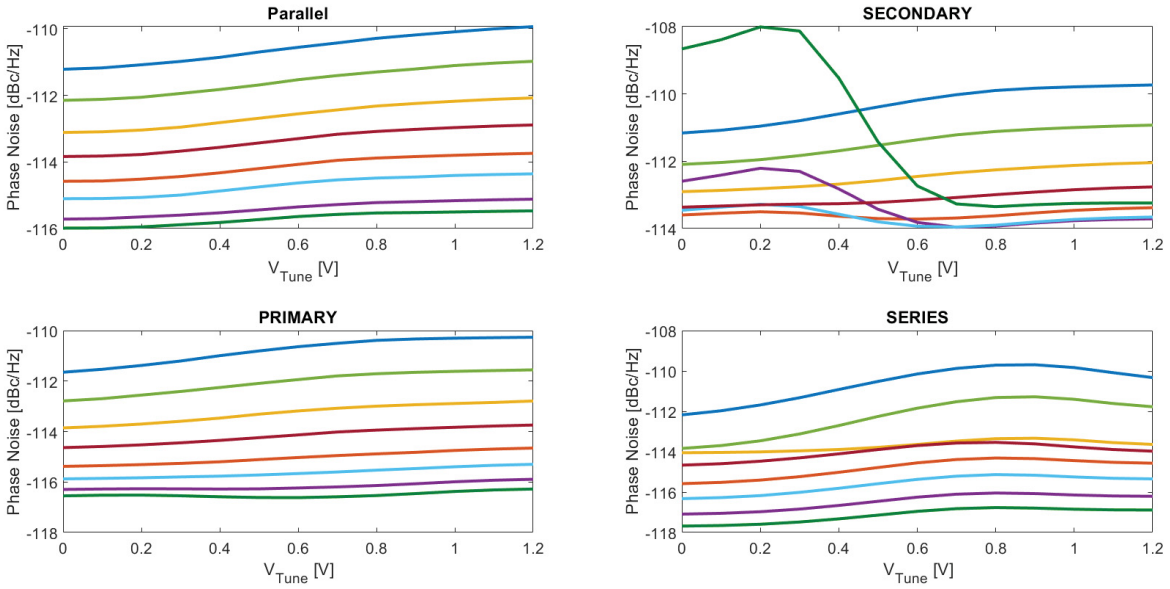

Figure 71 – Phase Noise @ 1 MHz

Figure 72 shows the VCO's power consumption for all configurations. When the parallel configuration is selected, the VCO consumes from 2.62 mW to 3.27 mW, when the secondary configuration is selected, it consumes from 2.91 mW to 3.28 mW. The primary configuration power consumption ranges from 2.69 mW to 3.21 mW and, finally, the series configurations power consumption ranges from 2.53 mW to 3.07 mW. Therefore, it is possible to state that the oscillator consumes a maximum of 3.28 mW, which is lower than the 5-mW threshold stablished in the design phase.

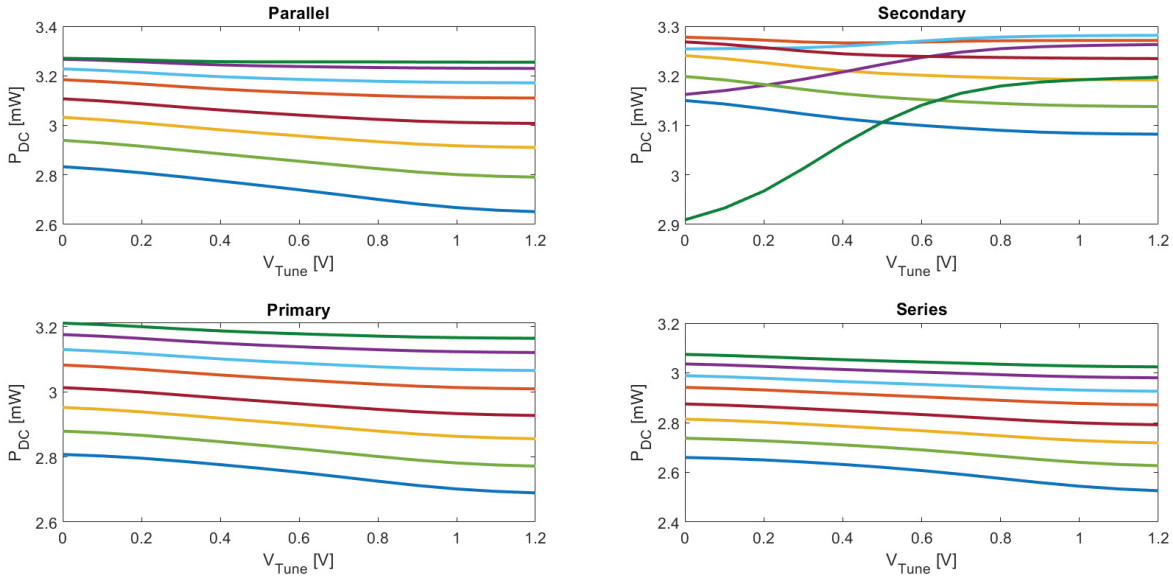

Figure 72 - Power consumption

In order to evaluate the overall performance of wideband oscillators, a common metric utilized is the FoM_T (FANG; YOSHIMASU, 2020), which can be described as:

$$FoM_T = L(\Delta f) - 20\,log\left(\frac{TR\%}{10}\right) - 20\,log\left(\frac{f_{central}}{\Delta f}\right) - 10log\,(\frac{P_{DC}}{1\,mW}). \quad (45)$$

Where L(Δf) is the phase noise at a certain Δf (1 MHz is most commonly utilized), $f_{central}$ is the center frequency of the oscillator, P_{DC} is the DC consumed power and TR % is the percentual tunning range delivered by the VCO. Figure 73 shows the oscillators FOM_T. The FOM_T delivered by the oscillator when the parallel configuration is active varies from - 217 dBc/GHz to - 222 dBc/GHz; when the secondary configuration is active the FOM_T ranges from - 214 dBc/GHz to - 220 dBc/GHz, while the primary configuration is selected, the VCO exhibits a minimum FOM_T of - 217 dBc/GHz to a maximum of -223 dBc/GHz and, finally, when the VCO is operation utilizing the series configuration it delivers a FOM_T varying from -217 dBc/GHz to - 224 dBc/GHz. Therefore, the best FOM_T delivered by the oscillator is - 224 dBc/GHz and the worst is - 214 dBc/GHz.

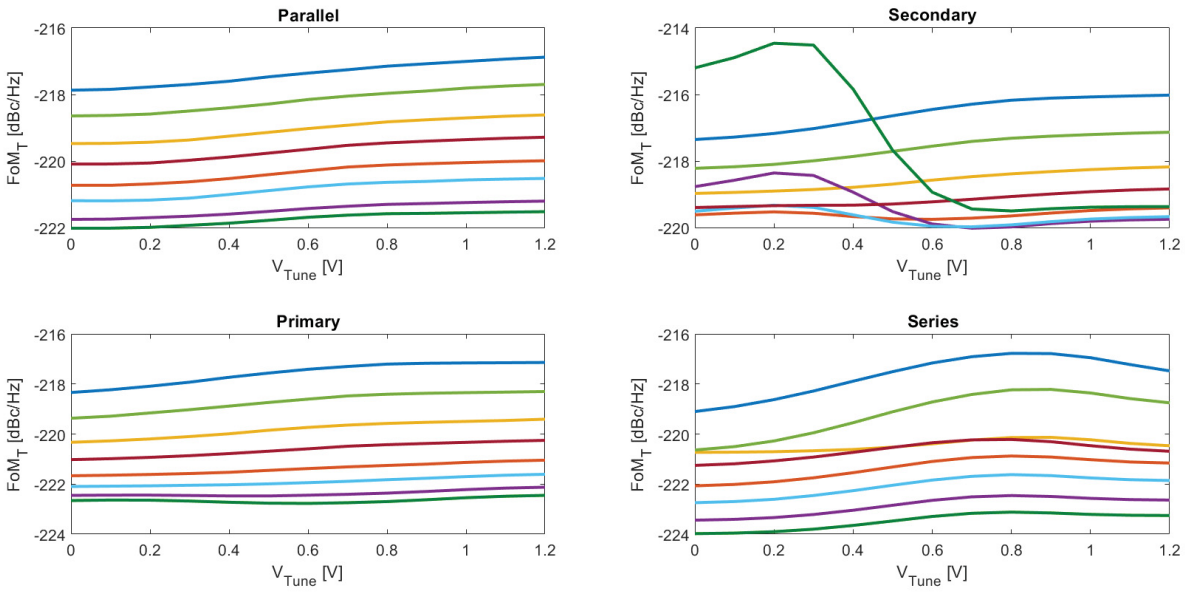

Figure 73 - Oscillators FOM_T

In order to situate the designed VCO in the state of the art, table V was compiled. All works arranged in the table correspond to fabricated circuits, whereas this work's data refers to post simulation results. The data marked with an asterisk represents calculated data and are not directly available in the original works. Two

rows are utilized to describe the results presented in this work, the first row represent worst-case scenario results (not necessarily all parameters stem from the same operation point), the second row represent the best-case scenario results (lower power consumed, higher phase noise and higher FOM_T obtained from the circuit).

Table V – State of the art comparison

	Central Frequency (GHz)	**Tunning Range (GHz)**		**Percentual Tuning Range**	**PDC (mW)**	**Phase Noise (dBc/Hz)**	**FOMT (dBc/Hz)**	**Area (mm^2)**	**Tech. (nm)**
		f_{min}	f_{max}						
(HUANG; HSU; WANG, 2019)	4.05	3.30	5.70	53.0%	3.54	-110.9	- 192.9	1.18*	180
(AQEELI et al., 2015)	5.00	3.45	6.23	57.0%	3.62	-132.4	- 219.6	0.66	130
(DHAMANI; SEPIDBAND; ENTESARI, 2018)	3.70	2.14	4.22	65.0%	15.0	-133.0	- 208.9	0.7	65
(WANG; CHEN, 2016)	6.26	4.60	9.10	65.7%	9.20	-124.2	- 206.8	0.55	180
(SHASIDHARAN; RAMIAH; RAJENDRAN, 2019)	2.45	2.20	2.90	27.0%	1.73	-120.0	- 194.0	0.3	180
(ZOU et al., 2019)	3.70	2.49	4.91	65.4%	6.30	-128.5	- 203.4	0.26	180
(FANG; YOSHIMASU, 2020)	5.18	4.14	6.23	40.3%	0.82	-109.1	- 197.3 / - 178.9	0.44	40
(GUI et al., 2020)	2.15	1.78	2.53	34.8%	28.0	-92.70	- 155.7	0.015	180
(LEONARDO NAKATANI MORETTI, 2021)	2.59	1.37	3.74	91.89%	22.9	-116	-189.8	0.405	130
This Work (Worst Case)	4.12	2.31	5.93	87.9%	3.28	-108	- 214	0.45	130
This Work (Best Case)					2.53	-117.7	- 224	0.45	130

*2 output buffers included

By analyzing Table V, the percentual tuning range of the oscillators utilizing the proposed structure stands out (highlighted in red), being the highest by a significant margin, delivering an extra tuning range to the third highest percentual tunning range. This work's consumed power is another remarkable result, since the designed VCO consumes a similar power that oscillators which deliver a significantly lower percentual tuning range. Due to the somewhat lower quality factor provided by the variable inductance's structure, the phase noise could be considered the weak link of this

oscillator, presenting a substantial difference to the highest phase noise from the researched works.

The FOM_T, which takes into consideration all of the oscillator parameters exhibited by this work's VCO is also in the higher end of the researched works. This can be explained by the higher percentual tuning range provided.

This chapter presented the design process of an LC tank based VCO operating in the 2.3 GHz to 5.9 GHz frequency range from the conception of the variable inductance structure, all the way to the cross-coupled pairs and variable capacitances that allows for a wide range operation. Different metrics were evaluated and compared to state-of-the-art results; this comparison showed that the oscillator utilizing a variable inductance is on par with current developments in wide band oscillator operation.

5 CONCLUSION

The utilization of variable inductances in integrated circuits is being researched for years, and several different solutions were proposed. This expresses the utility that employing a higher versatility to these elements could provide. However, since the integrated inductors performance is directly tied to its geometric construction, variable inductances generally depend on external elements to the coils in order to generate a variation in the element's inductance.

Such elements could be variable capacitances that alter the inductor's self-resonant frequency, switches attached to other inductances that change the equivalent inductance of the device, or even alter the current path creating a different inductance. It is also possible to magnetically couple other inductances to the original element, operating as a transformer; this solution, however, allows only the reduction of the original inductance since, without an external current flowing through the secondary inductance, the magnetic coupling will always be negative. This can be remedied by integrating the secondary inductance to the primary current path, which is the premise of this work.

Almost all of the aforementioned solutions require the implementation of integrated switches. These switches highly influence the inductance performance due to their parasitic capacitance and resistance. Besides, in order to reduce the resistance introduced by NMOS (or PMOS) switches, large transistors are utilized to implement said switches. Therefore, smart placing of the switches and utilization of its characteristics is paramount.

This work discusses the utilization of a composition of switches that provides a maximum of 6 different equivalent inductances. The proposed structure utilizes an integrated transformer with two windings and, through an association of these windings, delivers the equivalent inductances. Besides the inductance in each of the transformer's coils, the magnetic coupling and inductance ratio between the windings influences the equivalent inductances directly. A study of these parameters was presented in order to elucidate their relationships between each other.

The selection of the provided inductances is realized through three NMOS switches connected to the transformer's windings terminals. The switches' status defines the presented inductance by selecting between one of the structures' configurations, which are characterized by the current path through the transformer's terminals. The switches that define the operating configuration are externally controlled

by voltage levels, and its implementation impair the inductances' performance; quality factor and self-resonant frequency are especially affected by the switches' inclusion. This analysis is realized and considered when presenting the structure's design. Finally, it is important to mention that the six delivered inductances are ruled by interdependent parameters, which means that the final inductances will always be correlated (which is an important design limitation).

In order to illustrate the potential of the proposed structure, a voltage-controlled oscillator was designed. It utilizes only four of the six modes (since some modes would present worse results), however, even by only utilizing four modes it showed a frequency range significantly higher than works operating in similar frequencies. The VCO's design methodology is presented, including the variable inductance structure, illustrating design choices, such as the almost inexistant magnetic coupling between transformer's coils, and the switches parameter's sizing. Also, the capacitor bank and associated varactors required to fulfill the frequency range, avoiding blind zones and guaranteeing some overlap between the banks' modes (and also the different variable inductance configurations).

Lastly, the cross-coupled pair needed to be carefully designed in order to limit the power consumption and, most importantly, ensure the oscillatory operation and desired frequency scope. Since the proposed structure delivers a somewhat low quality factor due to the switches' degradation, the phase noise delivered is on the lower end when compared to the state-of-the-art options, however, due to the multi-inductance provided by the proposed structure, its wide tuning range is noteworthy; the VCO also presented a low power consumption if compared to the provided percentual tuning range.

The designed VCO presented a tuning range of 87.9%, varying from 2.31 GHz to 5.93 GHz. The power consumption is essentially between 2.53 mW to 3.28 mW, while the phase noise ranges from -108 dBc/Hz to -117.7 dBc/Hz at 1 MHz. The worst obtained FoM_T is - 214 dBc/Hz while the best FoM_T presented by the VCO is - 224 dBc/Hz. All in all, the proposed oscillator shows great promise and, if fabrication could be on the horizon, the presented data suggests that it could present important results.

5.1 FUTURE WORKS

An interesting point of future research would be different switches topologies that could lessen the impact caused by current the utilized topologies. One example is replacing the floating body technique by a switching body technique. Other switches topologies could be utilized as well, aiming to improve the quality factor and self-resonant frequencies impaired by the inclusion of the three switches.

Another point of study, could be the utilization of DPDT switches instead of the utilized SPST switches (or a composition of both). The overall structure would need the be readapted, but the described configurations could still be utilized.

Other possibilities include the addition of extra variable inductances to the structure, such as adding a switched third winding in the transformer, able to reduce the delivered equivalent inductances (which would further increase the number of different inductances that the structure could deliver).

Different transformers topologies could also be analyzed, such as the utilization of 8-shaped coils, or the effects of utilizing different topologies in each winding. The implementation of horizontal coupling in a more adequate technology could also present improvements to the overall structure.

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