UNIVERSIDADE FEDERAL DO PARANÁ

RODRIGO GODINHO SILVA

SIMULAÇÃO E PROJETO DE INDUTORES INTEGRADOS EM TECNOLOGIA CMOS PARA CIRCUITOS DE RADIOFREQUÊNCIA

CURITIBA

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SIMULAÇÃO E PROJETO DE INDUTORES INTEGRADOS EM TECNOLOGIA CMOS PARA CIRCUITOS DE RADIOFREQUÊNCIA

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Orientador: Prof. Bernardo Rego Barros de Almeida Leite
Coorientador: Prof. André Augusto Mariano

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ANDRÉ AUGUSTO MARIANO
Avaliador Interno (UFPR)

Dep.Eng.Elétrica-DELT, Centro Politecnico - UFPR - Curitiba - Paraná - Brasil
CEP 81531990 - Tel: 41 3361-3622 - E-mail: ppgee@eletrica.ufpr.br

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RESUMO

Este trabalho apresenta um passo a passo para qualificar a utilização de simulações eletromagnéticas com a finalidade de prever o comportamento de elementos passivos, especialmente indutores. Três dispositivos foram projetados, medidos e simulados. Tratam-se de dois indutores de duas camadas em que um deles possui uma estrutura de blindagem de substrato e um indutor de apenas uma camada (também com a blindagem). Os três elementos apresentam uma topologia octogonal simétrica. Os elementos são detalhados, bem como suas topologias e parâmetros construtivos. Para a análise individual dos dispositivos, o desacoplamento dos elementos externos é realizado. Figuras de mérito e parâmetros de análise são estabelecidos e utilizados para examinar a operação dos indutores através da comparação entre eles, visando demonstrar o efeito de certos parâmetros de projeto na performance dos elementos. A simulação eletromagnética é analisada através da comparação entre as figuras de mérito obtidas através da medição dos elementos e os dados obtidos pelas simulações. Investigam-se os parâmetros de análise para identificar causas de possíveis discrepâncias entre a simulação e os circuitos medidos. As simulações eletromagnéticas apresentaram resultados próximos às medidas, entretanto, algumas configurações podem ser melhor exploradas, o que poderia levar a melhores resultados. No pior caso, as simulações eletromagnéticas apresentaram uma discrepância de 15,7% no fator de qualidade máximo, 2,3% na frequência de ressonância e 9,9% na indutância de baixa frequência em relação aos dados obtidos da medição.

Palavras-Chave: Indutores, Simulações Eletromagnéticas, Microeletrônica

DESIGN AND SIMULATION OF INTEGRATED INDUCTORS IN CMOS TECHNOLOGY FOR RADIOFREQUENCY CIRCUITS

ABSTRACT

This work presents a step-by-step process to determine the applicability of electromagnetic simulations to predict inductor behavior. Three elements were designed, measured, characterized and simulated. These elements are a shielded double-layered, a shieldless double-layered and a shielded single-layered symmetric inductor. The elements are presented, their topology and constructive parameters are described and their differences are discussed. The devices were measured and the data were adapted as necessary. To evaluate the elements performance (as well as the simulation) analysis parameters are established and detailed. The elements' parameters are compared and discrepancies are highlighted. The performances of these elements are rated according to figures of merit such as equivalent inductance (5.1 nH for the double-layered elements and 5.5 nH for the single-layered), maximum quality factor (11.2 for the shielded double-layered, 12.2 for the shieldless double-layered, and 10.3 for the single-layered inductors) and self-resonant frequency (6.84 GHz, 6.89 GHz, and 8.3 GHz, respectively). The electromagnetic simulation presents results close to measurement; however, exploring not tested configurations could lead to improvements. In the worst presented case, the maximum quality factor displayed a discrepancy of 15.7%, the self-resonant frequency presented a 2.3% discrepancy, and the low frequency inductance showed a 9.9% difference between simulation and measured data.

Keywords: Inductors, Electromagnetic Simulations, Microelectronics

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LIST OF SYMBOLS

BEOL	–	Back end of line
DRC	–	Design Rule Checking
DUT	–	Device Under Test
FDTD	–	Finite Difference Time Domain
FEM	–	Finite element method
GF	–	Global Foundries
MoM	–	Method of Moments
PNA	–	Programmable Network Analyzer
RF	-	Radiofrequency

SUMMARY

1.INTRODUCTION

1.1. CONTEXT

The recent evolution in radiofrequency (RF) devices and integrated circuit technologies greatly expanded the number of wireless applications [1]. This expansion generated a growing demand for semiconductor manufacturers, requiring a higher integration in RF circuits. However, as passive device performances are directly tied to their geometry (especially for inductors), they end up being the bottleneck on radiofrequency circuitry integration.

Inductors are of utmost importance in radiofrequency circuits [2]. These devices are employed in critical building blocks of RF circuits such as intermediate frequency filters [2], low-noise amplifiers [3], voltage-controlled oscillators [4], and power amplifiers [5]. In order to reduce cost and size of these circuits, on-chip inductors are replacing their off-chip counterparts. As the performance of on-chip inductors directly affects the behavior and cost of the chip, these devices are of elevated importance [6], [7].

In order to maximize the performance while limiting the passive elements size, modification in the standard CMOS process can be introduced. These modifications encompass the use of thicker metal levels [8], employing dielectric layers with increased permittivity [9], and even altering the substrate characteristics [10]. These techniques, however, involve additional processing steps that increase the fabrication costs. This goes against one of the main purposes to look for size reduction in integrated RF circuits: minimizing costs. This requisite can also be achieved through design optimization.

Aiming to facilitate passive devices design optimization, foundries usually provide libraries with a set of predetermined passive elements, along with parameterized layouts and electrical models. By taking advantage of these predesigned elements, the designer can easily design devices with adequate performance. In some instances, however, these provided elements are not sufficient to comply with the required performance. In these cases, extra degrees of freedom in the design of passive devices are essential and can provide the necessary flexibility

to generate the expected results. This implies that the designer possess a certain degree of knowledge on these passive devices operation.

Therefore, achieving an understanding of inductors (and other passive devices) operation is vital. That should be possible through the analysis of a large quantity of data from different elements with different topologies and characteristics. This method, however, requires a high amount of time and its cost is elevated. An alternative solution is the analysis of the foundry-provided electrical models, but these models are typically optimized to specific frequency ranges and are limited to the predesigned provided elements. The method adopted in this work refers to the use of electromagnetic simulations to predict inductors behavior that are applicable to virtually any inductor geometry, providing a flexibility not found with the other methods. This flexibility allows the expansion of this work to a number of different elements (such as magnetically coupled double-layered inductors, and any manner of inductor topology as well as transformers).

Several works adopt electromagnetic simulations to characterize inductors. In [11], the influence of the metal layer thickness in spiral inductors is examined through 3D electromagnetic simulation. In [12], the sensitivity of inductors performance in relation to several constructive parameters is investigated. An accurate electromagnetic simulation comparing different simulators, as well as measurement processes of millimeter-wave inductors is presented in [13].

In order to evaluate the electromagnetic simulations proficiency, three inductors were fabricated. The use of electromagnetic simulations to predict an inductor behavior is widely applied.

This work possesses two main objectives. First, to perform a characterization of three manufactured devices, to present an analysis of the changes in performance based on the design choices applied to each instance, and to define the causes for the aforementioned changes. This will lead to a better understanding of these inductors behavior.

The second main objective is to evaluate the adoption of electromagnetic simulations in order to predict inductor behavior. This will serve to provide an increased degree of freedom when designing inductors, as the dependence of foundry-provided models would no longer be an issue.

The achievement of these objectives is key to develop a design methodology for these crucial elements and, ultimately, to extrapolate the process to any type of device not provided by foundries (such as alternate topologies or transformers).

1.2. METHODOLOGY

This work was divided in three main sections: the background research, the design and electromagnetic simulations of the inductors and, lastly, the measurement data and analysis. Figure 1 specifies the project's workflow.

Starting with the bibliography research, which was comprised by a general inductance study, followed by presenting largely utilized inductor models and its main analysis parameters. Important figures of merit for integrated inductors analysis are presented; as well as industry utilized integrated inductor topologies and its main characteristics. From there, a desired topology was selected. The de-embedding process is then explained as well as the electromagnetic simulation types.

The following step is to draw the layout. Before starting the layout design though, it is interesting to analyze and comprehend the technology characteristics for passive devices, such as physical characteristics of the layers and placement levels, which determine the optimal layout attributes. In order to extract the technologic advantages to the fullest, the technology library was investigated. Based on the available topology options, a guideline for the designed layout, as well as the elements building parameters, was chosen. With these characteristics defined, the layout procedure took place. In this phase, not only the selected inductors were inserted, but also the complete circuit around it, such as feed lines, pads and ground planes. Afterwards, the circuit was sent to fabrication.

Creating a coherent simulation environment is primordial to guarantee the simulations adequacy. This involves configuring a number of elements in a manner that the simulation environment is as close as possible to the utilized technology, as well as attributing the correct configurations to the layers in use. To guarantee the simulated design's fidelity to the fabricated circuit, the layout was imported to the simulation environment. After importing the layout, the simulation's configuration and execution began. In this step, the library's technology model served as guideline to realize the required configurations. This practice, however, can only be used as a

starting reference point for the simulator settings, which would be refined according to the measured data.

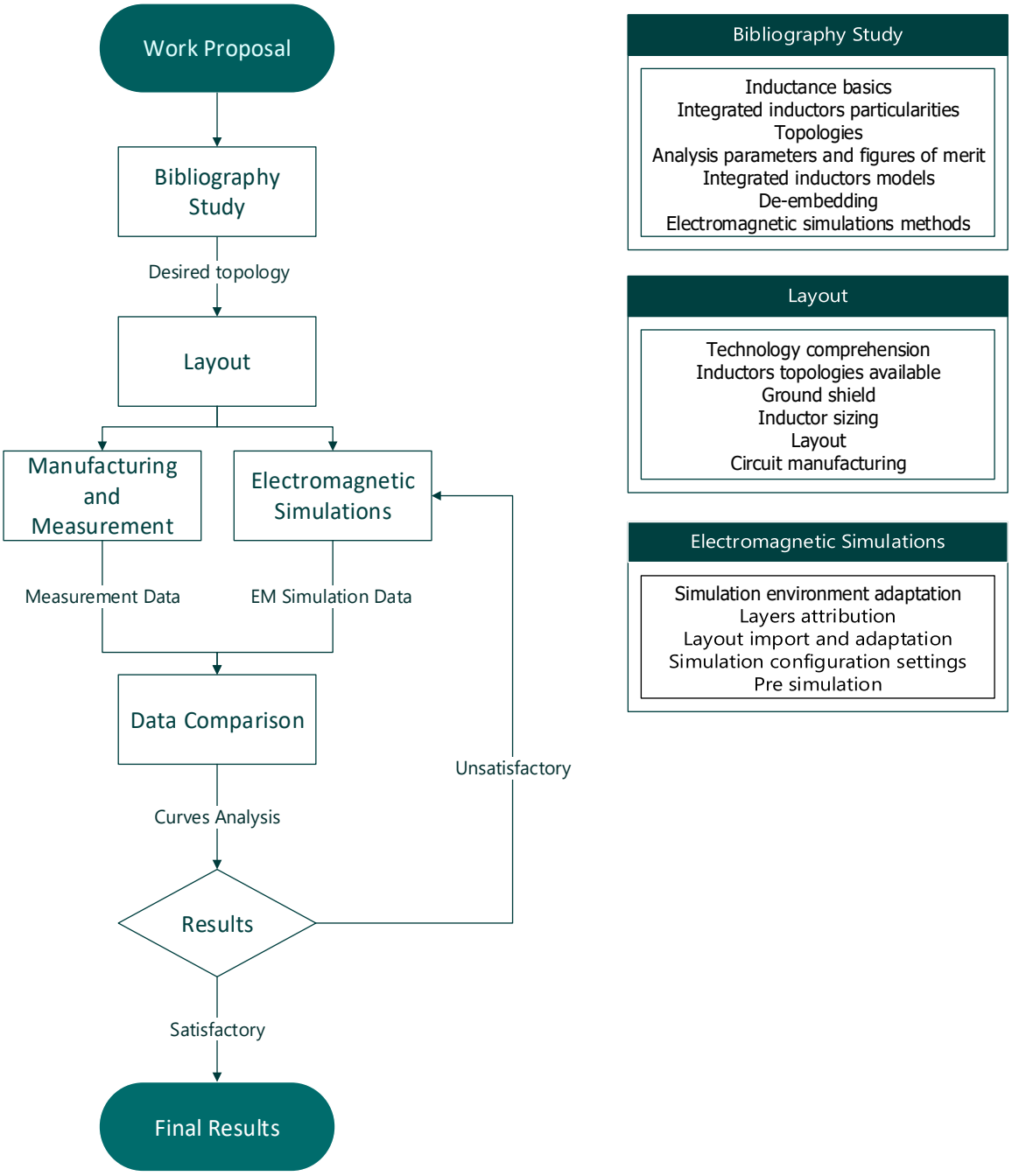

Figure 1 - Project development flow

The inductors' measured data were compared amongst each other and the fabricated inductors' characterization was devised. The analysis is divided in series branches, parallel branches, and figures of merit (equivalent inductance and quality

factor). After the characterization of the fabricated devices, the simulation data is compared to the electric model provided by the foundry (when applicable) and the data extracted from the elements` measurement. All of the aforementioned steps will be further detailed in the chapters to come.

2. BIBLIOGRAPHY RESEARCH

This chapter lays the knowledge foundation utilized through the project. The basics on inductance are presented, followed by integrated inductor specifics considerations. A number of different topologies are described and analysis parameters are explained. A study of models, used to describe integrated inductors and employed figures of merit, is introduced as well. The de-embedding process is discussed and, finally, types of electromagnetic simulations are presented.

2.1. INDUCTANCE

Inductance is an intrinsic property of every circuit where there is current flowing; it is related to the circuit's physical geometry. A common definition to inductance made in terms of flux linkage (that represents the sum of all magnetic fluxes applied to a specific element) ψ and the electric current flowing through the element I is determined by: [14].

$$L = \frac{\psi}{I} \quad (1).$$

The voltage applied to the inductor will depend on its self-inductance L, and the variation rate of the current. If there is another coil affected by the same magnetic flux, the correlation between the incited current and the voltage in the second coil is dependent from the mutual inductance M. These principles are exposed in [15]; as this work focus on inductors alone, the mutual inductance study will be neglected. The correlation between current and voltage is represented by:

$$V = L . \frac{dI}{dt} \quad (2).$$

As discrete inductors can reach inductances of hundreds of henry [16], their integrated counterparts are largely restricted due to its limited size and adverse environment (mainly caused by lossy substrate and relatively high resistivity metals). Practical on-chip inductances are in tens of nanohenrys [17].

2.2. Integrated Inductor Considerations

The integrated circuit fabrication process involves two distinct portions. The front end of line (FEOL), which refers to the first part in a wafer manufacturing line, and the back end of line (BEOL), that is where the metal interconnections are placed and where inductors are designed.

One of the most basic structure used when designing these elements is the ring inductor, shown in figure 2. This element's inductance and resistance are functions of the loop area and perimeter. The cross section of the ring plays an important part in the inductor's resistance; the larger the cross section, the smaller the resistance. This is obtained by increasing the ring width or height.

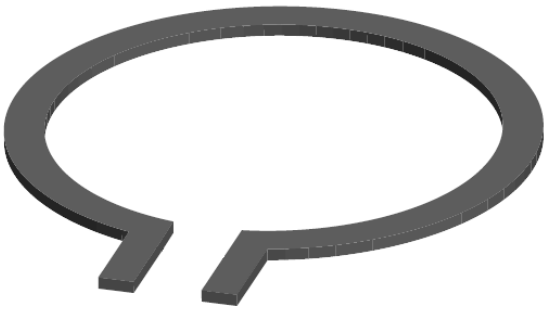

Figure 2 - Ring inductor [14]

When this structure is placed within an integrated circuit, a significant capacitance caused by the proximity to a conductive substrate appears [14]. This capacitance, illustrated in figure 3, is detrimental to the inductor performance; for this reason, integrated inductors are usually placed as far from the substrate as possible. In RF oriented technologies, the higher metal layers are also thicker, which is favorable to reduce the inductor resistance.

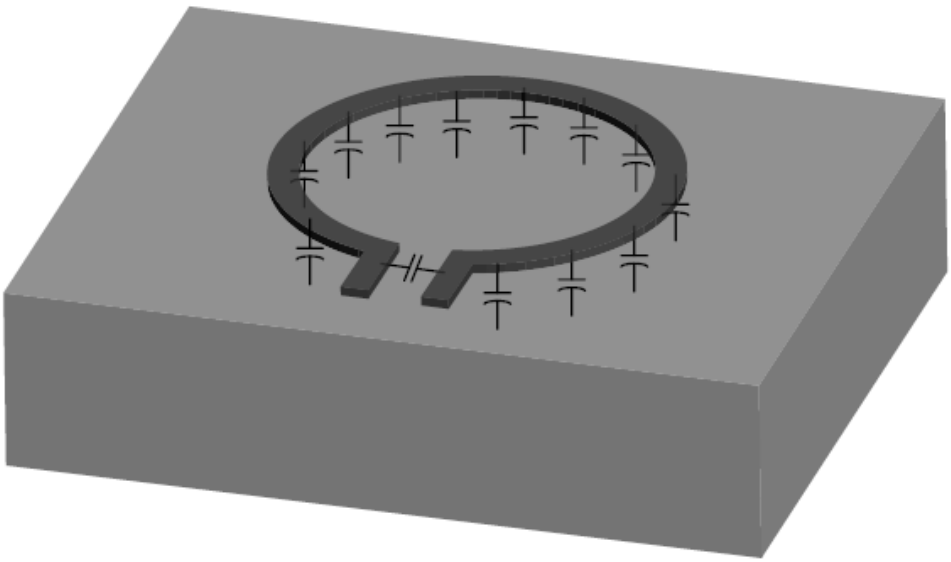

Figure 3 – Ring inductor substrate capacitance [14]

One approach to mitigate the substrate coupling is to insert a shield. This shield cannot be solid as the eddy currents would flow at the shield and reduce the inductance. In order to prevent electrical fields from penetrating the substrate and prevent eddy current flow, patterned shields are employed [14]. Some examples can be seen in figure 4.

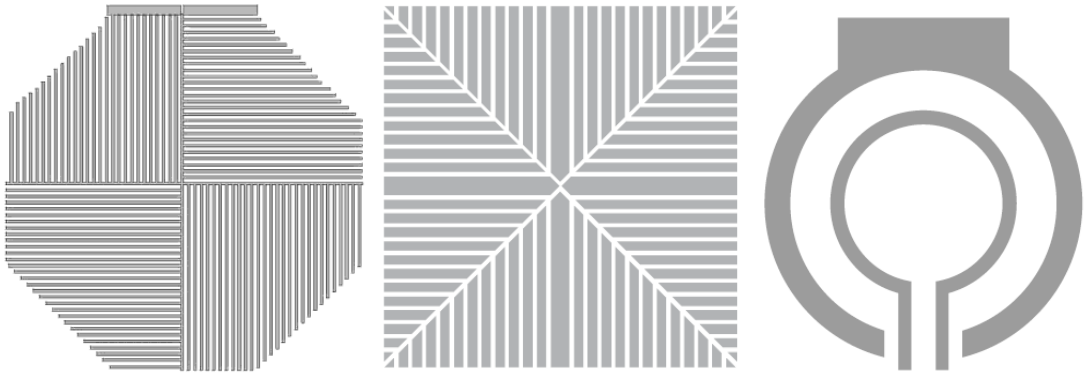

Figure 4 – Patterned shield examples [18], [14]

Despite generally increasing the quality factor, the insertion of a shield, however, also reduces the self-resonant frequency. In general, the silicon substrate is grounded at the bottom, and it is possible to reduce the electrical resistance of the substrate by grounding the shield, which minimizes the substrate electrical loss. This is a consequence of the growth in the capacitance between the spiral and the substrate, as the patterned shield is closer to the spiral than it is to the substrate.

As mentioned before, the resistance of a loop can be lowered by increasing the structure's width. However, at higher frequencies, the current tends to flow through the surface of the structure, which reduces the active cross section to the area in which most of the current actually flows, increasing the exhibited resistance. This phenomenon is called the skin effect.

2.3. TOPOLOGIES

Several different characteristics can be attributed to an inductor based on its topology, such as symmetry, occupied area, quality factor, inductance, series resistance. Altering an inductor's topology will have an effect in all of these characteristics. This is why choosing the topology of an inductor is a step of great importance. Therefore, an investigation of existing topologies is presented.

Normally, the most popular are the square, hexagonal, octagonal, and circular structures. These structures are presented in figure 5. Increasing the number of sides in these topologies causes a growth in the resistance and inductance of these elements, albeit the inductance suffers a higher growth than the resistance. Considering this, the circular geometry provides the largest perimeter for the same radius, which maximizes the inductance and quality factor of this topology [19]. However, it is not possible to ideally reproduce this format due to the angle limitations between tracks imposed by the manufacturing technologies. Therefore, circular inductors are used in ideal calculations only. Typically, they are extrapolated to a polygon with many sides. The work in [20] presents ways to estimate the inductance of these topologies. These structures can be divided into symmetric and asymmetric.

The shape of the inductor depends on the utilized technology, which dictates the allowed angles for their metal tracks through its design rules. Square inductors require 90 º angles, hexagonal spirals 60 º and octagonal structures require 45 º angles.

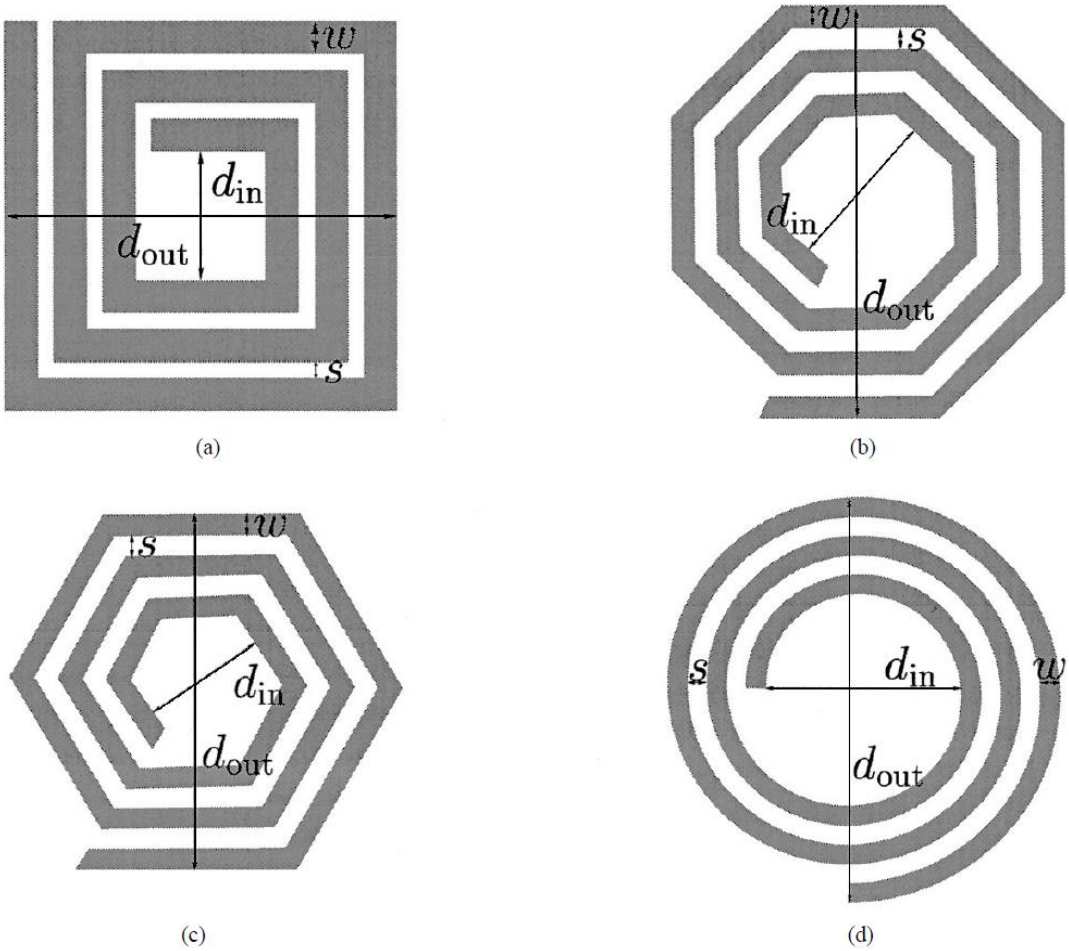

Figure 5 – (a) Squared inductor (b) Octagonal inductor (c) Hexagonal topology (d) Circular topology [20]

This type of horizontal topology is placed in the topmost metal layer, as it possesses the maximum available distance to the substrate in the technology (which minimizes the parasitic capacitance between the inductor and the substrate) and is the thicker layer available (which reduces the inductor's series resistance).

The horizontal spiral can be arranged in a symmetrical topology, which is used for fully balanced differential circuits. In addition, the spiral center point does not move electrically if the structure is excited by a fully balanced signal that allows for a number of different applications.

Figure 6 presents the 3D model of a vertical inductor topology (VI). In [21] this topology is compared to a symmetric one-looped, a symmetric two-looped and an asymmetric four-looped octagonal inductors, and some conclusions can be ascertained. This topology is exceptional in saving area [21], presenting an inductance density (inductance per occupied area) well above the horizontal topology inductors

and its unidirectional design makes it useful for placing it in small gaps. However, the consequences of the magnetic flow flowing through the BEOL metals is not analyzed and its performance is subpar, producing a much lower equivalent inductance, quality factor and resonant frequency. This topology certainly is interesting if the designer goal is to save chip area, and does not need an inductor that requires a high performance.

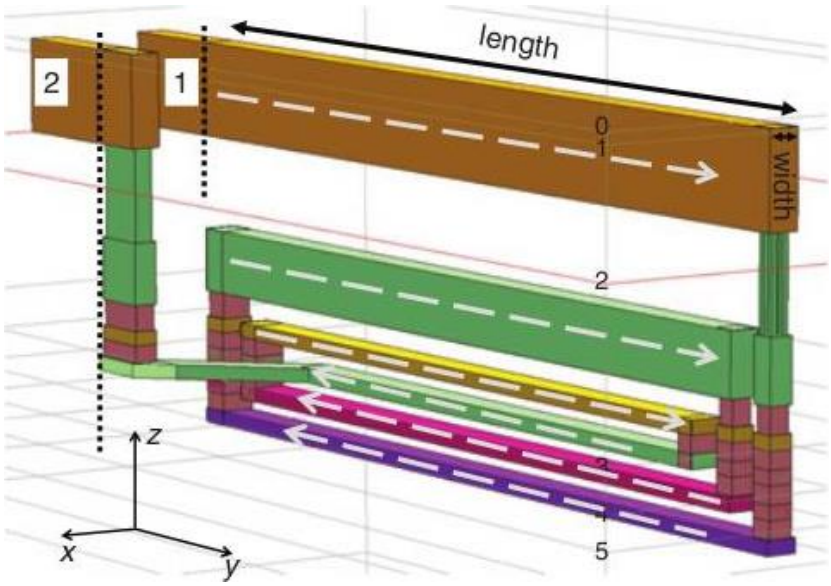

Figure 6 – Vertical inductor [21]

The next topology is a helical inductor, whose 3D diagram is presented in figure 7. This topology presents a similar structure as seen in discrete inductors and, as mentioned in [22], produces a better inductance than its planar counterpart (which is understandable as the solenoid format takes advantage of its multiple same sized spirals in the same magnetic field). However, the helical topology suffers in terms of self-resonant frequencies. Its quality factor is approximately the same for the planar and helical inductors analyzed in [22].

These vertical topologies, however, possess a limitation in number of spires as they are linked to the number of layers present in the utilized technology, which can be detrimental to their performance.

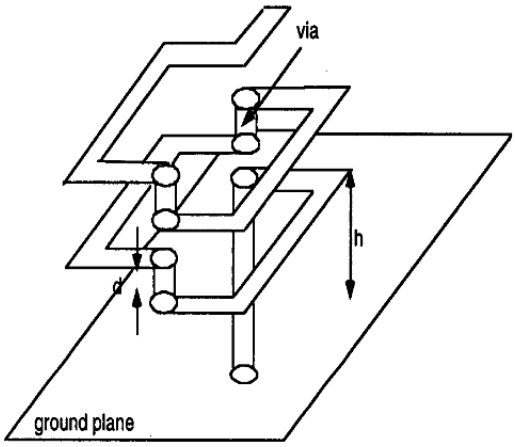

Figure 7 – Schematic diagram of a 3D helical inductor structure [22]

2.4. Analysis Parameters

A 2-port network is presented in figure 8. In order to characterize this network, its scattering parameters (S-parameters) can be extracted for a given reference impedance (usually 50 Ω in RF). A 2-port network presents four S-parameters (S_{11}, S_{12}, S_{21} and S_{22}). S_{11} is related to the reflection coefficient in port 1, S_{22} to the reflection in port 2, S_{12} is the reverse transmission coefficient and S_{21} is the direct transmission coefficient. In the case of passive networks, S_{12} and S_{21} are equivalent, representing the device's insertion loss.

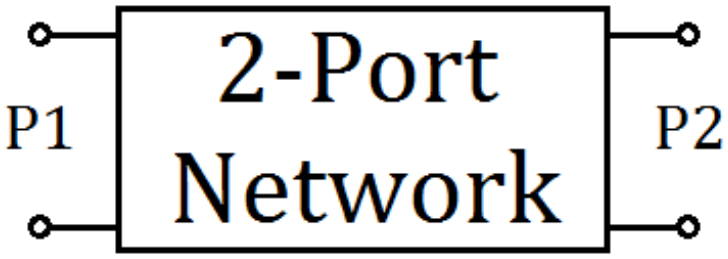

Figure 8 – Generic 2-port network

The analysis of inductive behavior through the scattering parameters is not necessarily the best option, though. With some algebraic manipulation, it is possible to extract the admittance parameters (Y-parameters) of a network from its scattering parameters. A π model can be used to describe the configuration of integrated inductors. By arranging the Y-parameters in this model, it is possible to achieve an understanding of the main loss mechanisms present in integrated inductors.

In figure 9, the shape in which the Y-parameters are arranged in the π model is presented. By analyzing this topology, we can conclude that the series branch is related to the Y_{12} parameter, and the shunt branches correspond to $Y_{11} + Y_{12}$ and $Y_{21} + Y_{22}$. Based on this configuration, a number of inductor models can be used.

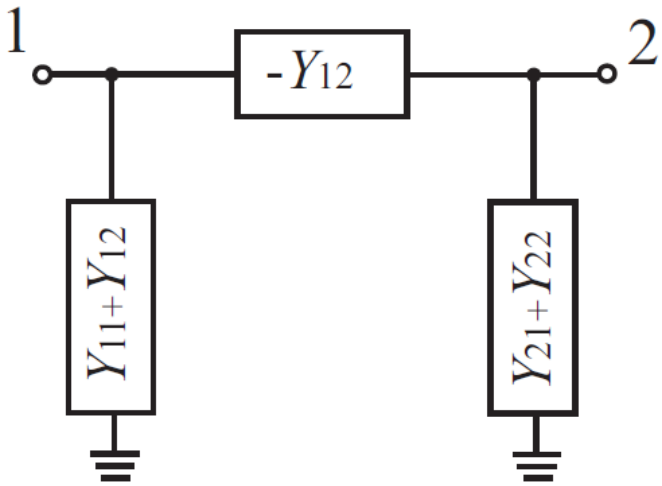

Figure 9 – Y-parameters π model [23]

2.5. Integrated Inductor Models

To analyze inductors, two main methods can be utilized. The analysis as a one-port network, grounding one of its terminals and evaluating the other terminal response; or analyzing the inductor as a 2-port network, where both terminals adopt the same reference. Figure 10 shows a one-port analysis, where all of the circuit parameters correspond to the impedance between the positive and negative port terminal [24].

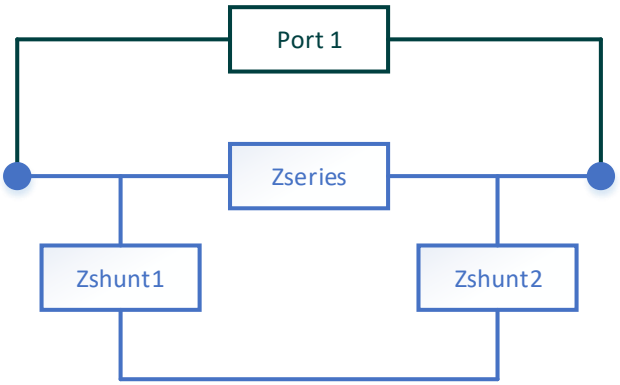

Figure 10 – One-port analysis

In Figure 11 is possible to observe that the 2-port network configuration provides data for all possible combinations of port 1 and port 2 connected to ground. This includes a differential connection between the pins [24].

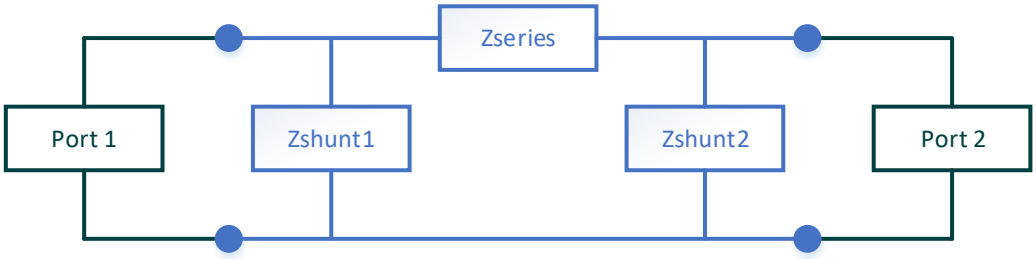

Figure 11 – Two-port analysis [24]

This configuration provides the possibility to analyze a variety of information, especially parasitic characteristics. Characteristics such as ohmic loss of metal wire, inter-coil capacitance, inductive and capacitive coupling with the substrate [25], that appear as series and shunt elements in the analysis (also presented in figure 11). In addition, if needed, the one-port configuration data can be extracted from this method through algebraic manipulation.

By working on these series and shunt elements, it is feasible to propose an equivalent circuit that functions as an equivalent model for the inductor's 2-port data. A π topology is typically employed. In this section, three different models and its parameters are presented and analyzed.

Figure 12 presents a high frequency π topology model. This model can be separated into series and shunt branches. The series branch is composed by C_o, R, L, R_s and L_s. C_o represents the overlap capacitance between the spiral and underpass metal lines, R_s and L_s characterizes the low frequency series resistance and inductance of the spiral. The R and L elements emulate the skin effect at the inductor that appears as the frequency rises, which causes the current to flow at the conductor's surface [26].

The shunt branch is formed by C_{ox}, that represents the metal-oxide capacitance, C_{sub} representing the substrate capacitance and finally R_{sub}that portrays the substrate resistance's effect. The possible asymmetry of an analyzed inductor will be seen by differences in the left and right segments [26].

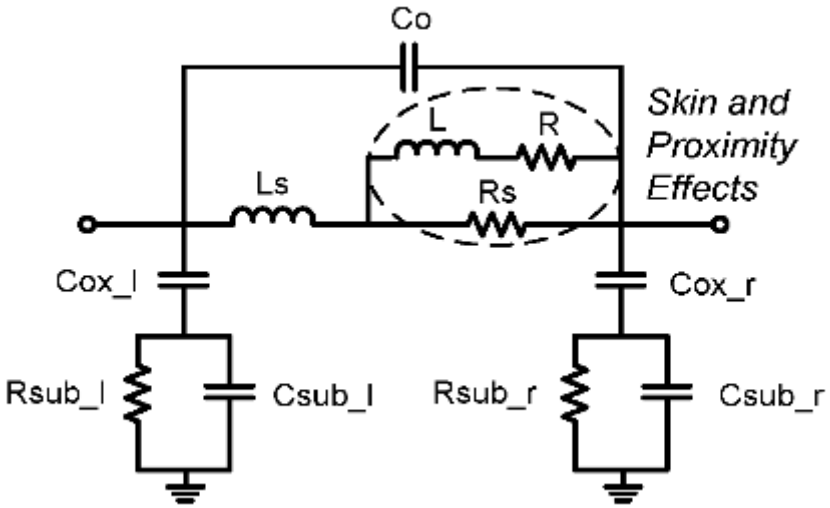

Figure 12 – High frequency π model [26]

As mentioned in [26], the single π model could not reflect the decrease in effective series resistance at high frequencies caused by the substrate coupling. The double π model presented at figure 13 was devised in order to remedy that. To exercise this model, the analysis of the inductor is separated in two segments along its length and a single π model is generated for each segment. The first segment's characteristics are presented at the model's left side whereas the second segment is shown at the circuit's right side. Each segment would then generate its own cell that is combined to form the complete double π model [27].

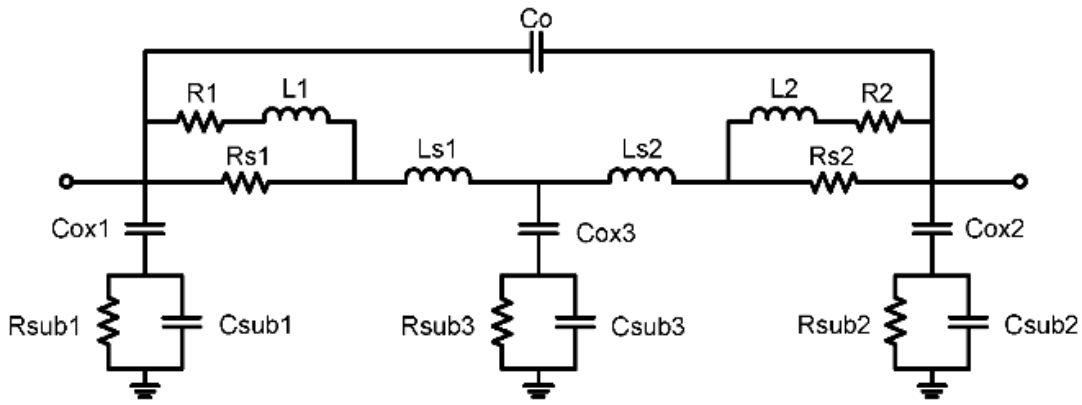

Figure 13 – Double π model [26]

This model possesses a third section and is formed through a combination between the shunt branches of both cascading single π cells [26], which were generated by the first and second sections of the inductor.

In order to obtain a simplified electrical model, it is possible to divide the series and parallel branches presented by the π model into their real and imaginary portions. The series branch portrays the characteristics of the winding where its real segment can be analyzed as the winding resistance and its imaginary segment is considered the winding inductance.

Likewise, the shunt branches portrays the relation present between the spiral and the substrate. These branches are divided into a capacitance and a resistance (determined by the imaginary and real portions of the branches, respectively). These relations are shown in figure 14.

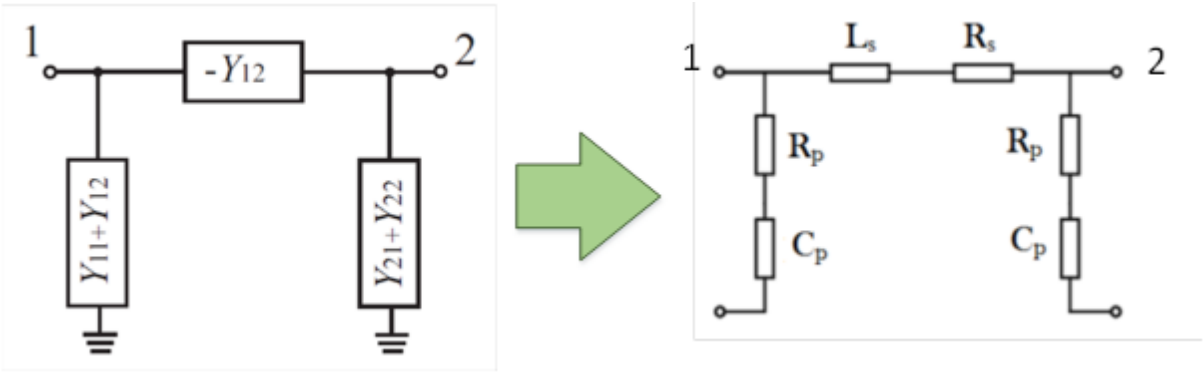

Figure 14 – π model relation to the simplified model

In order to improve the performance of the inductor, its series resistance must be reduced. By analyzing the classical low-frequency resistance formula,

$$R = \frac{\rho . l}{w . t} \tag{3}$$

where ρ is the resistivity, t is the height, w is the width and l is the length of the conductor, we can perceive the design choices related to reducing this resistance. The height and resistivity are tied to the technology utilized, therefore cannot be altered, which leaves the length and width of the conductor. Increasing the width of reducing the length will lead to a reduction in the winding resistance.

Several formulae are proposed to describe the inductance of an integrated spire; [15] proposes the following equation:

$$L = \frac{0{,}42 . \mu_o}{\pi} l \left(ln \left(\frac{2l}{0{,}2235 . (w + t)} + \frac{0{,}2235 . (w + t)}{l} - 1 \right) \right) \tag{4},$$

where μ_0 is the material permeability and is determined by the technology. Once again, the spire's width and length dictate this parameter. However, in order to increase the inductance, an increase to the conductor's length is required, which will increase the element's resistance.

The analysis of an integrated inductor is not restricted to its spire, as the capacitive effect between the element and the substrate is substantial. This capacitance is represented in the imaginary portion of the parallel branch. The classical parallel plates capacitance formula,

$$C = \varepsilon \frac{w.l}{d} \tag{5}$$

where ε is the material permittivity and d is the distance between the plates and are tied to the technology, describes this capacitive effect. As this effect is detrimental to the inductor's performance, its reduction is essential. Consequently, the reduction of the width and length and increase of the separation distance between the inductor and the substrate are desired. In order to maximize the separation distance, inductors are typically placed in the superior layers of the technology. The ambiguous relation between these constructive parameters (as well as technology limitations) illustrates the complexity involved in designing inductors.

The simplified model is highlighted in figure 15 and an alteration in the nomenclature is also proposed (where the resistances shift to represent the real segment of the branches, and the inductance and capacitance shift to represent the imaginary portion). This equivalent circuit can express characteristics of on-chip inductors and its elements can be derived from the Y-parameters. This is important in an analytical point of view, as it eases the perception at possible discrepancies between data [23]. This analysis will be presented in subsequent chapters.

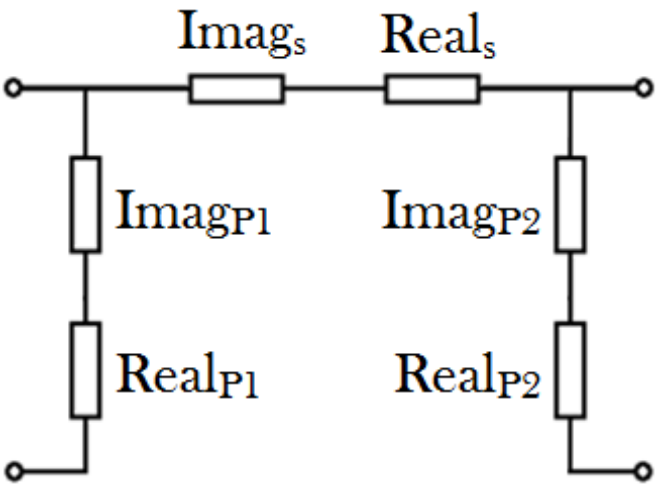

Figure 15 – Simplified π model

2.6. Figures of Merit for Inductors

A figure of merit is a metric utilized to evaluate the performance (or effectiveness) of a certain system. They are established from one (or more) characteristics of said system. There are two fundamental figures of merit that are used to characterize (and will be analyzed through this work) the performance of on-chip inductors: equivalent inductance and quality factor.

The equivalent inductance represents the inductance that the inductor presents including the effect of its own parasitics and can be determined by:

$$L_{eq} = \frac{imag\ (^1/_{Y_{11}})}{\omega} \quad (6).$$

The quality factor fundamental definition relates the maximum energy storage and the average power dissipation. However, accurately estimating the quality factor by this approach is complex [28]. Therefore, the most utilized interpretation involves the difference between the average magnetic and electric stored energies [29] and is defined by

$$Q = -\frac{imag\ (Y_{11})}{real\ (Y_{11})} \quad (7).$$

As this definition is easy to derive from the network parameters, its implementation is fairly convenient for comparing inductors operations characteristics and is considered a standard practice in the industry [30].

Another important metric is the self-resonant frequency, which is defined as the frequency at which the inductor resonates with its own parasitic capacitances. For frequencies higher than the self-resonant frequency, the inductor behaves as a capacitor [31]. Therefore, this metric corresponds to the frequency in which the equivalent quality factor and inductance reach zero.

2.7. DE-EMBEDDING

As integrated circuits are composed of micrometric (or even nanometric) structures, elements of interest can only be accessed through inserted devices called pads. In order to analyze a specific device from these circuits, the effect of the surrounding structure must be eliminated from the measured data. The process utilized to decouple these elements' data is called de-embedding.

As a broad definition, the term de-embedding can be conceptually used to refer to any mathematical shift of the electrical reference planes. As the electrical characteristics of a circuit are not always directly measurable at the reference planes of interest, the possibility of moving these planes is of great utility in the areas of microwave measurements. By shifting the reference planes closer to the device under test (DUT), it is possible to dismiss unwanted contributions from the measurement setting removing the embedded influences present at the measurement data, allowing for a precise analysis of the desired device [32].

There is a variety of de-embedding techniques, such as Thru-Reflect-Line (TRL) [33], Thru Only (TL) [34], Open-Short [35], etc. However, these methods typically require at least two extra fixtures (be it a thru, an open, or short fixture) and are used for higher frequency systems. The Open pad method provides reasonable results utilizing only one element to perform the de-embedding [36]. This process is also fairly simple to be applied, as a simple matrix subtraction is needed. To apply this method, we assume that the parasitics leading to the DUT can be described as a parallel admittance Y_p connected to the circuit's ports as shown in figure 16.

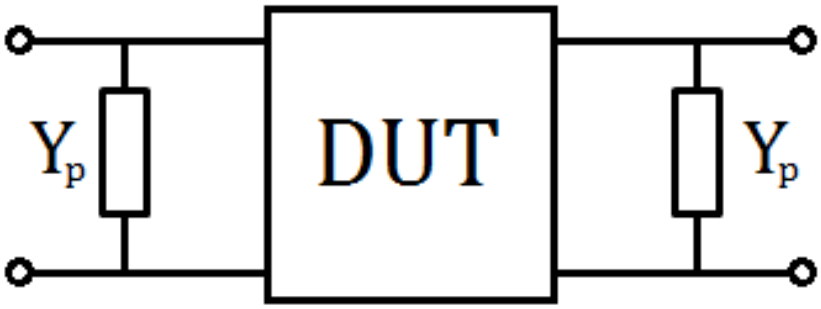

Figure 16 – Open pad de-embed topology

An open pad element can be described as the external elements from the device under test (figure 17 shows a generic Ground-Source-Ground open pad elements draft); this means that any element external to the analysis must be present (such as feed lines and the aforementioned pads). In order to acquire the parasitics admittance parameters, there are usually two options available: modeling or fabricating the open elements. In this work, an open element was manufactured, which enhances the importance of utilizing a single test fixture as it is more cost effective considering the size of the surrounding area occupied by passive elements (especially inductors). From there, the open element's scattering parameters were measured.

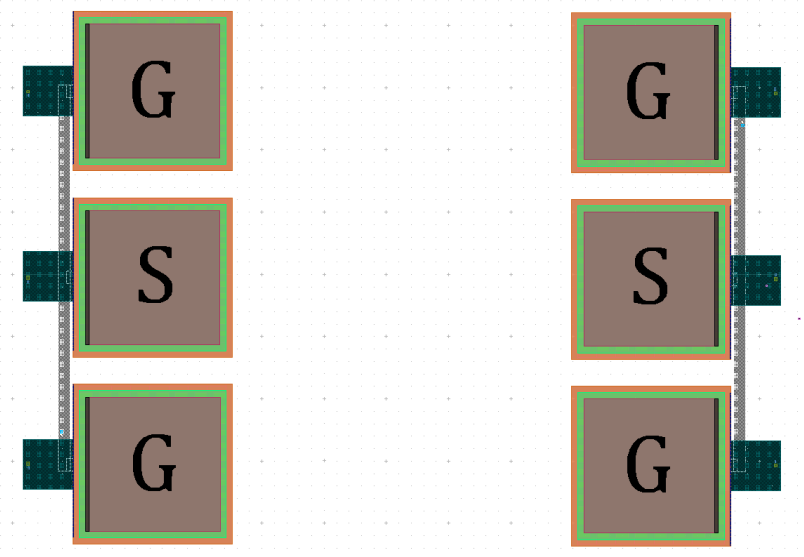

Figure 17 – GSG fixture

The admittance parameters were calculated through algebraic manipulations from the measured S-parameters. Finally, the DUT data can be calculated by

subtracting the open element measured data (Y_{Open}) from the raw circuit data (Y_{RAW}), as presented by:

$$Y_{DUT} = Y_{RAW} - Y_{Open} \quad (8).$$

This process is applied to all inductors analyzed in this work, which means that to produce coherent results, the devices surrounding structures are as important as the inductor's layout itself. Consequently, the circuit was designed in a manner that all of the analyzed inductors external components possessed a similar fashion, thus avoiding the necessity to fabricate multiple open pad fixtures.

Another possibility is to employ an *open-short* method (utilized in [15]) that considers the parasitics leading to the DUT are divided into a parallel and a series component, represented by an *open* and a *short* fixture. The open element is considered a shunt admittance Y_P, and the *short* is considered a series impedance Z_P. In this case, the *short* fixture connects the ground and the element's access. This technique's model distribution is presented in figure 18.

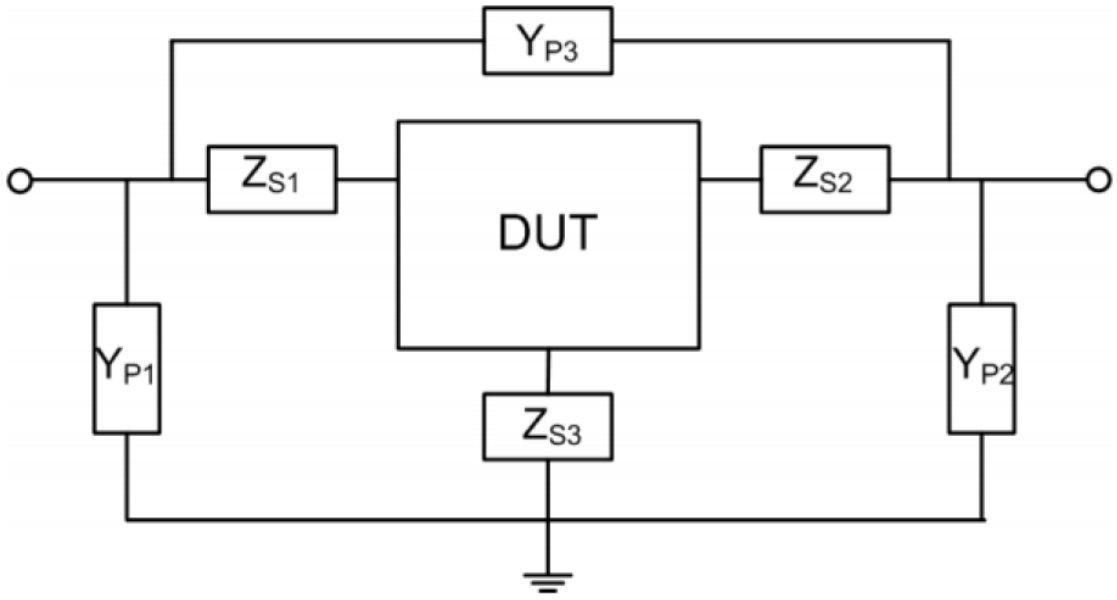

Figure 18 – Impedance model for the *open-short* de-embedding [15]

The open data is removed from the measurement in the same fashion as the *open* de-embedding, by subtracting the parallel impedance matrix. As the *short* data is considered a series component, its effect is removed by subtracting the *short*

element impedance matrix from the resulting subtraction obtained by the *open* step. The operations applied in this method are as follows.

$$Y_{DUT}^{(1)} = Y_{measured} - Y_{Open} \quad (9),$$

$$Y_{DUT}^{(1)} \rightarrow Z_{DUT}^{(1)} \quad (10),$$

$$Z_{DUT} = Z_{DUT}^{(1)} - Z_{Short} \quad (11).$$

Finally, a more complex five-step de-embedding technique is described in [37]. The used impedance model is shown in figure 19. Each step possess a test fixture that needs to be manufactured and emulates a different unwanted effect to be removed from the measured data.

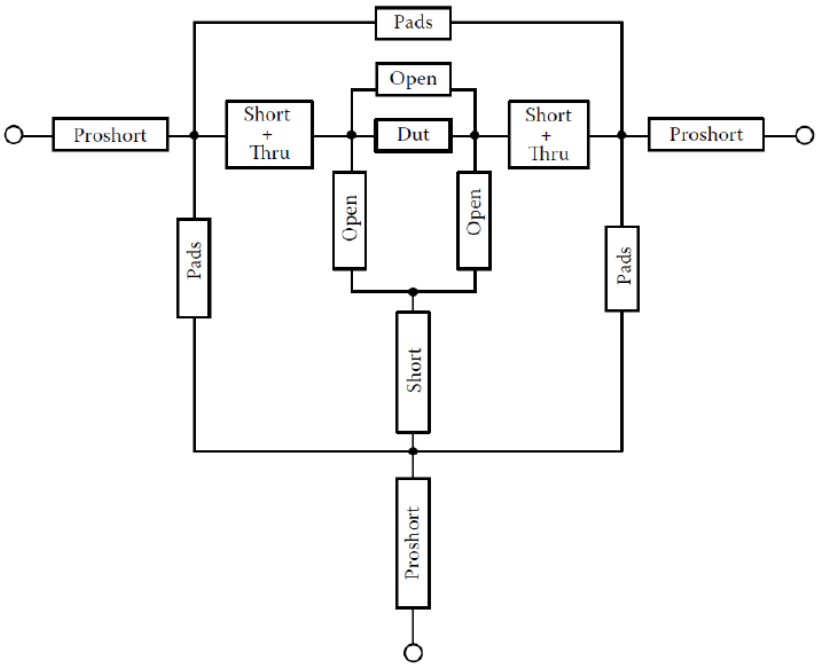

Figure 19 - Impedance model of the five-step de-embedding technique

This method is utilized in circuits designed to operate in very high frequencies [37], where any unaccounted element can significantly affect the complete circuit operation. Because of this, the presented method is a fairly complete de-embedding technique; typically, a smaller number of steps are utilized in de-embedding. Each de-embedding step requires its own test fixture, the associated fixture are presented in figure 20.

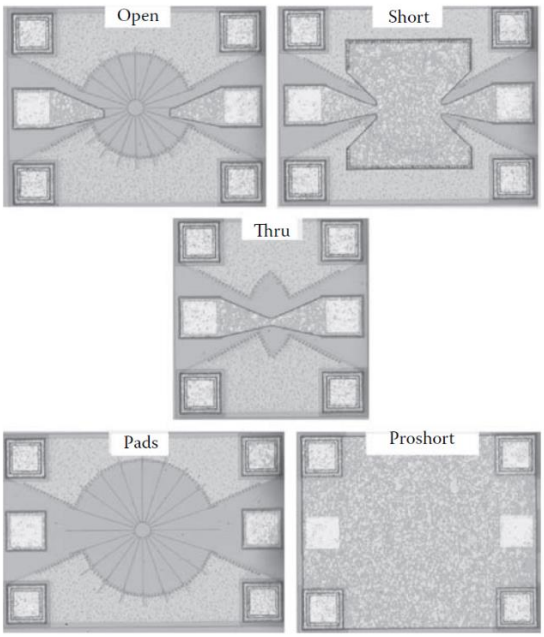

Figure 20 – On-wafer test fixtures required [37]

The *proshort, short* and *thru* effects are considered as series impedances between the entrance of the circuit and the device under test (DUT). Their effects are eliminated by subtracting the impedance matrix Z, obtained from the measurement of these fixtures, from the Z matrix of the DUT measurement. Analogously, *pads* and *open* fixtures are represented as parallel admittances and, therefore, are removed through the subtraction of their admittance matrix Y.

This elimination process must be performed in the order in which the fixture appear in the impedance model represented above. In this technique's case, the order is: *proshort, pads, thru, short* and *open*. This sequence is described by the following equations:

$$Z_{DUT}^{(1)} = Z_{meas} - Z_{Proshort} \quad (12),$$

$$Y_{DUT}^{(2)} = Y_{DUT}^{(1)} - Y_{Pads} \quad (13),$$

$$Z_{DUT}^{(3)} = Z_{DUT}^{(2)} - Z_{Thru} \quad (14),$$

$$Z_{DUT}^{(4)} = Z_{DUT}^{(3)} - Z_{Short} \quad (15),$$

$$Y_{DUT} = Y_{DUT}^{(4)} - Y_{Open} \quad (16).$$

Albeit being a more accurate method, the necessity of employing five different test fixtures can be a deterrent to the utilization of this method. Considering that inductors are large elements, this must be pondered when selection the de-embedding technique.

2.8. Electromagnetic Simulations

For the electromagnetic simulations, the utilized software was Keysight Advanced Design System (ADS). The software provides a range of tools to assist (and configure) the electromagnetic analysis, such as a 3D model representation that includes electric and magnetic properties of the different material employed (such as metals, dielectrics and semiconductors).

As there is a significant amount of practical computational electromagnetic solutions, this section will only cover the methods provided by the software. These methods are known as MoM (method of moments), FEM (finite element method), and FDTD (finite difference time domain).

2.8.1. Method of Moments (MoM)

The method of moments is a discretization technique utilized to solve Maxwell's electromagnetic simulations for planar structures embedded in a multilayered dielectric substrate. The momentum solution process encapsulates the following steps: calculation of the substrate Green's functions, meshing of the planar signal layer patterns, loading and solving the MoM interaction matrix equation, calculation and de-embedding of the scattering parameters and, finally, the reduced order modeling by adaptive frequency sampling [38].

Two modes can be utilized, a full-wave mode that uses full-wave Green functions, which are frequency dependent and fully characterizes the substrate without simplifying the Maxwell equations. The second mode is called quasi-static mode and utilizes frequency independent Green functions that results in L and C elements that are real and frequency independent. The approximation applied to the quasi-static mode implies that it should be used for structures that are smaller than half the wavelength analyzed [38]. This method is most efficient for planar and multilayer applications and complex structures.

2.8.2. Finite Element Method (FEM)

The Finite Element Method (FEM) divides the full space into smaller tetrahedral regions (called elements) and represents the field in each element by a local function [39]. This tetrahedron can be seen in figure 21.

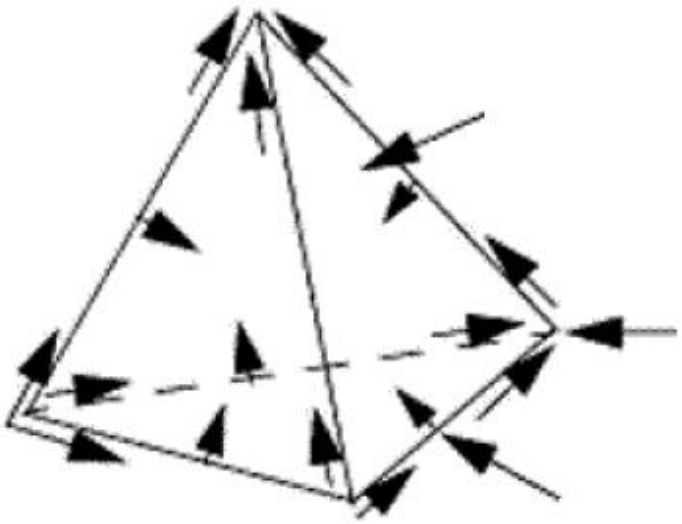

Figure 21 – Created tetrahedron [39]

The FEM simulator implements an adaptive mesh algorithm that generates an initial mesh and computes its electric fields (and S-parameters) for that mesh at a single selected frequency. This process generate an error estimative for all of the tetrahedra and refines the tetrahedron with the largest estimated error in order to create a new mesh on which the electric fields (and S-parameters) are computed one more time. The next step is a comparison between the S-parameters from consecutive meshes, if the difference (named delta) between the parameters is above a certain threshold (selected by the user) the simulator computes a new error estimative, with a new mesh and subsequent new electric fields (and S-parameters) until the delta is below the selected threshold. In that event, the simulation starts to compute the results for all the other frequencies [39].

2.8.3. Finite Difference Time Domain (FDTD)

The FDTD follows the volumetric sampling of the electric and magnetic field employed by the FEM. However, instead of using tetrahedral cells, the FDTD meshes are built from rectangular and curved conformal cells. The field values are updated through time (instead of frequency as the FEM) [40].

This results in a wide band frequency range analysis. Its utilization is recommended for electrically large problems and provides a broadband solution, however, each port present in the analysis requires an extra simulation [40].

3.INDUCTOR DESIGN AND SIMULATION

The utilized software to design the manufactured devices was Cadence Virtuoso. This chapter explores the steps applied to develop the design, detailing the technology utilized, enumerating the available topologies, presenting the concept of coupling shields, specifying the inductor constructive parameters, presenting the layout sent to fabrication and the electromagnetic simulation configuration process. Due to a non-disclosure agreement, the physical characteristics of the technology are omitted.

3.1. TECHNOLOGY COMPREHENSION

The Global Foundries CMOS8RF (CMRF8SF) technology is a 0.13 μm CMOS process intended for RF, analog and mixed-signal applications. The utilized technology configuration possesses five different BEOL wiring options. The 3-2 option was adopted, which means that there were three thin metal layers (M1, M2, M3), two intermediate metal layers (MQ and MG) and three thick RF layers (LY, E1, MA). Figure 22 shows a diagram representing the layers' stack of the adopted option.

Bellow the metal (and polysilicon) layers a p^- substrate is allocated. It is in the substrate that the BFMOAT layer is formed. This layer is a special case, as it does not represent a physical stacked layer, but a differentiation in the substrate doping at the drawn area. This doping increases the resistance of the selected portion of the substrate and is used to diminish the substrate coupling, reducing the substrate losses.

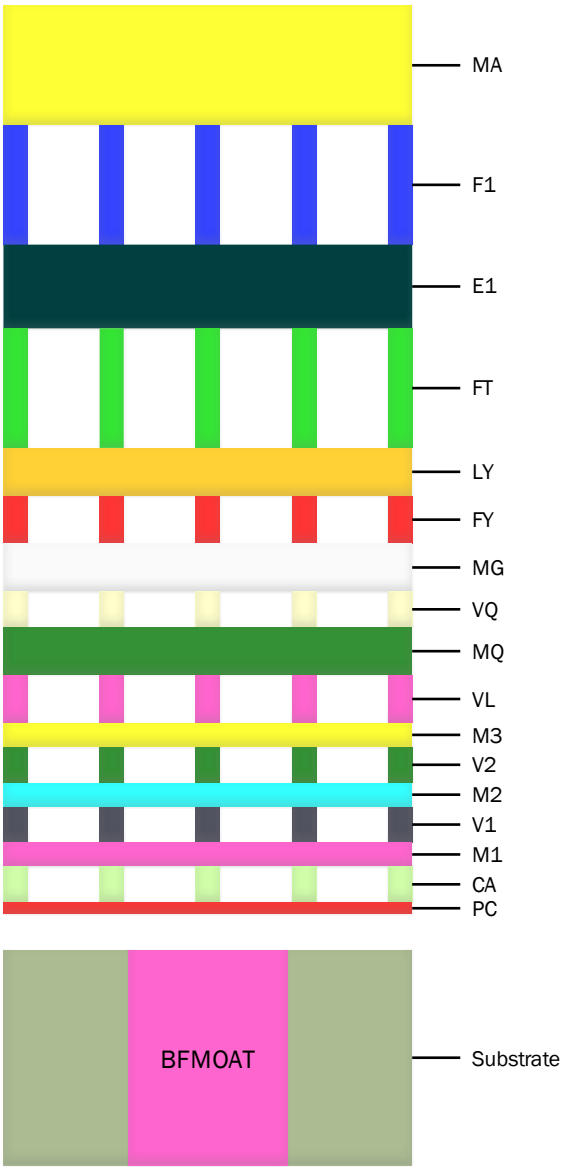

Figure 22 – Representation of the BEOL for the CMOS8RF (MA, 3-2) process (dimensions not to scale).

3.2. Inductor Topologies

The technology library presents a variety of inductor topologies. Such topologies are named IND, INDP, INDS, SYMIND, and SYMINDP.

The IND topology is a single-layer standard spiral, with the second port connected through an underpass connection; the standard spiral is asymmetric due to the varying length of each turn and the underpass connection. Figure 23 shows this topology's superior view.

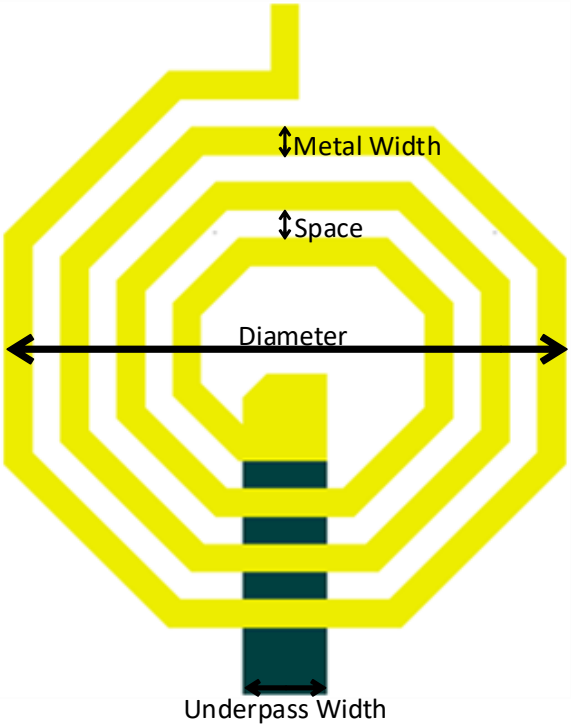

Figure 23 – IND type (IND, INDP and INDS) inductor top view

In order to utilize this cell, the following parameters must be set by the designer: metal width, space, diameter (outer dimension) and underpass width, which are highlighted in figure 23. The remaining parameters are the number of turns and type of ground plane (BFMOAT or M1). The inductor is placed at the top of the technology stack, in layers MA (for the coil) and E1 (for the underground pass).

The INDP category is a double-layered (MA and E1) spiral in which via bars connects both layers in parallel. This topology presents the same underpass connection as its single-layered counterpart, located at E1. That causes the lower layer to be interrupted at the underpass region, to avoid shorts. These inductors provide a lower series resistance than IND, because of the parallel connection, a lower self-resonant frequency due to the higher capacitance between the element lower metal (that is closer to the substrate than IND's lower metal) and the substrate.

Figure 24 shows a 3D view of this topology. The bar vias can be seen, (represented in blue) as well as the E1 layer below. This inductor's parameters are the same as the utilized in the IND topology.

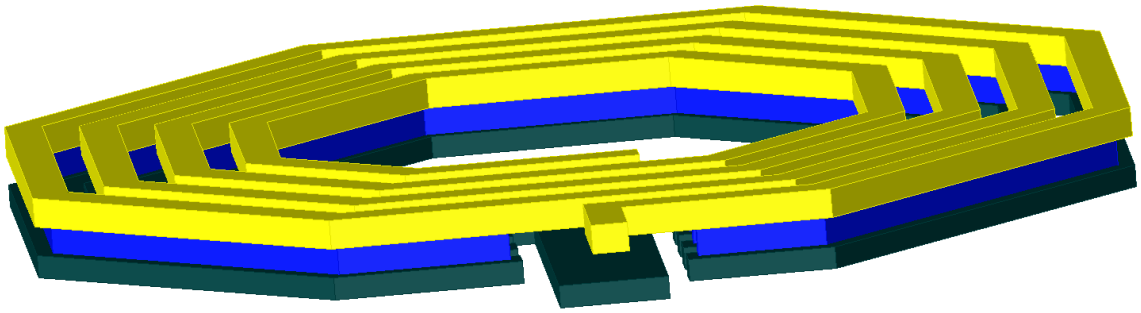

Figure 24 – 3D view of INDP's topology

INDS is also a double-layered spiral, but its spirals are connected in series (as seen in figure 25), which causes an increase in the magnetic field flow. The ports are positioned in different layers, as the inductors start at the topmost layer and ends at the lower layer. It presents a higher inductance density (inductance per unit of area) when compared to its standard spiral counterparts. This inductance increasing comes at the cost of the self-resonant frequency, caused by the enhanced coupling from turn to turn in the spiral, and the increased capacitance between the lower layer and the substrate that comes from the lower spiral placement in this topology into E1 (as opposed to the MA spiral in the single-layered topology). Once again, this topology is located at the top layers of the technology, utilizing MA for its first spiral, connected in series by the vias F1 to the second spiral E1. This topology's parameters are the same as before, however, the underpass width is excluded (as the second terminal is located at the lower spiral).

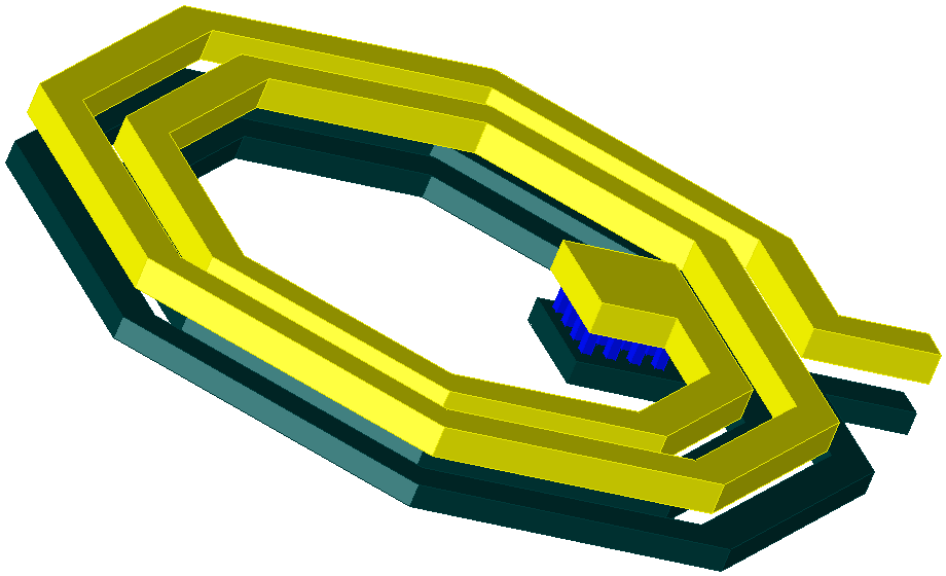

Figure 25 – INDS topology 3D-view

Finally, SYMINDP is a dual-layered octagonal symmetric spiral with both layers interconnected in parallel through bar vias (as in INDP, it utilizes the layers MA, F1 and E1), these elements ports are located at the outermost turn and there are crossovers at every half turn to prevent shorts. It is possible to insert a tap connection in order to allow access to the symmetric point of the spiral. This topology presents an enhanced performance in differential mode due to its balanced configuration.

The topology applied to the elements analyzed in this work is the SYMINDP topology. These symmetrical inductor *pcells* provides a number of design alternatives, like outer diameter, inductor coil width, number of turns, separation between turns, a center tap option and a ground shield option. Figure 26 presents a 3D view of the selected topology.

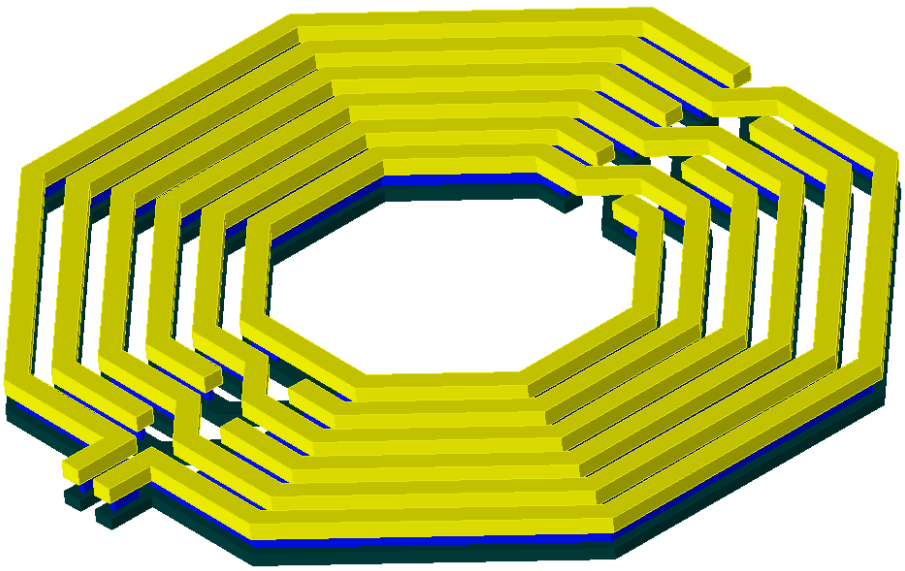

Figure 26 – SYMINDP 3D view

3.3. Ground Shield

As previously mentioned, one source for Q reduction is the coupling between the inductor and the substrate. The selected topology presented an option to insert a patterned shield at M1 (first metal layer) with a centerline used to connect the shield to the AC ground through the *subc* contact that is a device that executes a connection to the substrate. The patterned shield is presented in figure 27.

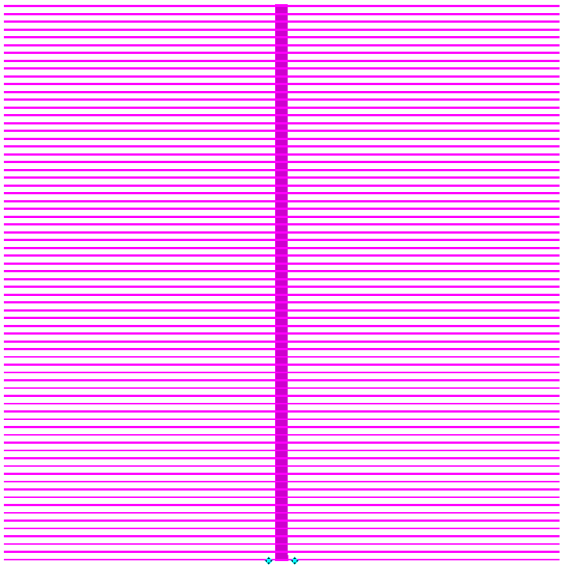

Figure 27 – Utilized ground shield's pattern

3.4. INDUCTOR SIZING

Figure 28 shows the selected topology's top view. The number of six turns is easily identified. An increase in this parameter will increment the magnetic flow through the coil, raising the cumulated inductance. The turns separations defines how close each turn is from one another, the closer the turns, more turns can be placed in the same area, considering that the width is maintained.

The feed length represents how long the inductor feed is. This attribute is not changeable at the *symindp pcell*; however, it is an important component of the inductor, especially in higher frequencies. Next is the coil width, which controls the width of the fabricated inductor; the width is directly responsible for the series resistance of the inductor, as increasing the width will definitely decrease its series resistance. Increasing this parameter may also inhibit the number of turns in the coil, dropping the cumulative inductance.

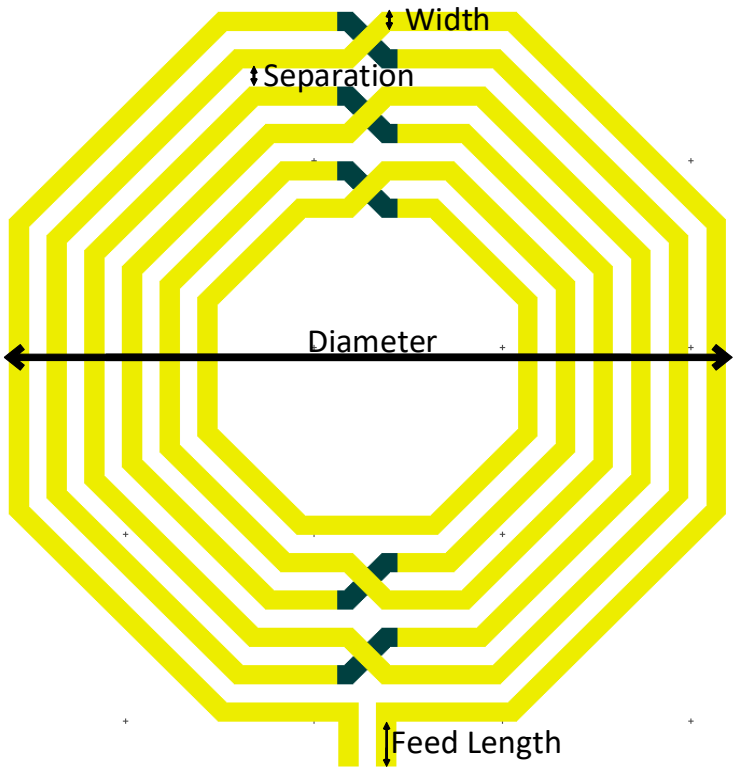

Figure 28 – Inductor's constructive attributes

The last parameter is the diameter of the coil. This parameter defines the overall area of the dispositive. All of the other parameters revolve around the diameter. A small inductor does not allow for a great number of turns, or a large coil width, but a large inductor may not be cost-effective. These contradictory relations makes the designing of inductors a difficult task to accomplish.

Three inductors were designed with the constructive attributes presented at table 1. As the structure to be manufactured mainly involved the designed inductors and their related pads, it was decided to design an element with size equivalent to these pads, which dictated the element's diameter. The pads possess a width of approximately 240 µm and a length of approximately 450 µm. As the inductor is connected to the center of the pad, it was decided to opt for a diameter of approximately half of the pads height, in order to take advantage of the large space required for the pad. However, density issues emerged in the design rules verification for diameters larger than 190 µm, limiting the inductor size.

In order to better utilize the provided space, another design choice was to increase the inductance of the inductor (therefore maximizing the number of turns) as errors in measurement of inductances tend to be more significant for small

dimensions. This increased number of turns serves to another analysis: the series resistance effect into the quality factor. The utilized trace width and turn separation were the default values for the design kit model.

Turns	Turn separation	Feed length	Trace width	Diameter
6	5 µm	12 µm	5 µm	190 µm

Table 1 – Inductors dimensions

3.5. LAYOUT

Four elements were designed and sent to be manufactured. The designed elements consisted in an open element (used for de-embedding) and three inductors. The first inductor, identified from now on as *Ind2xM1*, uses the *symindp* pcell. The inductor's top view is shown in figure 29, where the yellow lines represent MA layers and the greenish blue represents E1. It has a M1 layered shield (represented by the pink horizontal lines) and at the substrate level, a different doping is responsible for increasing the substrate resistance in that (purple) area, which indicates the presence of the BFMOAT layer.

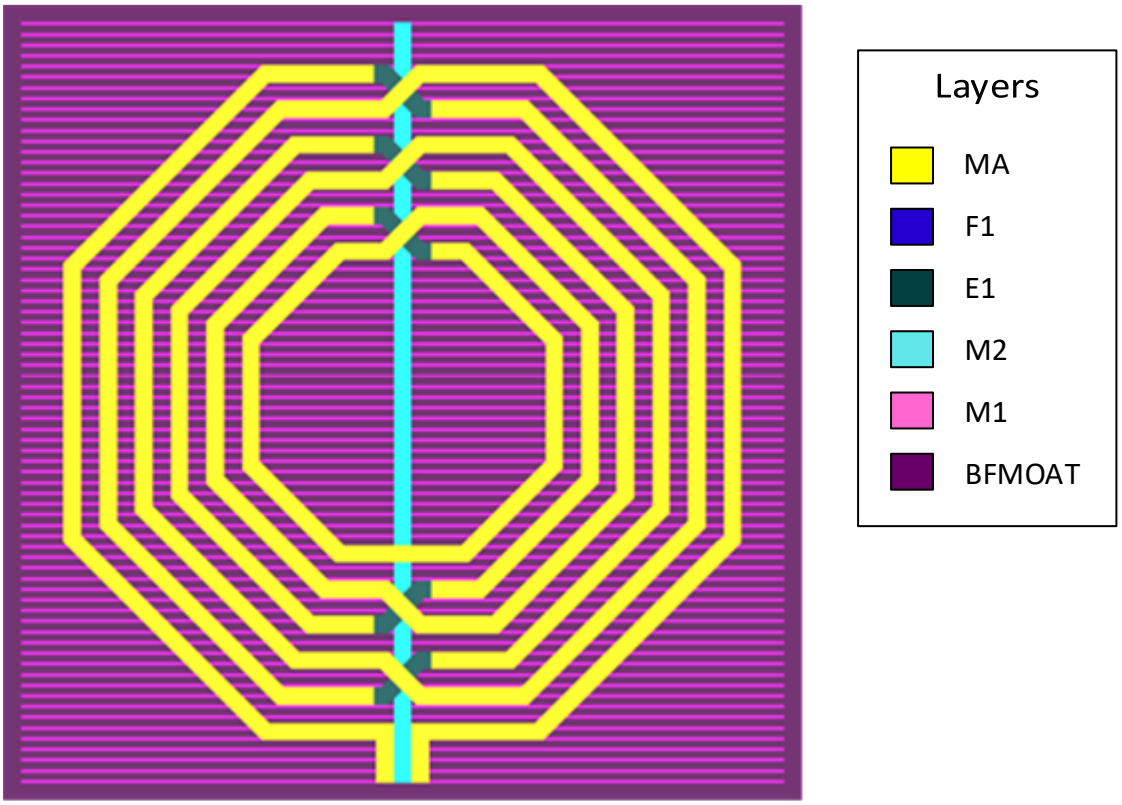

Figure 29 – Ind2xM1 top view.

In figure 30, a 3D top view is shown. It is possible to notice a dark blue (F1) element between the top layer MA and E1. That is the bar via that connects both layers in parallel and is responsible for reducing the intrinsic resistance of *symindp*.

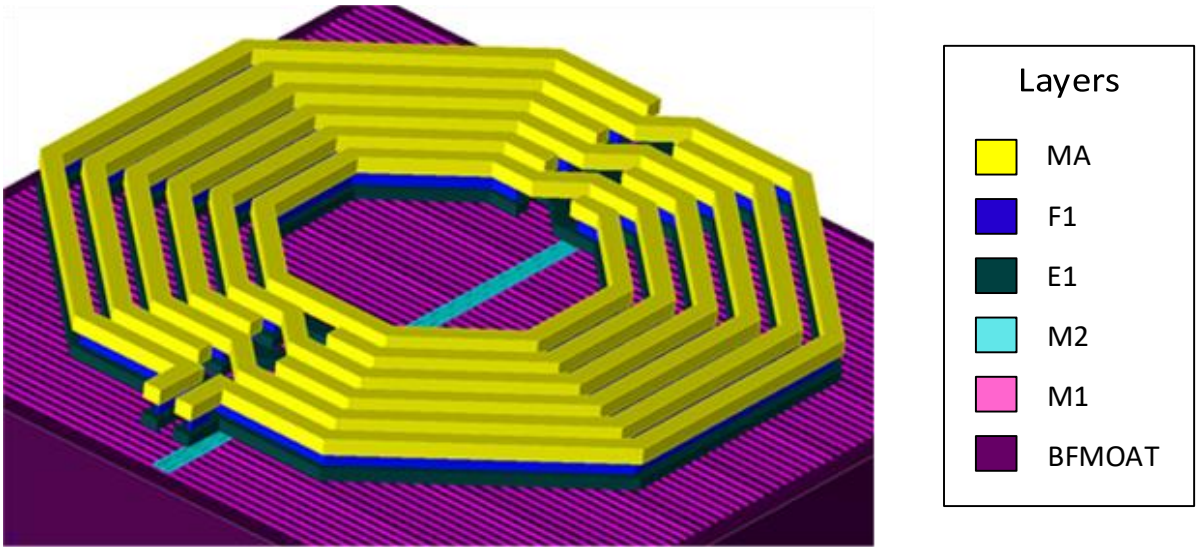

Figure 30 – Ind2xM1 3D view

The second fabricated inductor also uses the *symindp* pcell; it is denominated *Ind2xBFMOAT*, and, as mentioned before, has the exact same characteristics expressed at table 1. However, in this case, the shield is absent, making this inductor's ground plane the BFMOAT layer present below the structure. Its 3D view is shown in figure 31. Because the shield is absent, a lower Q than its predecessor and a higher self-resonant frequency are expected.

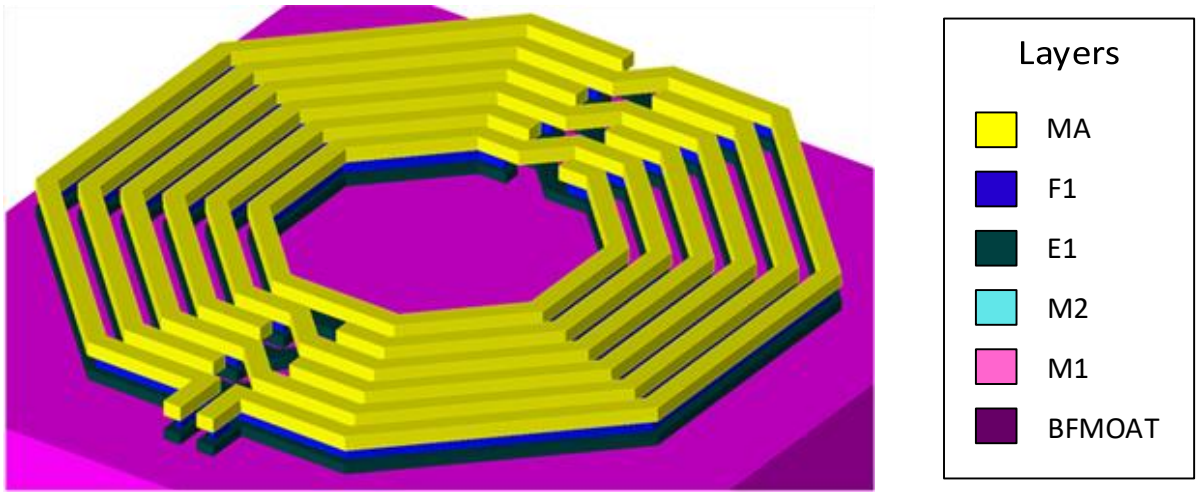

Figure 31 – Ind2xBFMOAT 3D view.

Opposed to the other two mentioned inductors, the last one (called *Ind1xM1*) was manually design and therefore, does not possess an electrical model attached. It was designed by removing the layer E1 from the winding in Ind2xM1 so that it only possesses the MA layer. The E1 layer is present solely at the crossovers. Figure 32 shows its 3D view.

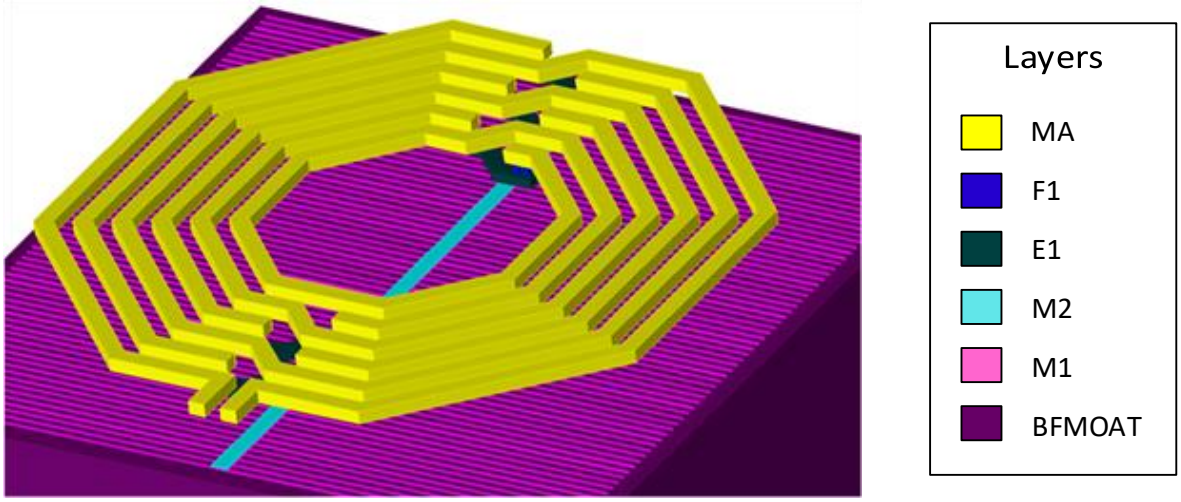

Figure 32 –Ind1xM1 3D view.

The last device is the open element. This element's main function is to reproduce the inductors external elements (such as the feed lines and pads). It is used to de-embed the connecting elements from the measurement data.

These elements were placed in pairs; the single-layered inductor was paired with the open element, and the double-layered inductors formed the second pair. The images in this section have some layers omitted (most of them are drawing and DRC layers), to provide a better understanding of the circuits presented.

Figure 33 shows the first designed pair, and embodies three main elements from the circuit. The first, marked in 1, is one of the GSG pads, with the ground pad located at its extremities and the signal pad at the center. It is important to mention that the ground pads are connected through the white layers (M1) and does not possess a connection to the signal pad. The elements marked as 2 and 3 are the single layered inductor and the open element respectively. Note that a ground plane element surrounds them, and their feed lines are positioned relatively at the same place. To achieve a good de-embedding, it is important that the environment surrounding the open element be the same as the designed inductors (as mentioned in the de-embedding section).

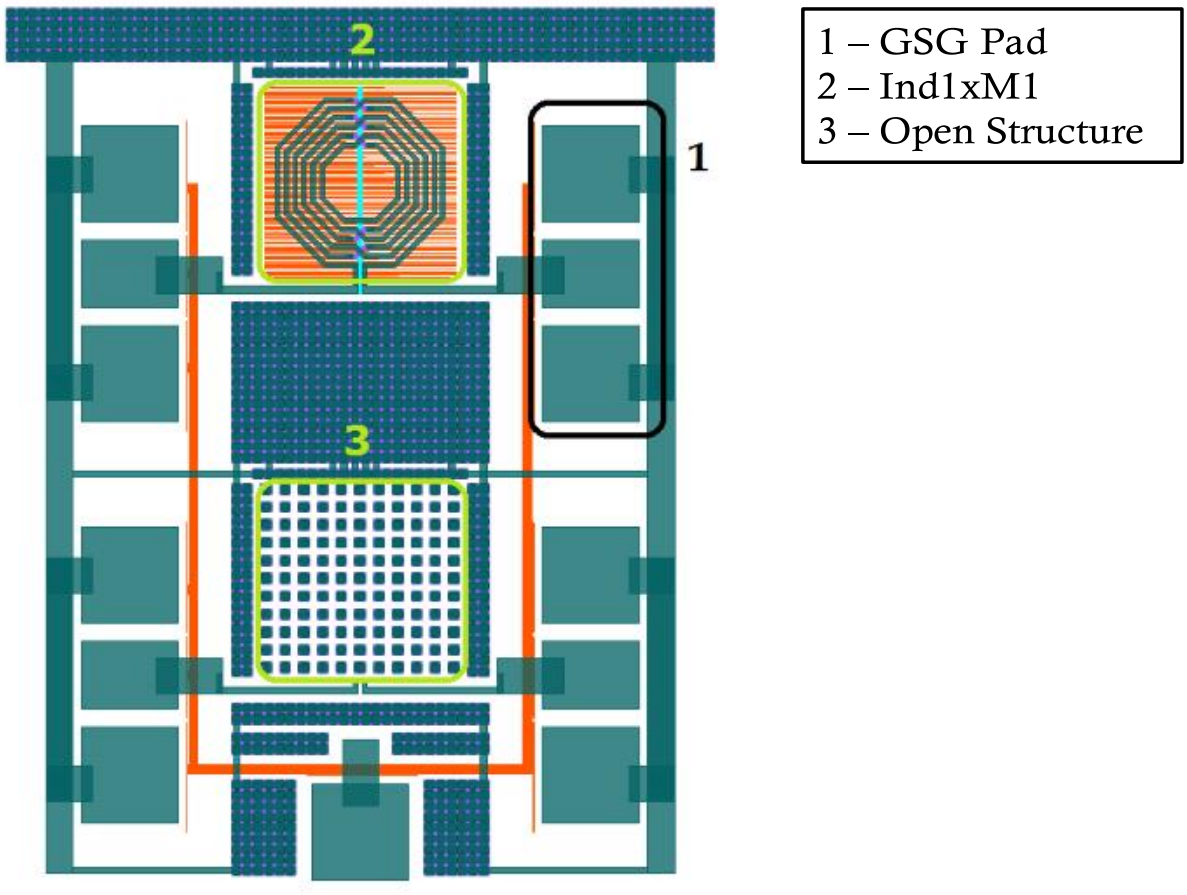

Figure 33 – Single-layered inductor and open element design layouts

The designed inductor has a centerline in M2 (represented by a light blue strip in figure 33) that is used to connect the M1 shield to the AC ground through a *subc* connection, as suggested by the technology manual. Ideally, the open element should be a completely open space. However, due to DRC density limitations, the presented configuration was designed. As its main purpose is to emulate the inductors surrounding environment, this element is not connected to anything.

Figure 34 shows the double-layered inductors designed. Highlighted in 1 is the double layered M1 shielded inductor; as its single-layered counterpart, there is a connection to the AC ground through the light blue centerline. The inductor highlighted in 2 is the inductor without the shield, this element is connected to the AC ground through a *subc* contact in the area corresponding to the BFMOAT layer. As before, both are connected to two pads each, that are connected to their terminals, the pads also presents the GSG configuration, with the signal terminal at the center.

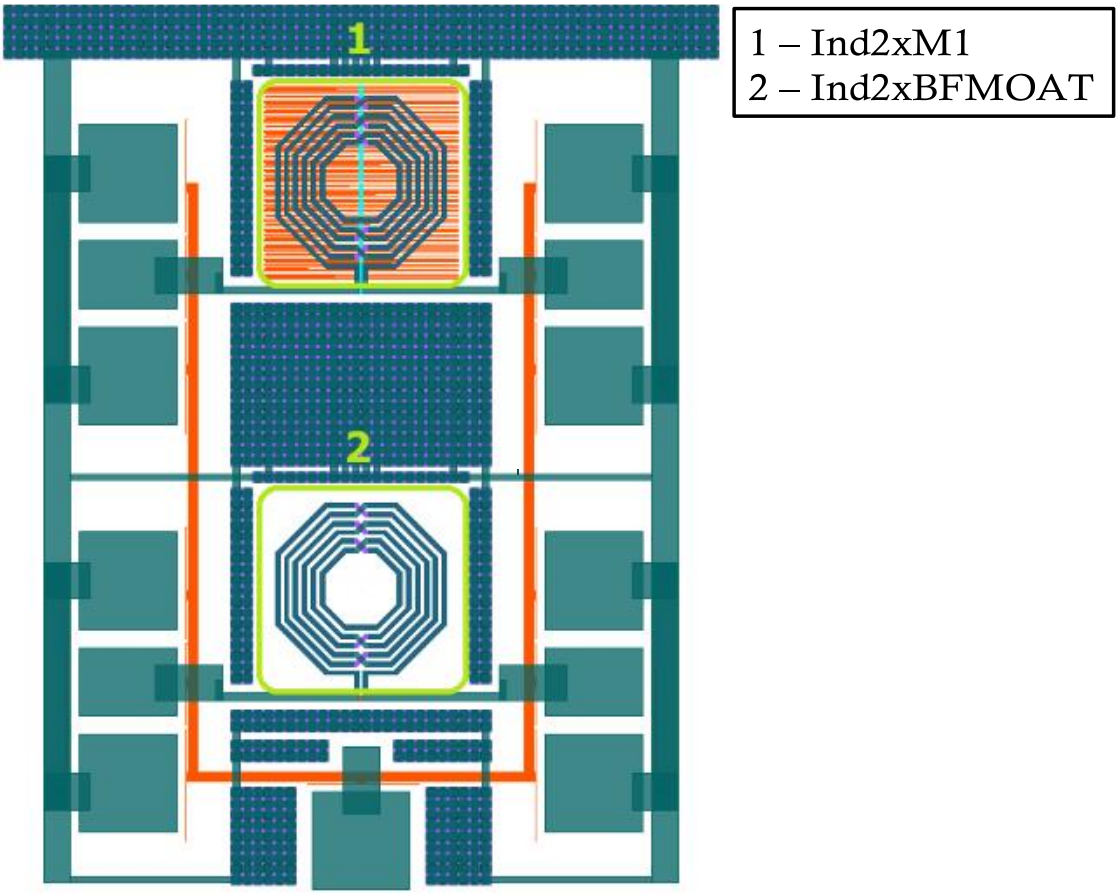

Figure 34 – Double-layered inductors layout design

A detailed part from figure 34 is shown in figure 35. This image also shows the BFMOAT substrate doping in pink; it has an area of 214 x 214 µm, approximately the same size as the open element. The vertical (in this figure) distance between the BFMOAT and the reference plane is 10.18 µm; the horizontal distance is 13 µm (to both sides). The feed line vertical segment, counting from outside the BFMOAT region, has a length of 8.14 µm and the horizontal's length is 150.88 µm.

The orange element between the feed lines corresponds to the *subc* connection to the substrate mentioned before. It is not connected in any way to the feed lines, as it is located at a lower layer. The distance between the BFMOAT region and the signal pad is 46.46 µm to both sides. In order to allow all inductors to be under the same circumstances, the three designed inductors are positioned in the same fashion, which means that these dimensions are the same in all of the layouts.

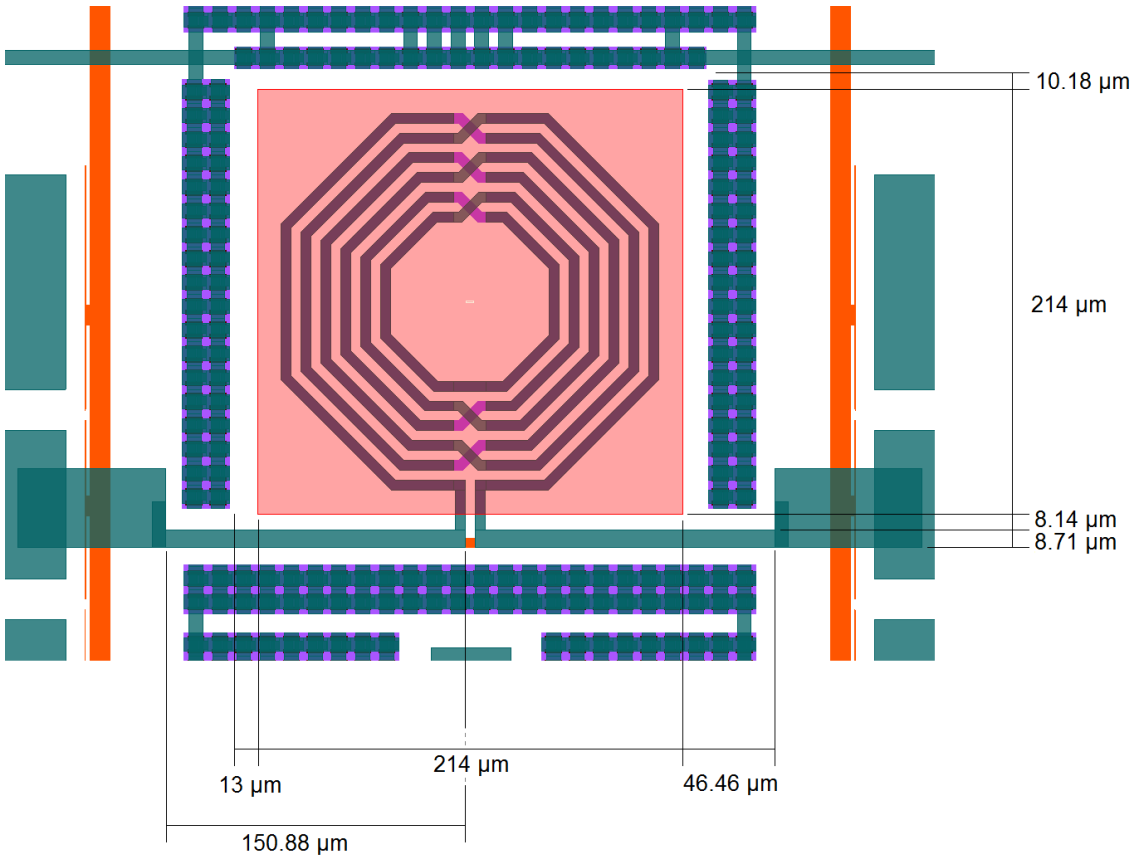

Figure 35 – Ind2xBFMOAT Detailed cut

Due to the technology density rules, the ground plane elements utilized are not solid structures; they are formed by inserting several small blocks side by side. Table 2, shows the number of blocks present in each of the highlighted structures in figure 35.

Structure	Horizontal Blocks	Vertical Blocks
1	1	20
2	18	2
3	2	24

Table 2 – Ground plane building blocks

These blocks are formed by different designs in each layer (as shown in figure 36) and each block occupies an area of 12x12 µm².

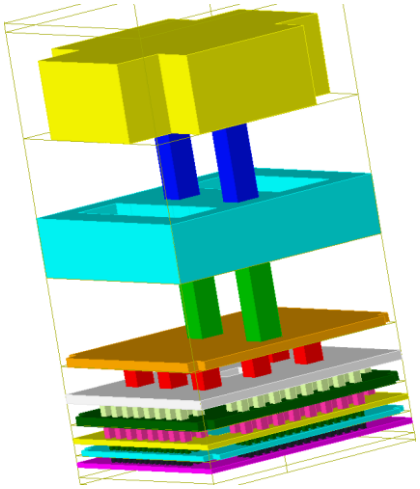

Figure 36 – Ground plane building blocks layers stack

3.6. Circuit Manufacturing

The presented layouts were allocated in a larger chip with other circuits included. They were positioned side by side, in order to provide both circuits with similar placement characteristics and were sent to be manufactured. Figure 37 presents the *Ind2xM1* and *Ind2xBFMOAT* pair's micrograph.

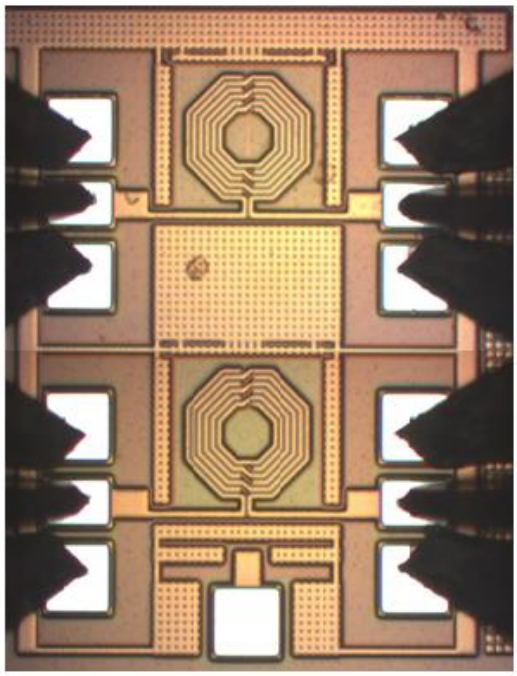

Figure 37 – Ind2xM1 and Ind2xBFMOAT micrograph

The single-layered inductor Ind1xM1 and the open element compose the other manufactured pair that is shown in figure 38.

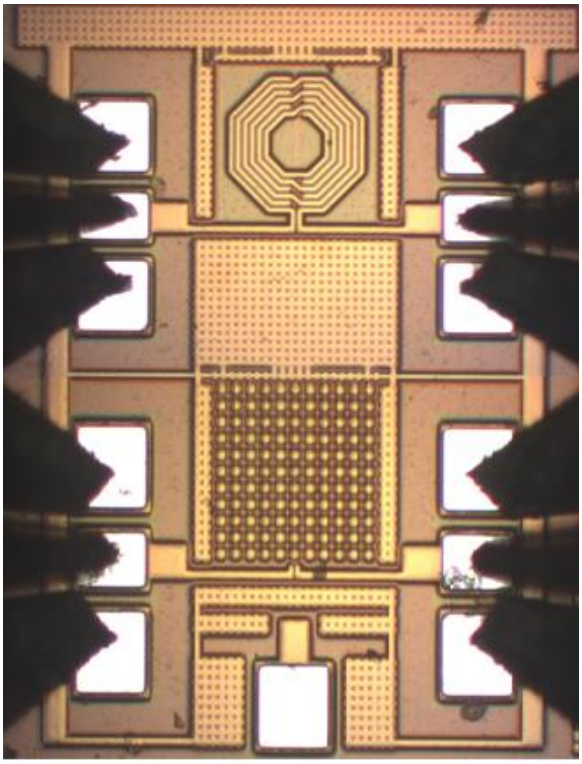

Figure 38 – Ind1xM1 and open element micrographs.

3.7. Electromagnetic Simulation

3.7.1. Adaptation of the Simulation Environment

Before starting the simulation, it is necessary to set the environment in which it will take place. This means that the configuration layers material, describing metals, dielectrics and substrate, must be in accordance with the utilized technology. In order to access this information, one needs to inspect the technology's manual (provided along with the design kit). For this work, a *substrate description file* (also provided with the design kit) accurately described the BEOL, as well as the last metal options materials and oxides. This description file provided a more accurate data than the technology manual, where the resistivity values were roughly rounded.

Figure 39, shows the layer configuration platform. It is possible to notice that each physical layer is placed in a different oxide; below PC, a semiconductor layer represents the silicon substrate. Note that the PC layer (that represents polysilicon) and the contact CA (which corresponds to the contact that connects the polysilicon and the lower metal layer M1) were not present at the *substrate description file*, and were manually added. Its characteristics were extracted from the technology manual and inserted into a newly created CA (and PC) material.

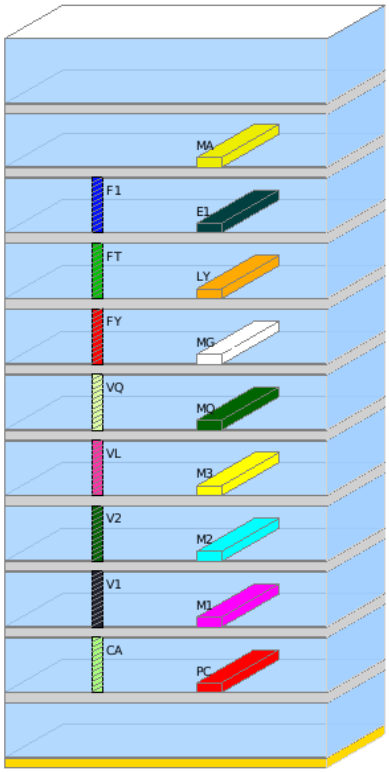

Figure 39 – Simulation's physical environment

This was not the only adaptation required, though. As shown in figure 39, the *substrate description file* specified only the last metal options of the environment. However, the designed inductors possessed a BFMOAT layer below that is responsible for a different doping at the substrate in that area.

To introduce this layer in the environment, a BFMOAT layer was inserted, with its corresponding resistance value. As the substrate is the lowest object in the environment, creating a layer with the exact height of the substrate leads to a number of simulation errors. To alleviate this issue, the created BFMOAT layer possessed almost the same height as the substrate.

A comparison between a simulation with the insertion of the BFMOAT layer and without the layer showed a significant improvement in the simulation's accuracy. For this reason, the layer was maintained with the aforementioned configuration.

On top of the MA layer, two dielectric layers are present. These layers determine the top of the layer stack. As the *substrate description file* determines that the uppermost layer (above the aforementioned dielectrics) is defined as an open boundary, this layer is constructed as a layer with a vertical extension thickness configured by the user and an open boundary condition to truncate the problem

domain. In the simulation configuration, a vertical extension of 100 µm is selected. A horizontal extension is applied as well (in this case, 10 µm was selected). In both these boundary limits, an absorbing wall boundary is implanted, which is applied to approximate an infinite extension. The boundary limits are shown in figure 40. These limits are depicted in relation to the layers MA (upper limit) and BFMOAT (lower limit). It is possible to notice the relatively large extra vertical space above the MA layer. The boundary box is represented by the dark blue box surrounding the element.

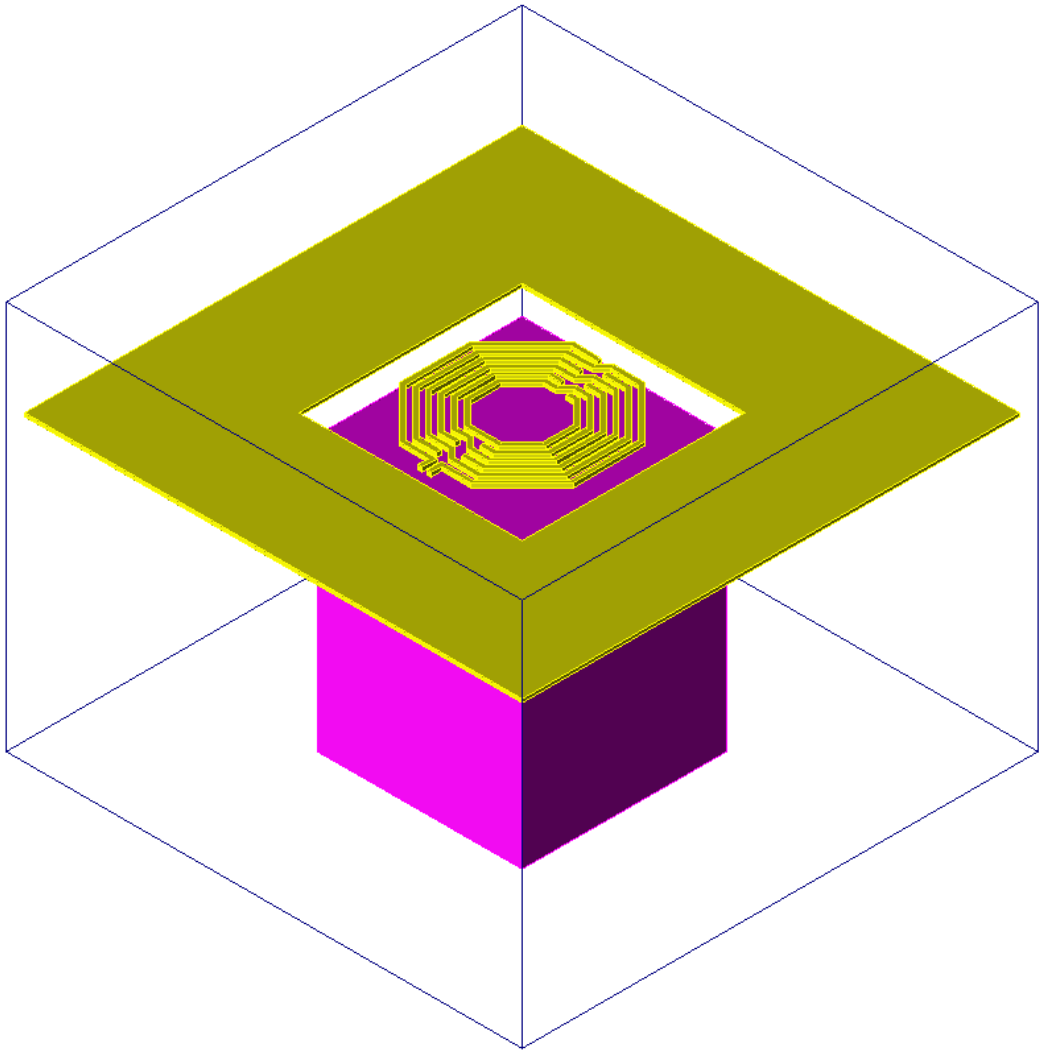

Figure 40 – Boundary box

3.7.2. Layers Attribution

The layer management in ADS separates the layers configuration in two different types: the physical and the drawing layers. The physical layer comprises its

physical characteristics (such as the metal's material, height, etc.) and its position at the layer stack (as previously presented in figure 40).

The drawing layer represents the layers used to draw the desired layout and is defined by its attached physical layer, drawing color and name. After configuring the physical layers (process described in the previous section), in order to transform the designed layout into a full 3D model, it is necessary to attribute a drawing layer to their respective physical layers. As the number of layers present in the technology is not large, this process was done manually.

The CMOS8RF technology interface includes several types of layers (such as drawing, label, DRC, etc). Since not all layers represent a physical component at the layout, these layers were not included into the environment configuration, as their presence would only add extra drawing layers without a defined purpose.

3.7.3. Layout Import

The export (from cadence) and import (to ADS) process realized in this work was executed through the GDSII stream format. This database file format contains information about the layout of a circuit, including levels, geometric shapes and text labels. However, as a CAD stream format, the physical properties of the layers are not included in the file. In the ADS interface, these are considered the drawing layers and, this means that without the previous steps, the imported layout would end up as a 3D description model without physical meaning, containing only the layout geometry.

During this process, a *map file* that associated the GDSII code to the layers name was created. This process is only required once, as the *map file* is saved and can be browsed for subsequent import process.

3.7.4. Layout Adaptation

Instead of simulating the complete manufactured layout, the inductors were analyzed separately in order to simplify the simulations and analyze the inductors response independently. Therefore, for all elements of interest (inductors) the external elements, such as the circuit feed lines and pads, were removed from the simulation.

The ground plane was also adapted. As mentioned before, the ground plane inserted at the layout was not a solid structure by virtue of technology density rules. This structure is relevant to the electromagnetic simulation as well, being an important

part of the simulation [13]. However, this kind of sectioned element imposes a high strain at the mesh creating process, largely increasing the simulation time. For this reason, the ground plane utilized in the simulation phase was a solid structure composed of all metal layers and corresponding vias, from MA through PC.

Figure 41 represents the adapted BFMOAT inductor simulation layout with the ground plane included. The ground plane's width is 150 µm, and has a 10 µm separation from the BFMOAT area. This results in a 544.08 µm x 544.08 µm total area. This adaptation is applied to all of the analyzed inductors.

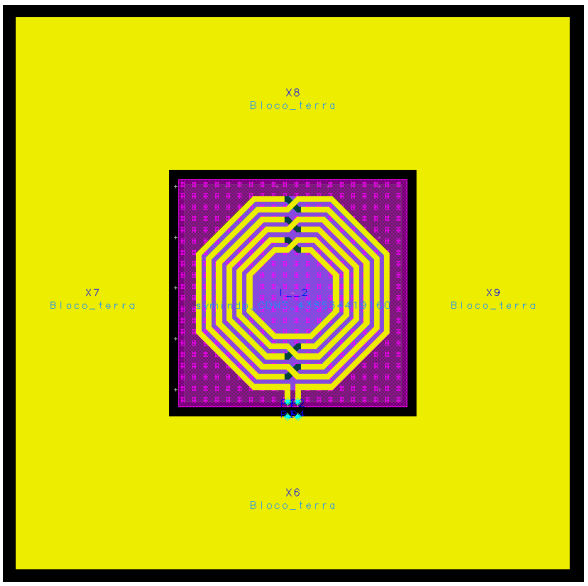

Figure 41 – BFMOAT inductor enveloped by ground plane

3.7.5. Simulations Configurations Settings

As previously discussed, inductors can be analyzed as single or double port network elements. In order to choose the best-suited simulation method, table 3 was compiled. The data presented in the table 3 was extracted from [41].

FEM	FDTD	MoM
3D Arbitrary Structures	3D Arbitrary Structures	3D Planar Structures
Full Wave EM Simulation	Full Wave EM Simulation	Full Wave and Quasi-Static Simulations
Frequency Domain	Time Domain	Frequency Domain
Multiport simulation at no additional cost	EM simulations per each port	Multiport simulation at no additional cost
High Q	GPU based hardware acceleration	High Q

Table 3 – Simulation method comparison [41]

As FDTD is a time-domain method and requires a different simulation for each port, its utilization was discarded. This method would become very taxing in future works when analyzing 4-port devices such as transformers.

With FDTD discarded, the simulation method selection was between FEM and MoM. FEM was chosen for being a full 3D arbitrary frequency-based simulation method (as opposed to MoM's 3D planar method), which ensures a larger gamma of geometric possibilities. This freedom is desired, as this setting will be used for a different number of future works. The initial target mesh size can be configured as well; however (as the software suggests) this setting was left on automatic.

For this work, the 2-port network option utilized. Differential ports were utilized to apply the two-port network concept to this simulation environment. The ADS software allows the establishment of those ports by creating a two-pin port, where each pin acts as a terminal (a positive and a negative). This structure results in the arrangement presented in figure 42. Where the positive (+) pin of port 1 is connected to the inductor's first terminal and the negative pin is connected to the ground plane positioned below. The same technique is applied to port 2, with the positive pin connected to the inductor's second terminal. This guarantees that the ground plane acts as the circuits reference as designed in the fabricated layout.

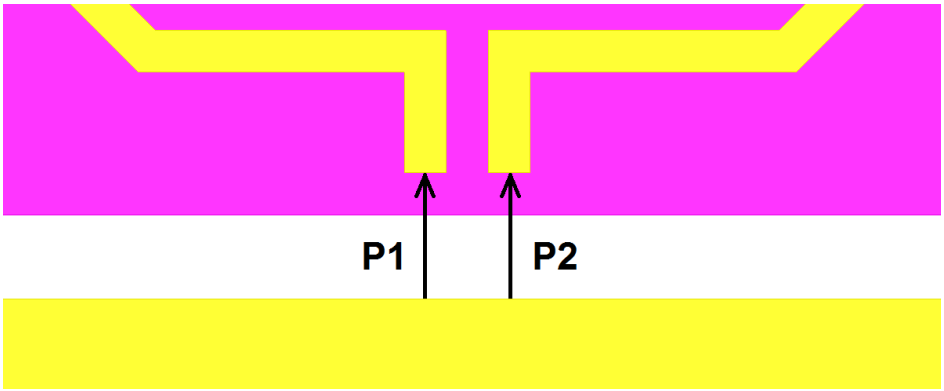

Figure 42 – Ports configuration

Another port configuration option provided by ADS is the type of calibration. This calibration is utilized to shift the location of the reference parameters. This shift is utilized to erase the effect of probes when measuring hardware prototypes [42]. According to [43], there are five calibration options: TML, TML (zero length), SMD, Delta Gap and None. TML and TML (zero length) calibration inserts a transmission feed line to the port, with the source being added at the end of the feed line to excite the structure [42]. Whereas selecting SMD or Delta Gap calibration connects a two pin SMD component that adds two feed lines to the layout pins of the port, a source is added over the delta gap connecting the feed lines, the SMD configuration removes the parasitic effects of the feed lines while Delta Gap calibration does not [42].

As the pins of each port are positioned in different reference planes, the TML calibrations are not recommended. The same goes to SMD and Delta Gap, because no SMD component is utilized. Therefore, it was decided not to calibrate the ports.

Refinement frequencies of 5 GHz, 10 GHz, and 15 GHz were tested and sequentially compared to the measured data in order to determine the refinement frequency that displays the closer results. It is also possible to select more than one refinement frequency; however, as the number of refinement frequencies increases, the number of created meshes also increases, causing the time required to refine the mesh to be impractical (especially considering that most of the refinement occurs at the highest frequency tested, making the extra refinements a waste of time).

The simulation frequency range is in accordance with the measurement data (which used a frequency range from 1 to 10 GHz), and the utilized frequency sweep was adaptive. Logarithmic sweep was also an interesting option, but did not provide any substantial improvement to the results, and usually took more time to complete.

Finally, the last configuration was the metal model settings. Due to the skin effect, the increase in frequency operation causes the current in the conductor to flow at the conductor's surface. As it is the standard procedure in FEM simulations, an approximate surface impedance is used in the surface of the conductors. This configuration matches the loss modeling at high frequencies [44]; however, this work's target frequency range includes lower frequencies, to which the "Meshed Interior" option presents a more accurate solution. A comparison between the figures of merit obtained by the meshed interior and surface impedance configurations is presented in the Appendix A, where the poor low frequency loss modeling of the surface impedance configuration appears in the discrepancy of the elements quality factor.

3.7.6. Pre Simulations

This phase consisted in simulating the Ind2xM1 and Ind2xBFMOAT inductors and comparing its simulation results to the model provided by the technology's library. In this phase, the necessity of the aforementioned BFMOAT layer emerged. The ground plane's expansion from M1 through MA to PC through MA also started to be investigated.

The refinement frequency utilized so far was 10 GHz, as the simulator suggested "the highest frequency", and the ground plane size and distance from the inductors were adjusted in this step. All of these considerations were revisited at the measurement results analysis, detailed in the next chapter.

3.7.7. Electromagnetic Simulation Characteristics

With the measurement data available, the simulation setting were updated in order to approximate the simulated data to the measured results. The main difference in the simulator configuration was the refinement frequency that shifted from 10 GHz to 15 GHz that provided more precise results.

Table 4 presents the electromagnetic simulation characteristics for the simulated inductors, such as the quantity of tetrahedra and unknowns in the initial (and refined mesh), number of refining required to comply with the established 0.01 delta error.

	Ind2xM1	Ind2xBFMOAT	Ind1xM1
Initial Mesh Tetrahedron	320,216	107,191	278,470
Initial Mesh Unknowns	2,033,420	682,976	1,769,764
Final Mesh Tetrahedron	487,031	223,141	583,950
Final Mesh Unknowns	30,95,610	1,421,834	3,715,678
Refining Levels	4	6	6
Total Elapsed Time	8 hrs 07 min	2 hrs 50 min	6 hrs 20 min

Table 4 – Simulation characteristics

The absence of the detailed shield structure at Ind2xBFMOAT is the only difference between the numbers of tetrahedra generated from the Ind2xM1 simulation. This greatly reduces the total simulation time, even considering that less refinement steps were applied to the double-layered shielded inductor. The same can be said about the single-layered inductor, which presented a high number of tetrahedra, if compared to the shieldless inductor. The generated mesh at all the inductors is presented in the Appendix B.

4.MEASUREMENT AND RESULTS

This chapter overviews the analysis parameters, compares the manufactured inductors' data among each other and compares the measured and simulated data through a graphical analysis. Finally, an interpretation of the results is presented.

The measured data was obtained using the PNA Keysight E8361A network analyzer. Besides the network analyzer, a typical setup for doing on-wafer measurements for RF application consists on several equipment such as IC probe stations, probe link arms, GSG probes and semi-rigid cables [36]. Aside from these structures, there is the need of testing pads and feed lines connecting the device under test (DUT) to them.

The results obtained from the on-chip inductors represent the performance of the whole element situated between both accesses of the measurement platform. Besides the device of interest, others elements are present such as feed lines and pads. These elements include parasitics, impairing the data. To avoid these parasites, a correction method (de-embedding) is applied to the system [15]. In order to obtain the correct data from the inductors, the de-embedding process was applied.

4.1. ANALYSIS PARAMETERS

As seen in previous sections, admittance parameters are used to analyze an inductor's performance. The algebraic manipulations required in order to transform scattering parameters into admittance parameters are:

$$Y_{11} = \frac{(1-S_{11})(Z_{02}^{*}+S_{22}Z_{02})+S_{12}S_{21}Z_{02}}{(Z_{01}^{*}+S_{11}Z_{01})(Z_{02}^{*}+S_{22}Z_{02})-S_{12}S_{21}Z_{01}Z_{02}} \quad (17),$$

$$Y_{12} = \frac{-2S_{12}\sqrt{R_{01}R_{02}}}{(Z_{01}^{*}+S_{11}Z_{01})(Z_{02}^{*}+S_{22}Z_{02})-S_{12}S_{21}Z_{01}Z_{02}} \quad (18),$$

$$Y_{21} = \frac{-2S_{21}\sqrt{R_{01}R_{02}}}{(Z_{01}^{*}+S_{11}Z_{01})(Z_{02}^{*}+S_{22}Z_{02})-S_{12}S_{21}Z_{01}Z_{02}} \quad (19)$$

Where Z_{01} is the source impedance, $Z_{02}$is the load impedance, and R_{01} and R_{02} are the real part of Z_{01} and Z_{02}, respectively..

The admittance parameters can be assembled in a π fashion, as suggested in chapter 2. The component's symmetric characteristics and the presence of only

passive elements allow us to simplify the parameter's network, which cause both shunt branches to present very similar results. A parallel can be traced between the network π configuration and the analysis model; this correlation is presented in figure 43.

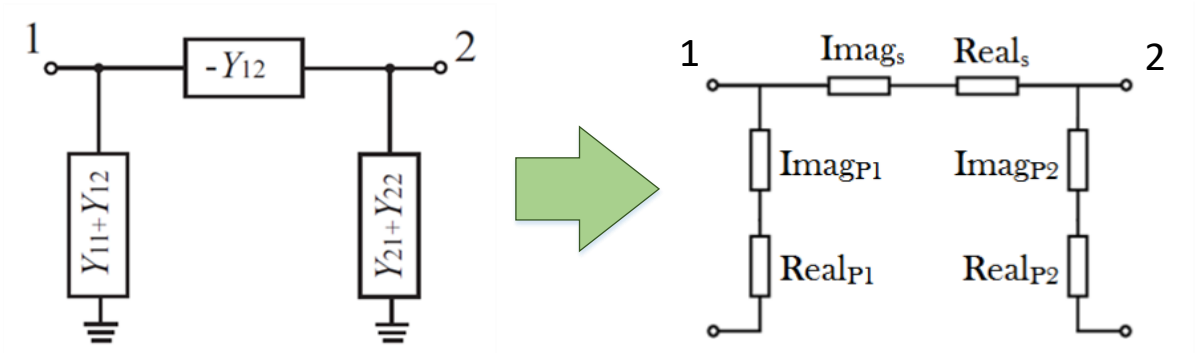

Figure 43 – Y-parameters π model updated

The model series branch presents a direct correlation to Y_{12}. With that, we can divide the inverse of the admittance parameter in its real and imaginary part and analyze it separately. The real part of the inverted series admittance will be called $Real_s$, as it symbolizes the real segment of the measurement's data impedance, as shown:

$$Real_s = real\left(-\frac{1}{Y_{12}}\right) \quad (20).$$

The imaginary part of the inverted series admittance will be considered as an inductive reactance (the element in consideration is an inductor, after all). The resulting analysis parameter in this case is $Imag_s$. For that matter, the reactance must be divided by the angular frequency (known as ω). This analysis parameters is described by:

$$Imag_s = \frac{imag\left(-1/Y_{12}\right)}{\omega} \quad (21).$$

The same process is applied to the parallel branch. Where instead of considering the series admittance, the shunt admittance is the target. Starting with the real part, $Real_p$ represents the real segment of each shunt branch. Defined by:

$$Real_p = real\left(\frac{1}{Y_{12} + Y_{11}}\right) \quad (22)$$

The imaginary shunt branch behaves as a capacitance. For this reason, it is analyzed as such and is calculated by inverting the opposite of the imaginary part of the branch reactance and multiplying it by the angular frequency. The branch reactance is bestowed by inverting the sum of Y_{12} and Y_{11}. This parameter is called $Imag_p$ and its formulae is :

$$Imag_p = -\frac{1}{imag\left(\frac{1}{Y_{12}+Y_{11}}\right)}.\frac{1}{\omega} \quad (23)$$

4.2. Inductors Comparison

This section will provide a comparative analysis of the manufactured inductors, which will start with the series and parallel branch parameters, in order to observe the consequences of the differences in the devices' design. Following this analysis, the figures of merit are delineated and the effect of those discrepancies in the analysis parameters are exposed.

4.2.1. Series Branch

In order to improve the series branch analysis, we extrapolate the previously presented model to the lumped configuration exhibited in figure 44. We can extract the lumped model's inductance (from the imaginary component) and resistance (from the real segment) by observing the parameters in low frequency, where the capacitive effect are less prominent.

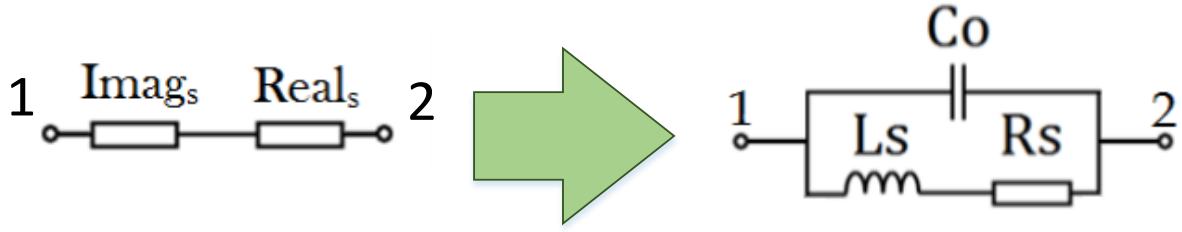

Figure 44 – Series branch model equivalent

The inductors' series imaginary component (also referred as series inductance) are shown in figure 45. It can be seen that in this case the double-layered inductors present a very similar response. Therefore, we can confirm that the ground

plane does not influence the series branch imaginary component significantly. Meanwhile, the single-layered inductor presents a higher inductance than the one obtained from the double-layered elements. This was expected as wires with smaller cross section areas present a larger inductance because they generate more magnetic flux external to the wire [11].

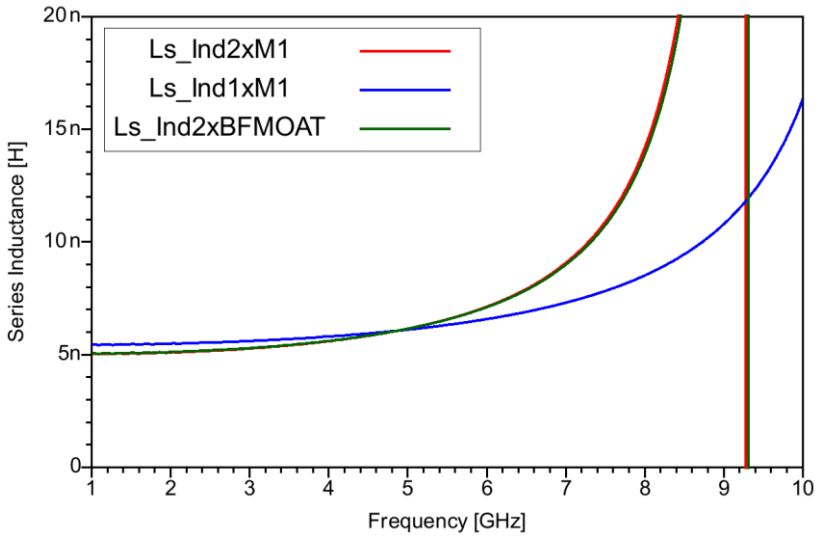

Figure 45 – Series imaginary component comparison

By considering the low frequency series imaginary component as the inductance and the resonant behavior present in the series branch behavior, C_o can be estimated by:

$$C_o = \frac{1}{\omega_0^2 . L_s} \quad (24),$$

where ω_0 is the resonant angular frequency.

Finally, the series real component (also referred as series resistance) is shown in figure 46. The low frequency results presented by this element correspond to the series resistance of the devices. Due to its smaller cross section area, the single-layered inductor presents a higher resistance. As expected, the double-layered elements present a similar low frequency response. It is possible to notice the impact that skin effect presents in these elements resistance, since, as frequency increases, the effective area in which current flows reduces, which causes the increment in the equivalent resistance.

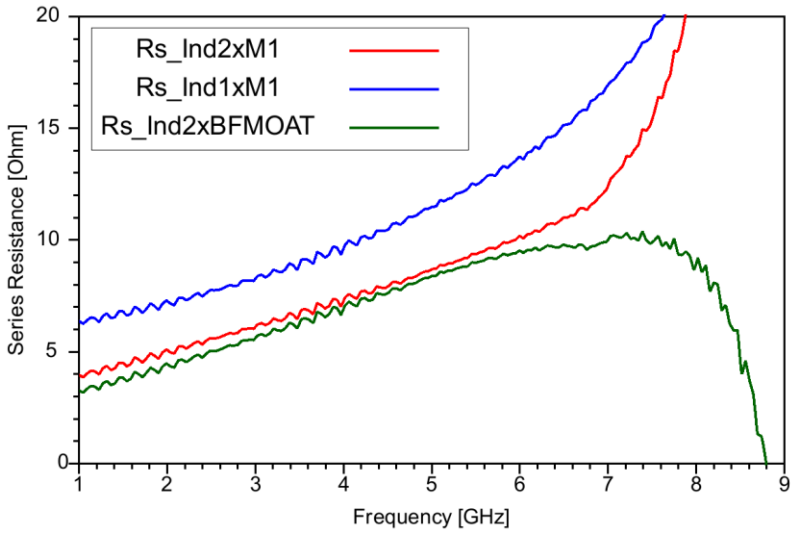

Figure 46 – Series real segment comparison

Table 5 shows the LF parameters values, series branch resonant frequency (and their relative differences to Ind2xM1 value) and estimated C_o. As, Ind1xM1 capacitance cannot be accurately estimated, we consider that its resonant frequency is higher than 10 GHz, consequently affirming that it is lower than 46.5 fF.

	Ind2xM1	**Ind2xBFMOAT**	**Ind1xM1**
LF Inductance	5.0 nH	5.1 nH	5.5 nH
Relative LF Inductance	0%	0.4%	8.2%
LF Resistance	3.9 Ω	3.3 Ω	6.4 Ω
Relative LF Resistance	0%	17.5%	61.3%
Resonant Frequency	9.3 GHz	9.3 GHz	>10 GHz
Estimated Capacitance	59 fF	58.0 fF	<46.5 fF-

Table 5 – Series branch parameters

4.2.1. Parallel Branch

For the parallel capacitance, the analysis model is highlighted in figure 47. This models presents two important parameters: C_{ox} and C_{sub}, where C_{ox} represents the metal-oxide capacitance and C_{sub} illustrates the substrate capacitance, as previously mentioned.

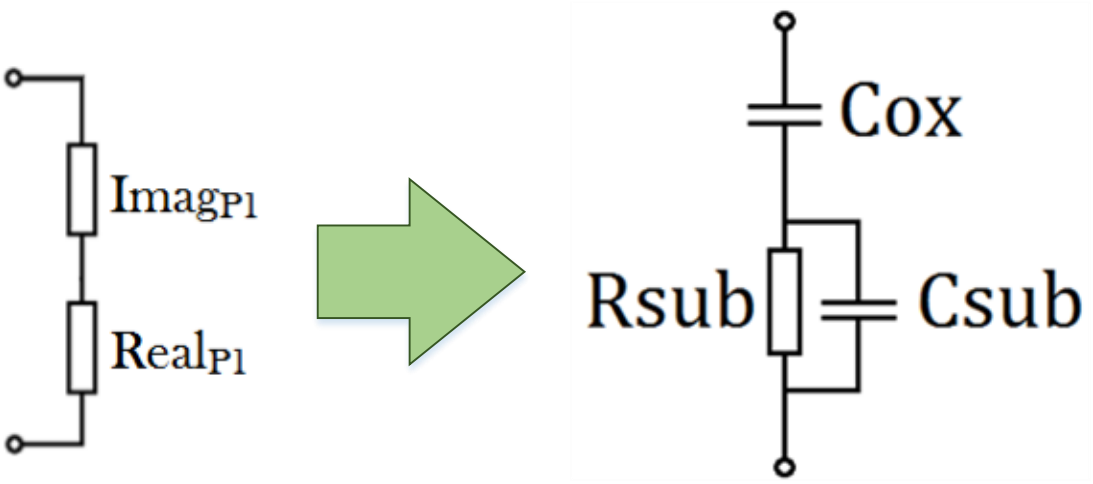

Figure 47 – Shunt model analysis

At lower frequencies, the parallel capacitance mainly represents C_{ox}, as C_{sub} is in parallel with R_{sub}, which masks the substrate effect for lower frequencies. In higher frequencies, a blend of C_{ox}, C_{sub} and R_{sub} appears in the curves.

The parallel resistance represents the substrate resistance loss. The shunt resistance low frequency analysis helps to direct at R_{sub}'s value, however, it is not determinant as the oxide capacitance presents a high influence at these frequencies. As the frequency increases, the C_{sub} effect in the parallel connection increases and these parameters data are harder to distinguish.

It is possible to estimate the values of these parameters; however, a broader range of frequency is required for this analysis, as C_{ox} is prominent in very low frequencies (to which we do not have access in these datasets).

Figure 48 presents the imaginary portion of the parallel branch results. It is noticeable that the single-layered inductor's oxide capacitance is lower than the double-layered elements' (55.3 fF for Ind1xM1, 75.8 fF for Ind2xM1 and 72.3 fF for Ind2xBFMOAT). This was expected, as the single-layered inductor presents and extra oxide layer, which diminishes its overall oxide capacitance.

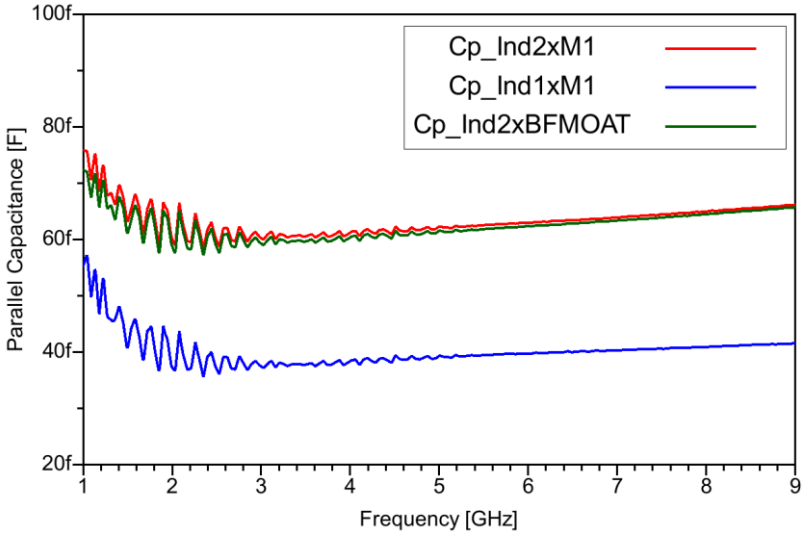

Figure 48 – Parallel imaginary portion comparison

Figure 49 shows the shunt branch real component. The high frequency results represents the parallel between $R_{sub}$and C_{sub}, and are close to each other (41.21 Ω for Ind2xM1, 53.64 Ω for Ind2xBFMOAT and 48.69 Ω for Ind1xM1).

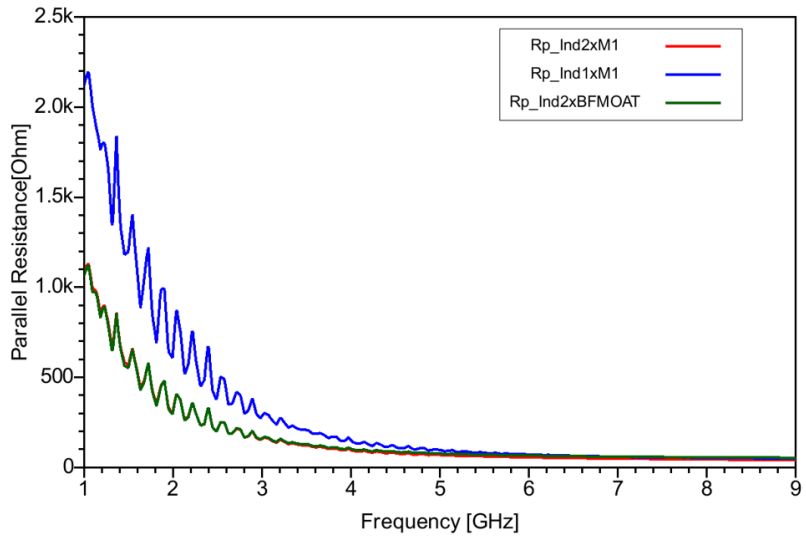

Figure 49 – Parallel Resistance Comparison

4.2.2. Figures of Merit

The equivalent inductance is presented in figure 50. As seen for the series branch, the single-layered inductor presents a higher equivalent inductance, and a significantly higher self-resonant frequency. The difference in the inductance value comes from the higher series inductance demonstrated in the previous section. The

self-resonant frequency increase is the result of the lower oxide capacitance presented by this element.

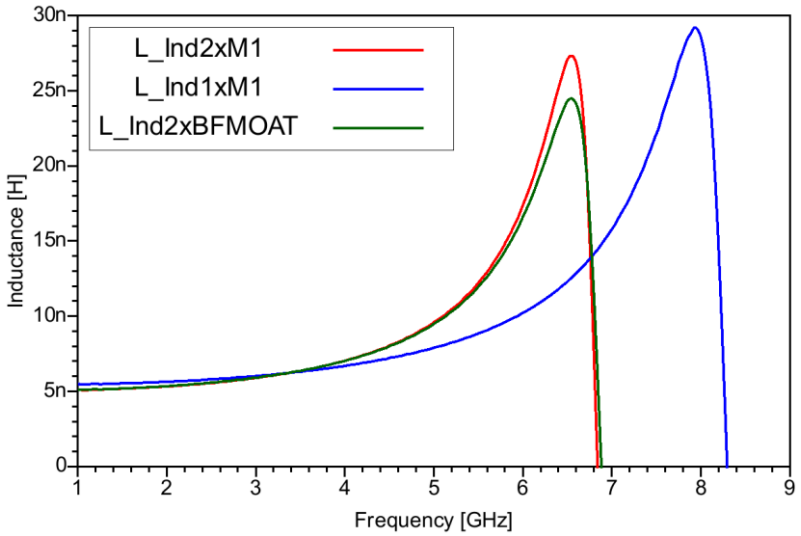

Figure 50 – Comparison between inductance from the fabricated inductors

The quality factor is presented in figure 51. A higher quality factor was expected from Ind2xM1, as the ground shield should reduce the parasitic current at the substrate due to the magnetic coupling (and the self-resonant frequency as a consequence), which is not perceived in this analysis.

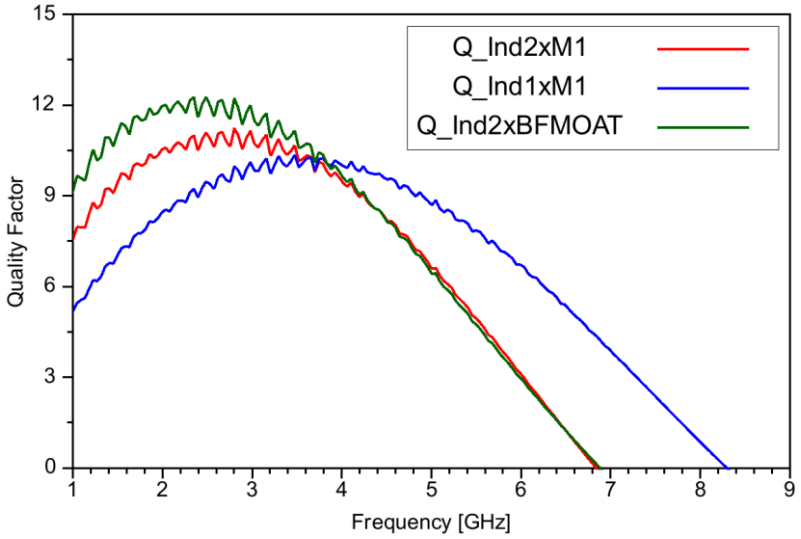

Figure 51 – Fabricated inductors' quality factor

Another possible analysis is the quality factor's high sensitivity to the low frequency series resistance. As it can be observed by the difference between the shielded elements' quality factors.

The higher low frequency inductance presented in the single layered inductor reflects in a higher equivalent inductance of the element, also the higher low frequency resistance is detrimental to this device's quality factor, which causes its reduction. The reduced capacitance presented by the single-layer inductor reflects at the element's self-resonant frequency, which will is higher.

Table 6 presents the equivalent inductance, self-resonant frequency and quality factor of the elements.

	Ind2xM1	**Ind2xBFMOAT**	**Ind1xM1**
LF Inductance	5.1 nH	5.1 nH	5.5 nH
Self-resonant Frequency	6.84 GHz	6.89 GHz	8.3 GHz
Maximum Quality Factor	11.2	12.2	10.3

Table 6 – Important parameters

4.3. Simulation Results

From this point on, the data set from the manufactured inductors are compared with the electromagnetic simulations and the design kit model (from this point on referred as GF model). The design kit model is presented in figure 52.

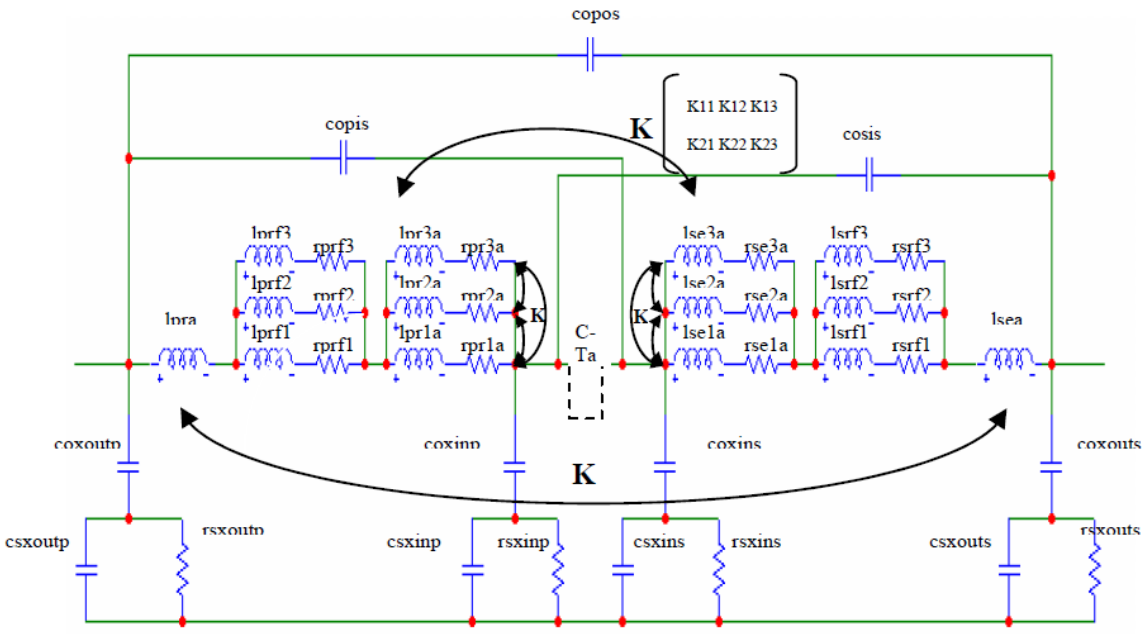

Figure 52 – Design kit model

This model tries to emulate the skin effect, proximity effects, turn-to-turn coupling capacitances, spiral to substrate capacitances the substrate parameters. Table 7 presents the elements related to each occasion.

Skin Effect	Rpr1a, Rse1a, Rpr2a, Rse2a, Rpr3a, Rse3a, Lpr1a, Lse1a, Lpr2a, Lse2a, Lpr3a, Lse3a, Lpra, Lsea
Proximity Effect	Rprf1, Rsrf, Rprf2, Rsrf2, Rprf3, Rsrf3, Lprf1, Lsrf1, Lprf2, Lsrf2, Lprf3, Lsrf3
Turn-to-turn Coupling Capacitances	Copis, Cosis, Copos
Spiral to Substrate Capacitances	Coxoutp, Coxouts, Coxinp, Coxins
Substrate Parameters	Rsxoutp, Rsxouts, Rsxinp, Rsxins, Csxoutp, Csxouts, Csxinp, Csxins

Table 7 – Design kit model parameter's description

Despite the dataset ranging from 1 to 10 GHz, the frequency range is presented only up to the resonant frequency, with the exception of the series inductance.

The electromagnetic simulation analysis refers to the overall performance of the fabricated elements. For this reason, the figures of merit and scattering parameters are presented. Sequentially, characteristics from the electromagnetic simulations are presented. The series and parallel branches parameters are presented in the Appendix C.

4.3.1. Inductor Ind2xM1

4.3.1.1. Equivalent Inductance

The first studied element is the double-layered shielded inductor, Ind2xM1. This inductor's equivalent inductance is shown in figure 53. Three critical points for the analysis can be highlighted: the low frequency inductance, the inductance's curve behavior and the self-resonant frequency.

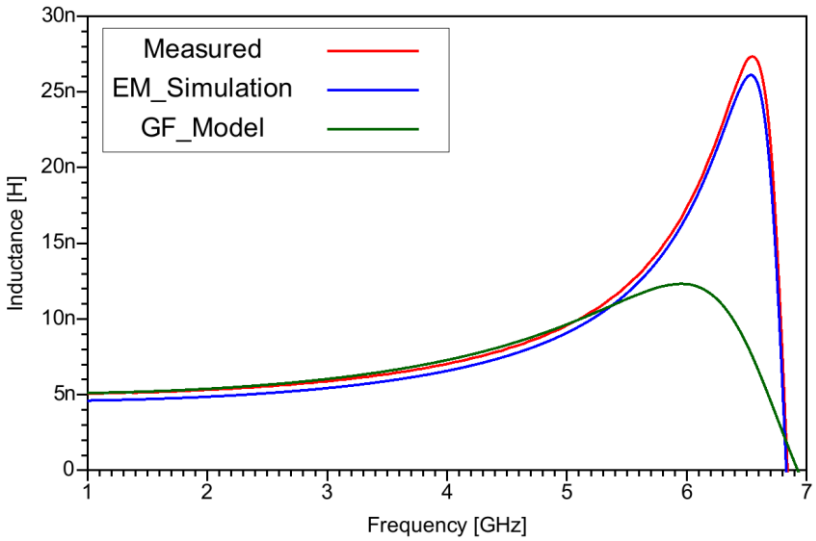

Figure 53 – Ind2xM1 equivalent inductance

As mentioned before, the frequency range is from 1 to 10 GHz. This restricts the low frequency results; and, from this point on, 1 GHz will be considered low frequency. In this case, the low frequency equivalent inductance between the GF model and the measured data is extremely close, and the electromagnetic simulated data is somewhat further from the measured data. Nevertheless, both data presents satisfactory results.

The simulated data present a very similar shape to the measured results, meanwhile, the GF model deviates greatly (especially at higher frequencies). Finally, the self-resonant frequency obtained for the GF simulated model differs a little from the target. The self-resonance of the electromagnetic simulation exhibits a remarkable proximity to the self-resonance of the measured data. These notable values are presented in table 8, with the percentual discrepancies from the measured data outlined in parenthesis.

	Low Frequency Inductance	**Self-Resonant Frequency**
Measured	5.1 nH	6.84 GHz
EM Simulation	4.6 nH (9.39%)	6.83 GHz (0.15%)
GF Model	5.1 nH (0.37%)	6.93 GHz (1.13%)

Table 8 – Ind2xM1's Equivalent Inductance Notable Parameters

4.3.1.2. Quality Factor

The element's quality factor is presented in figure 54. The electromagnetic simulated data present an overestimation of the real quality factor and a better

outcome than the model at higher frequencies. However, the discrepancy between the low frequency data is a lot more significant than the discrepancy present in the equivalent inductance. The electromagnetic simulation still presents a better overall result than the GF model, though. The maximum quality factor obtained at the measured data is 11.2 at 2.80 GHz, at the simulated data is 13.0 st 2.31 GHz and at the provided model is 13.3 at 1.82 GHz. This represents an overestimation of 15.68% from the electromagnetic simulation and the measured data; and an overestimation of 18.70% for the model. However, the electromagnetic simulation presents precise results for higher frequencies.

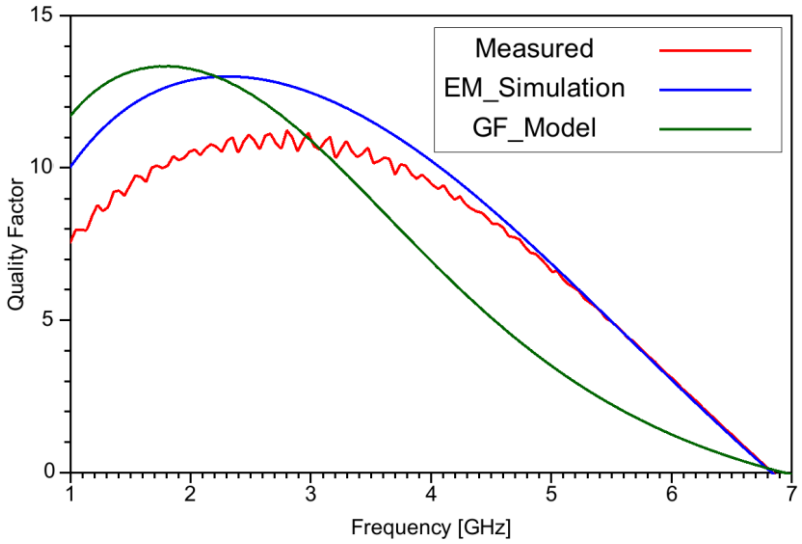

Figure 54 – Ind2xM1 quality factor

As in the equivalent inductance, the simulated self-resonant frequency is practically the same as the self-resonant frequency acquired from the measured data, and the provided GF model presents a small deviation.

4.3.1.3. Scattering Parameters

Figure 55 presents S_{11} for Ind2xM1. The left axis presents the magnitude while the right axis presents the phase.

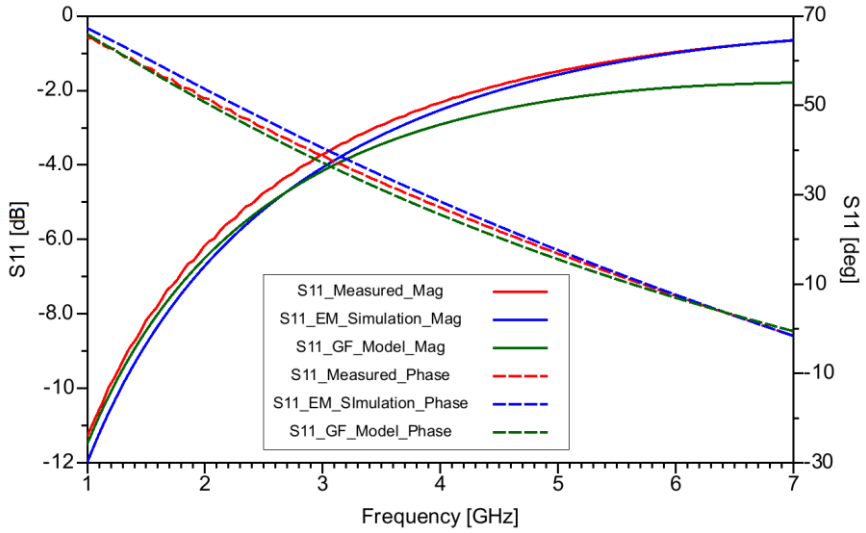

Figure 55 – Ind2xM1 S_{11} parameters

The S_{12} parameters of Ind2xM1 are presented in figures 56 while the S_{22} parameters are shown in figure 57.

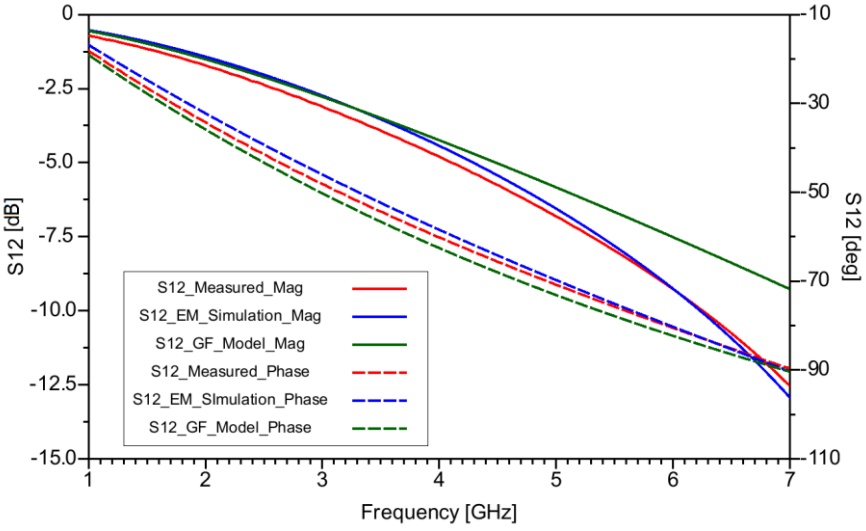

Figure 56 – Ind2xM1 S_{12} parameters

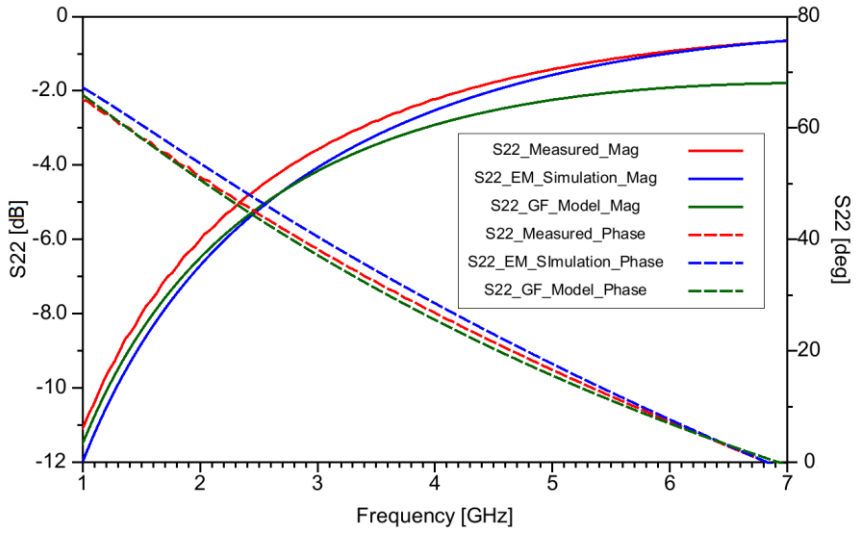

Figure 57 – Ind2xM1 S_{22} parameters

It is possible to see that the simulation presented a closer resemblance to the measured data than the model provided by the technology library for all the presented scattering parameters.

4.3.2. Inductor Ind2xBFMOAT

4.3.2.1. Equivalent Inductance

Figure 58 presents the equivalent inductance of Ind2xBFMOAT. This device's results are very similar to its shielded counterpart. The GF model presents an excellent low frequency result, but as the frequency increases, its performance as a model decreases drastically, culminating in an increased discrepancy of its self-resonant frequency.

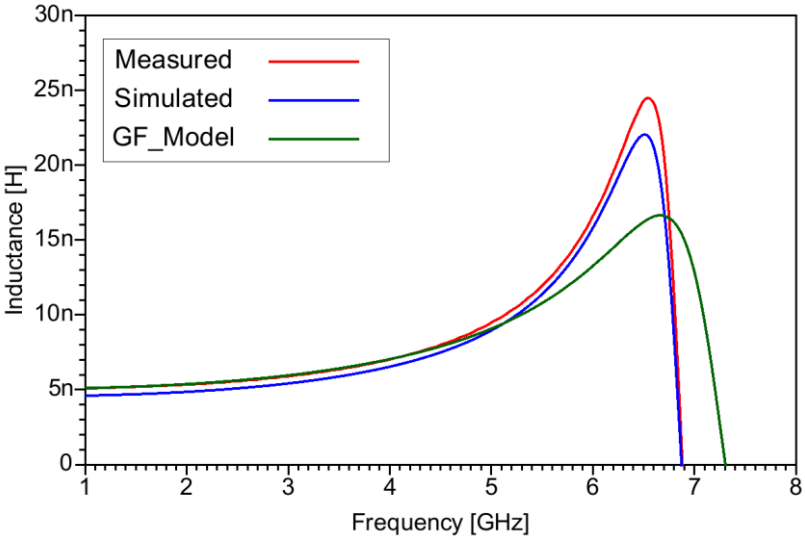

Figure 58 – Ind2xBFMOAT equivalent inductance

The electromagnetic simulation presents a lower equivalent inductance through all the frequency range and a consistent proximity to the measured data behavior. The low frequency equivalent inductance and the self-resonant frequency are shown in table 9. In parenthesis is presented the relative difference from the measured data.

	Low Frequency Inductance	**Self-Resonant Frequency**
Measured	5.110 nH	6.89 GHz
EM Simulation	4.606 nH (9.86%)	6.88 GHz (0.14%)
GF Model	5.108 nH (0.04%)	7.30 GHz (5.95%)

Table 9 – Ind2xBFMOAT Equivalent Inductance's Notable Parameters

4.3.2.2. Quality Factor

The quality factor for Ind2xBFMOAT is displayed in figure 59. As before, a small discrepancy is present in lower frequencies; however, for this element, the disparity is reduced. Once again, the electromagnetic simulation presents a higher quality factor than the measured data, and a better performance than the GF model.

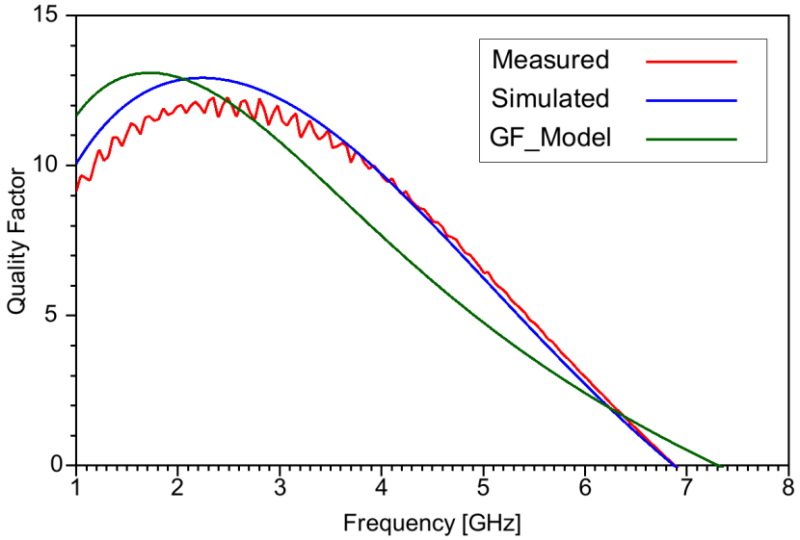

Figure 59 – Ind2xBFMOAT quality factor

The maximum quality factor obtained at the measured data is 12.2 at 2.35 GHz, while at the electromagnetic simulation is 12.9 at 2.2 GHz and 13.1 at 1.74 GHz at the model. This represents a discrepancy of 5.384% and 6.779% for the simulation and model respectively.

4.3.2.3. Scattering Parameters

Figure 60 shows S_{11} for the Ind2xBFMOAT inductor, while figures 61 and 62 present S_{12} and S_{22}, respectively.

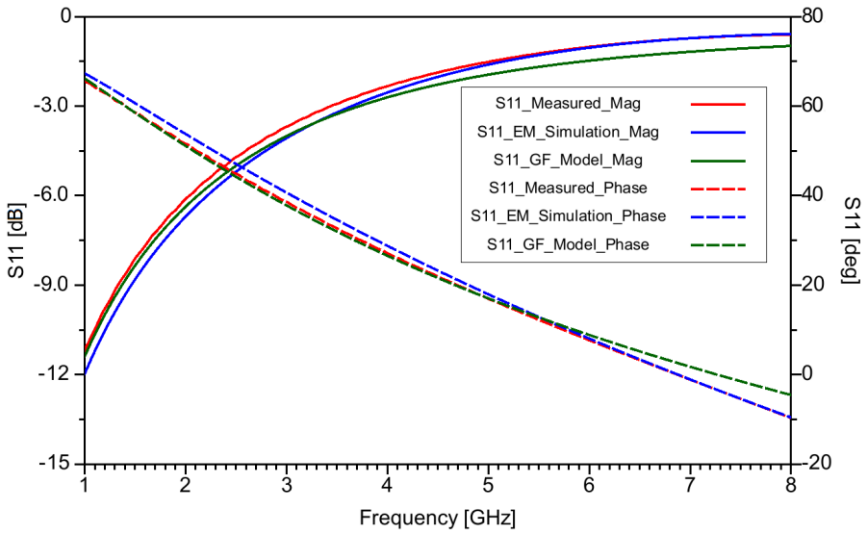

Figure 60 – S_{11} parameters

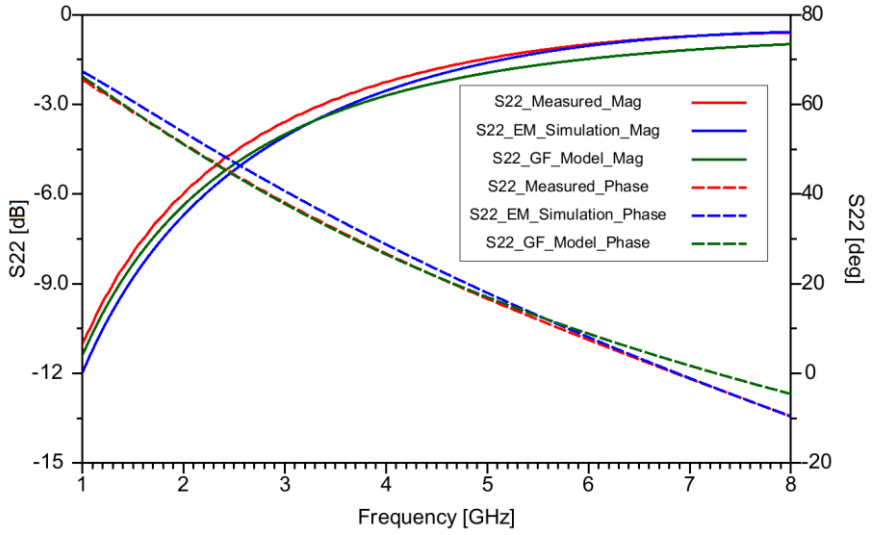

Figure 61 – S_{12} parameters

Once again, the scattering parameters of the simulation presents better results than the provided model. In this case, a larger discrepancy in the model can be perceived for frequencies higher than 4 GHz.

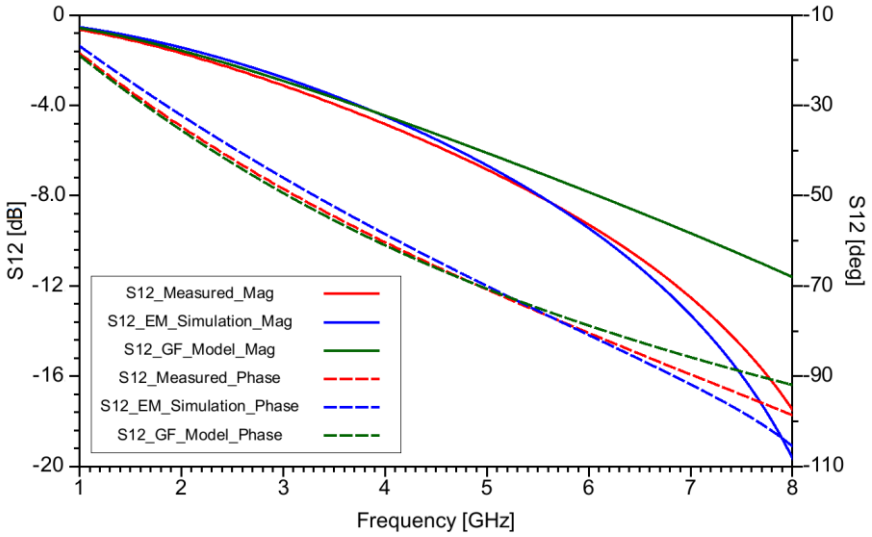

Figure 62 – Ind2xBFMOAT S_{22} parameters

4.3.3. Inductor Ind1xM1

The analysis for the shielded single-layered inductor Ind1xM1's data is compared only between the electromagnetic simulation and the measurement data, because this designed inductor was not part of the design kit's library. This means that this element does not possess a provided model by the foundry.

4.3.3.1. *Equivalent Inductance*

The equivalent inductance is presented at figure 63. It is possible to notice that the small low frequency discrepancy is still present. The self-resonant frequency presents a slight shift. The divergences are the same as the evaluated for the previous elements, which are a lower low frequency equivalent inductance and self-resonant frequency.

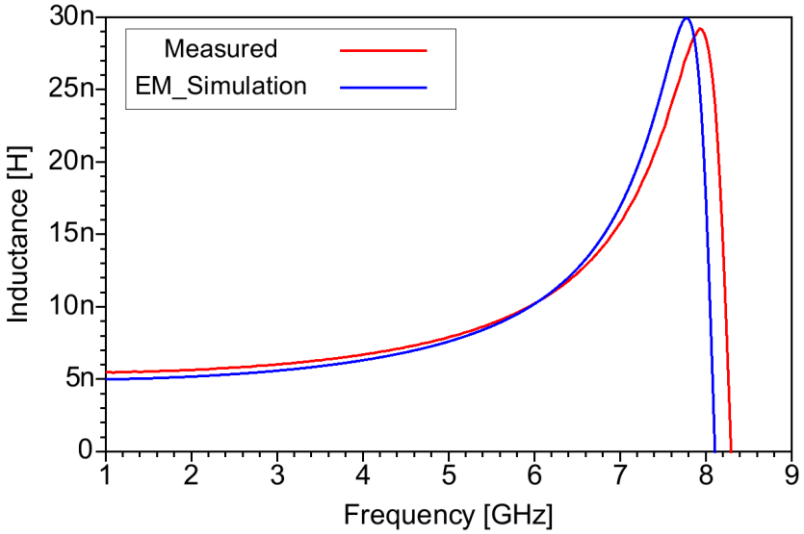

Figure 63 – Ind1xM1 equivalent inductance

Table 10 provides Ind1xM1's data notable parameters.

	Low Frequency Inductance	**Self-Resonant Frequency**
Measured	5.5 nH	8.300 GHz
EM Simulation	5.0 nH (9.25%)	8.110 GHz (2.29%)

Table 10 – Ind2xBFMOAT Equivalent Inductance's Notable Parameters

4.3.3.2. *Quality Factor*

The quality factor, presented in figure 64, shows an even closer result for lower frequencies than Ind2xBFMOAT. Once again, the quality factor for lower frequencies is smaller for the measured data than the simulation. As the self-resonant frequency manifests a shift at the simulated data, the higher frequency response is not as optimal as the previous elements.

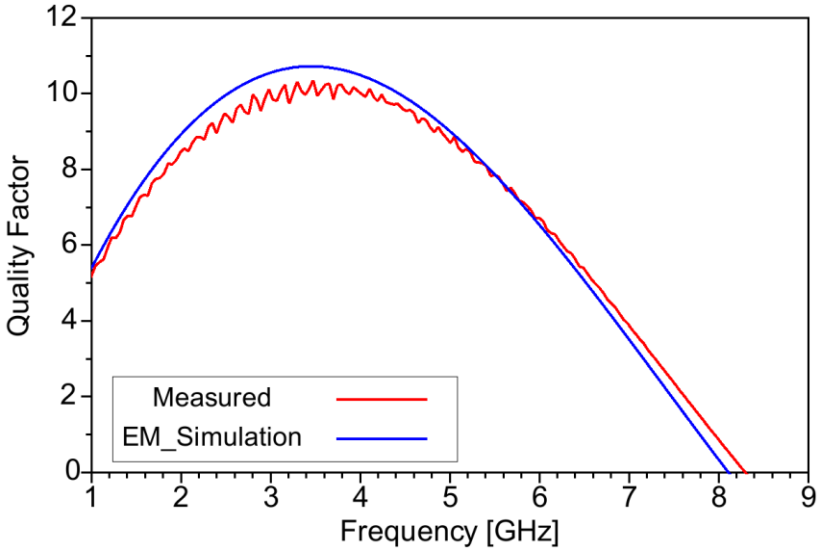

Figure 64 – Ind1xM1 quality factor

The quality factor for the simulation is 10.7 at 3.44 GHz and for the measured data is 10.3 at 3.47 GHz. This means that the quality factor is overestimated by 3.715%.

4.3.3.3. Scattering Parameters

Figure 65 shows S_{11} of the single-layered element. As previously, the results are significantly close and accurately represent the element's behavior.

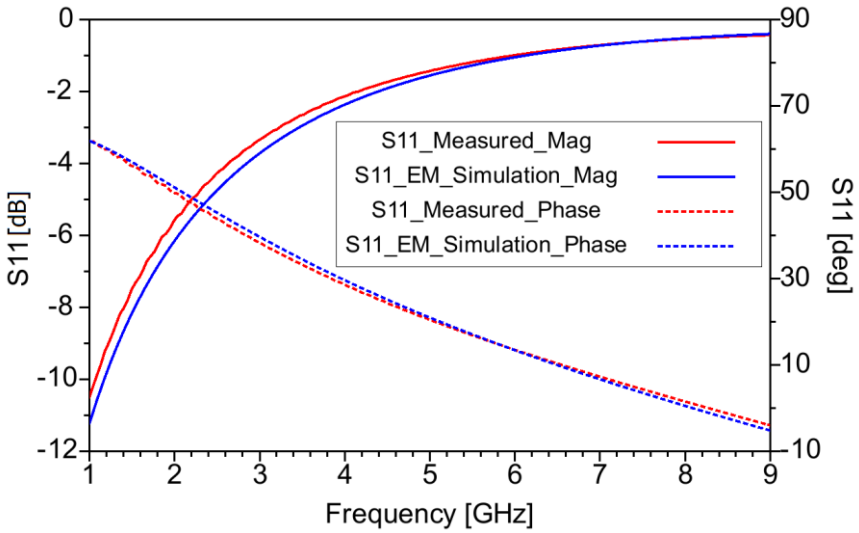

Figure 65 – Ind1xM1 S_{11} parameters

Figures 66 and 67 show the S_{12} and S_{22} parameters of the single-layered inductor, respectively. It is noticeable the similarities of the simulated results to the measurement data.

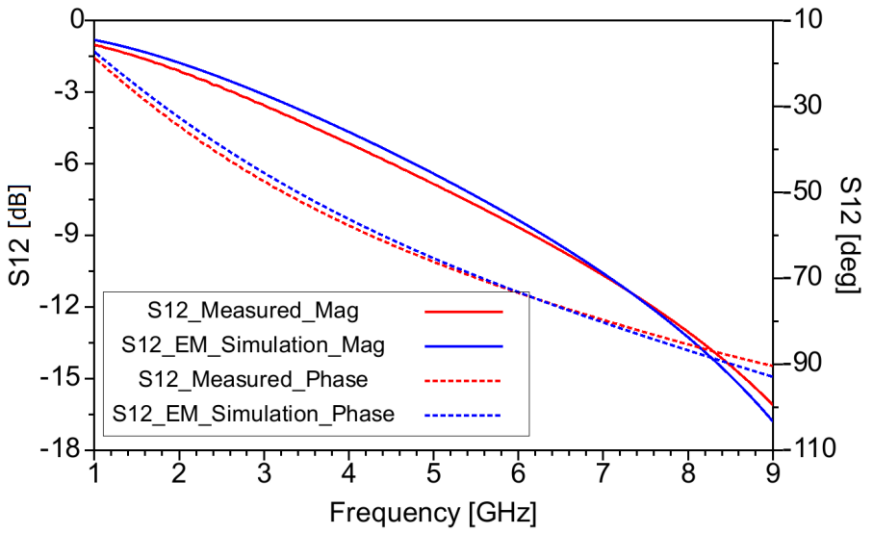

Figure 66 – S_{12} parameters

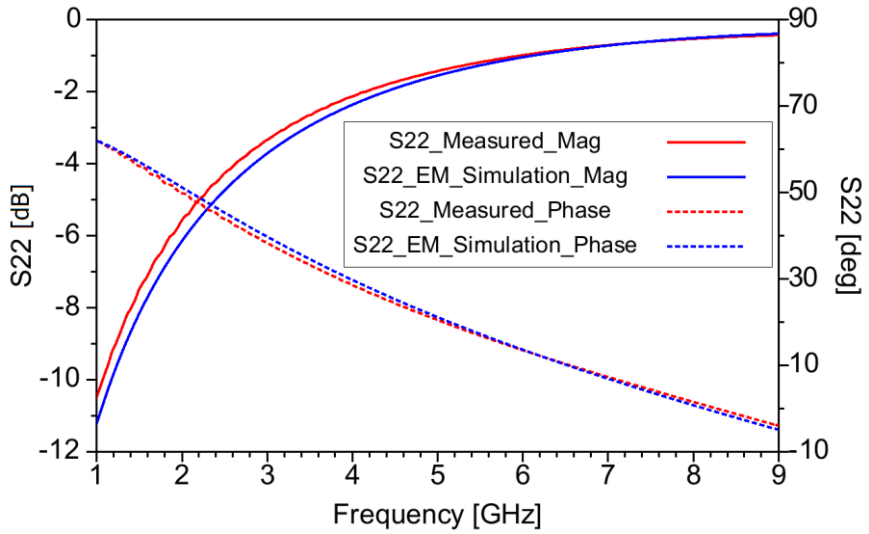

Figure 67 – S_{22} parameters

4.4. CONSIDERATIONS

In order to keep track of the discrepancies between the electromagnetic simulation and the measured data, a table was compiled. Table 11 shows a simplified analysis of the 18 diagrams data presented in the previous sections, where it is stated if the simulated data is higher (in red) or lower (in blue) than the measured data and by how much.

	Ind2xM1	Ind2xBFMOAT	Ind1xM1
Low Frequency L	9.39% Lower	9.86% Lower	9.25% Lower
Self-Resonant Frequency	0.15% Lower	0.14% Lower	2.29% Lower
Maximum Q	15.7% Higher	5.38% Higher	3.72% Higher
Low Frequency R_s	28.7% Lower	13.95% Lower	10.5% Lower
Higher Frequency R_s	21.6% Lower	132.2% Lower	16.1% Lower
Low Frequency L_s	9.55% Lower	9.95% Lower	9.52% Lower
Higher Frequency L_s	3.54% Higher	7.82% Higher	3.29% Higher
Low Frequency R_p	92.7% Lower	90.6% Lower	97.1% Lower
Higher Frequency R_p	17.9% Higher	49.2% Higher	2.43% Lower
Low Frequency C_p	13.7% Lower	11.4% Lower	19.2% Lower
Higher Frequency C_p	2.29% Lower	4.15% Lower	5.88% Higher

Table 11 – Electromagnetic simulation performance

The objective of table 11 is to simplify the simulation behavior for the different inductors. This cannot be used to offer a deep analysis of the parameters, since curve behavior cannot be expressed in the table; however, it is enough to make some assumptions.

As practically all of the discrepancies present at the analysis parameters possess the same behavior for all of the different inductors, we can conclude that these discrepancies are most likely generated from a common source. These common sources could be the configuration of the simulations, adaptation of the ground plane, uncertainties from the measurement process, or de-embedding process.

4.4.1. De-embedding the series effects

The main discrepancy between the electromagnetic simulation and the measurement data is present in the quality factor, which reflects a disagreement between the measured and simulated series resistance. As the *open* de-embedding does not consider the series effects of the circuit's interconnections and the electromagnetic simulation proved its accuracy in the previous section, a simulation of a *short* fixture is presented and embedded in the simulated data. This is proposed in order to reduce discrepancies between simulated and measured data.

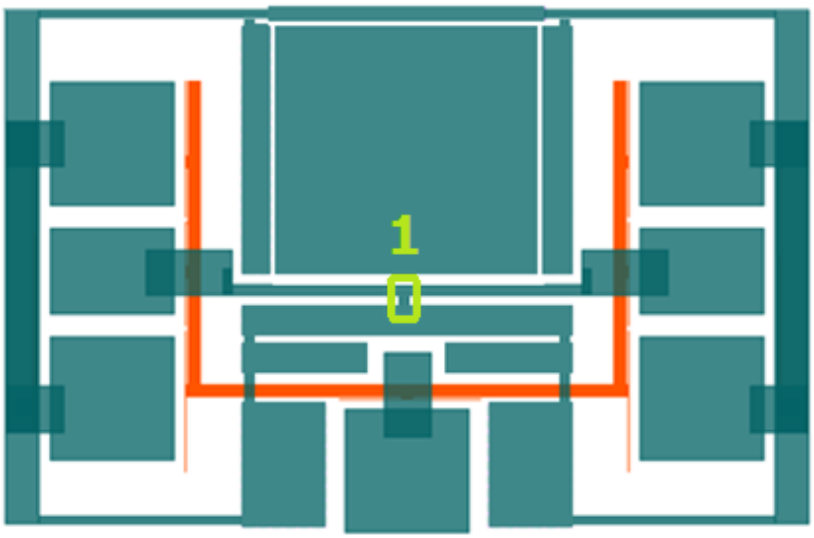

Figure 68 – Simulated Short Fixture

The short fixture is shown in figure 68. The defining characteristic of a *short* fixture, is the short between the signal and ground pads. This connection is marked in 1. As before, the ground blocks were replaced by solid structures in order to reduce simulation time. The simulation ports are located in the extremity of the pads, where each port is comprised of 3 pins, a positive pin located in the *signal* portion of the pad and two pins located at the *ground* portion.

The data obtained in this simulation are incorporated into the simulated inductors by adding the impedance matrix to the inductor's impedance matrix. The obtained results for Ind2xM1 are presented in figure 69. The red curve represents the de-embedded measured data, the blue curve represents the simulated data, and the green curve is the simulated data with the *short* fixture embedded into it.

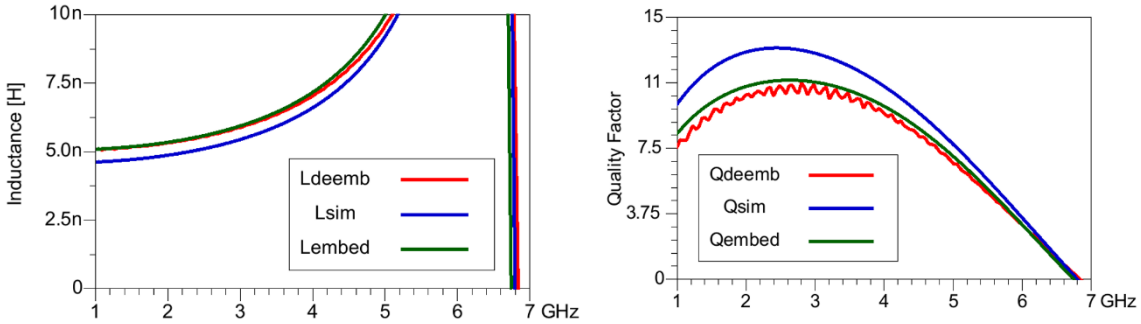

Figure 69 – Embedded equivalent inductance and quality factor

Table 12 provides the notable parameters, and a sensible difference in the parameters is noticed.

	Low Frequency Inductance	Self-Resonant Frequency	Maximum Quality Factor
Measured	5.1 nH	6.84 GHz	11.2
Embedded	5.1 nH	6.78 GHz	11.1
EM Simulation	4.6 nH	6.83 GHz	13.0

Table 12 – Ind2xM1 notable Parameters

Likewise, Figure 70 shows the equivalent inductance and the quality factor for Ind2xBFMOAT. A reduction in the quality factor, and improvement in the low frequency inductance is also notice here. In this case, however, the quality factor improvement is not as evident as before.

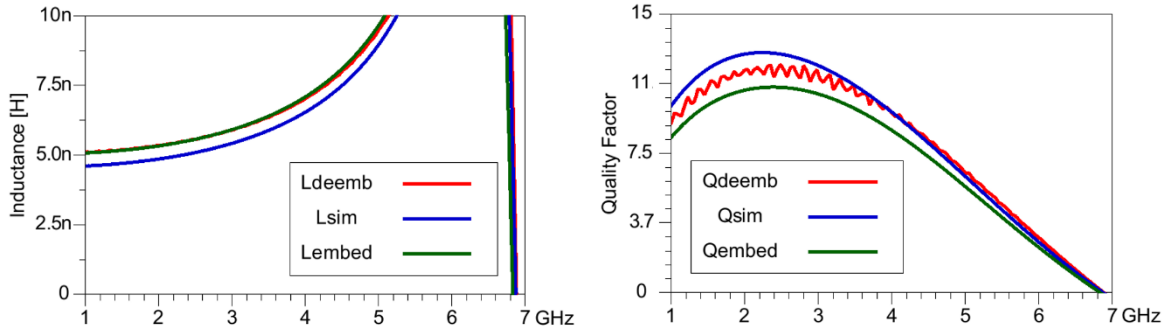

Figure 70 – Embedded equivalent inductance and quality factor for Ind2xBFMOAT

Table 13 provides the notable parameters; this time, the maximum quality factor for the embedded simulation is farther from the measured data than the original simulation, however, the low frequency inductance, once again, is on point.

	Low Frequency Inductance	Self-Resonant Frequency	Maximum Quality Factor
Measured	5.1 nH	6.89 GHz	12.3
Embedded	5.1 nH	6.84 GHz	11.1
EM Simulation	4.6 nH	6.88 GHz	12.9

Table 13 – Ind2xBFMOAT notable Parameters

Finally, figure 71 and table 14 show the comparison for the single layered inductor.

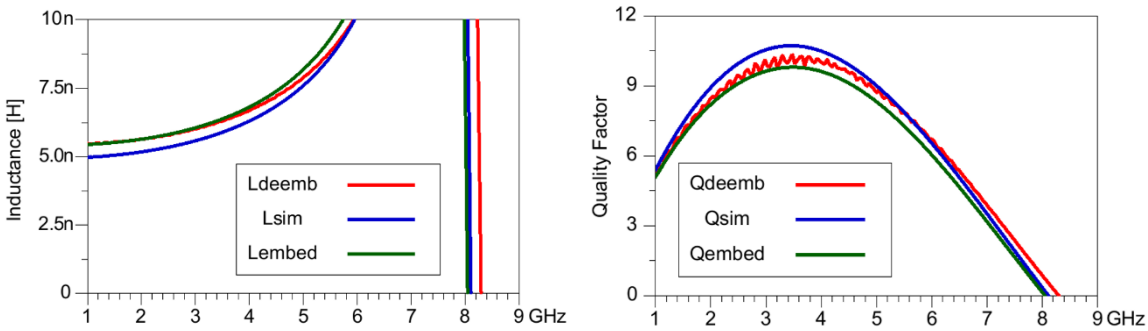

Figure 71 - Embedded equivalent inductance and quality factor for Ind1xM1

	Low Frequency Inductance	Self-Resonant Frequency	Maximum Quality Factor
Measured	5.5 nH	8.30 GHz	10.3
Embedded	5.4 nH	8.04 GHz	9.80
EM Simulation	5.0 nH	8.11 GHz	10.7

Table 14 – Ind1xM1 notable Parameters

From the analysis of the results presented in this section, we can affirm that the de-embedding is the main reason for the discrepancy in the series parameters. The addition of the series effects into the analysis showed a significant improvement in the low frequency inductance. In some instances, the quality factor presented a decrement in its precision. However, the overall results are positive.

5.CONCLUSIONS

5.1. SUMMARY

With the increasing popularity of fully integrated devices, the use of on-chip passive elements skyrocketed. In order to apply these elements, it is required to guarantee their quality and competent optimization, especially for inductors. The design of these devices is particularly intricate, as their operation heavily depends on their geometry. However, these geometric parameters influence on the device performance is convoluted.

The insertion of modifications into the standard CMOS process is a technique applied to improve inductors overall performance. However, these modifications tend to increase the manufacturing costs of the circuits, which limit their implementation. Another option is to use predesigned cells provided by foundries. These parameterized cells normally possess electrical models attached to them that greatly simplify the design process. Because the cells are predesigned, this method ends up restricting the designer, as a limited number of elements can be created, impairing the fine tuning (and consequent optimization) of these elements.

In order to achieve the needed flexibility when designing passive devices, the use of electromagnetic simulations to predict these devices behavior is a common practice. Obviously, this process greatly benefits from the designer's expertise.

This led us to the two main objectives of this work: the creation and analysis process (which involves the design, manufacturing, measurement, and characterization) of three integrated inductors and the familiarization with the electromagnetic simulation environment (and its consequent evaluation).

The first objective assisted in elucidating the whole design process and inductor behavior, as well as analysis parameters and figures of merit commonly utilized. The second main objective introduced the peculiarities of the electromagnetic simulation environment, with its required adaptations, as well as determine the simulations accuracy and elementary configuration settings.

Achieving these objectives will assist in developing a complete design methodology (from the elements conception to its manufacturing) for integrated inductors. This can be broadened to any manner of integrated passive elements, due

to the flexibility provided by the electromagnetic simulation, such as alternate topologies, transformers, or even different CMOS technologies.

The work was divided into four mains sections: bibliography research, layout procedure, electromagnetic simulations, and data analysis. The bibliography research laid the foundation to the diverse selected design choices and presented figures of merit and analysis parameters that would grant diverse options in the investigation of the obtained data.

The layout procedure started by analyzing the inductors topology provided by the foundry and a double-layered symmetric topology placed in the topmost layers (MA and E1) was elected. Next, the differences between the three devices were determined: the ground shield and the number of layers of the elements. Therefore, one of the inductors incorporated a M1 patterned shield (called Ind2xM1), and in a second inductor, this shield was removed (referred as Ind2xBFMOAT). The third inductor (labeled Ind1xM1) would then be a single-layered element. However, the provided library did not include a single-layered inductor and this element was manually designed by removing the E1 layer from the provided topology layout (which enforces the aforementioned claim about the flexibility when designing passive devices). All of the inductors possessed 190 µm of diameter, a trace width of 5 µm, as well as 5 µm turn-to-turn separation and 6 turns. An open element to realize the de-embedding of the data was also designed.

The chosen simulation method was the finite elements method, for providing a 3D analysis of the electromagnetic problem. Besides the simulation method, the simulation environment with all the technology's characteristics had to be created. The designed layout was then imported to the simulation software and accordingly adapted. The simulator was then pre-configured and the simulations performed. When the measurement data were available, the simulations configuration settings were fine-tuned to exhibit the closer results to the available data.

The data inspection started with the fabricated inductors comparison and characterization. The evaluated analysis parameters were the series branch real and imaginary segments, followed by the real and imaginary part of the shunt branch. The major consequences for the design choices were observed in this comparison.

The series resistance for the single-layered element presented a 61.3% increment (3.946 Ω against 6.364 Ω). The series inductance also suffered a small (8.2%) increment, 5.04 nH for the double-layered element versus 5.5 nH for the single layered inductor. However, the capacitive component of the shunt branch presented a reduction from 75.8 fF (of the double-layered element) to 55.3 fF (of the single-layered one). The shield presence did not influence much in the inductors characteristics, that could be caused by a misconnection at the shield in the layout phase. The most noticeable parameters discrepancy was series resistance, that exhibited a 17.53% decrease with the removal of the shield (from 3.946 Ω to 3.254 Ω). These differences in the analysis parameters resulted in a significant increase in the single-layered inductor self-resonant frequency (6.84 GHz for the double-layered inductor versus 8.3 GHz for the single-layered); however, a mitigation in the maximum quality factor was also observed (11.2 for Ind2xM1 versus 10.3 for Ind1xM1). Even though Ind2xM1 and Ind2xBFMOAT presented a similar operation overall, the exception of the series resistance was enough to increase Ind2xBFMOAT's maximum quality factor from 11.2 to 12.2.

Sequentially, the electromagnetic simulation data were compared to the measurement data and the model provided by the foundry. Overall, the results for the low frequency were slightly better for the electric model than the electromagnetic simulation, however, the difference shown for this frequency range was not exacerbated. The electromagnetic simulation presented a clear superior performance in predicting the higher frequency behavior than the electric model, including the prediction of the self-resonant frequency.

Based on the shown comparison, the applicability of electromagnetic simulations to predict inductors behavior can be deemed satisfactory. The similar curve's shape and magnitude support this idea. However, some caution must be taken, as these slight discrepancies can alter the element's operation. The quality factor is especially important because of the more substantial deviation from simulated and measured data. Despite present, the discrepancies between the electromagnetic simulation and measurement data, were consistent, which appoints to a common error factor, such as the de-embedding and measurement process, as well as the simulator's configuration.

5.2. FUTURE WORKS

Possible future works involve two different ideas: to optimize the current work in order to present better results and to use it as basis to explore related ideas. Both fields are equally important; therefore, suggestions on both fronts are presented. Looking to improve this work, the main targets are to revisit the ground shield's role in the manufactured elements and decrease the electromagnetic simulation discrepancy to the measured data.

A design revision is a good starting point, as it could potentially solve both problems. Besides that, the alteration of the de-embedding method may bring better results; however, this is not a guaranteed proposition. Another idea is to produce simpler inductors in order to identify inconsistent parameters more easily, and compare said parameters to physically calculated instances. By identifying the disagreeing parameters, the electromagnetic layout can be analyzed and individual errors may be perceived. This proposal could also be used to produce a predictive electric model for these devices. Parameters such as the series resistance, oxide capacitance, substrate resistance, and substrate capacitance are easily calculated from simple physical propositions. For the series inductance, several works present different approaches to infer this parameter's value. Altering some configuration options not explored in this work is another alternative. Advanced mesh and preprocessor configurations are some examples. Finally, a physical parameters verification for the metal and oxide layers is interesting as well, especially BFMOAT, PC, and CA that were manually configured.

The executed work can be expanded by taking advantage of the freedom provided by the electromagnetic simulations. The most obvious contribution is suggesting diverse new integrated inductor's topologies with their consequent electromagnetic simulations in order to compare the improvements or drawbacks achieved and subsequent manufacturing. The study of already cemented devices with proven utility, such as transformers, that present an even higher challenge to design than inductors and therefore, are usually not included in design kits provided by foundries.

The establishment of electrical models with parameters calculated based in their physical operation in order to predict inductor behavior, which would be a great

starting point in developing a design method for these devices, is another option. In addition, the analysis of symmetric inductors as 3-port devices by attaching a center tap to it is interesting as well.

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APPENDIX A: SURFACE IMPEDANCE VERSUS MESHED INTERIOR CONFIGURATION

This section presents a comparison between the precision of the different metal model settings. Figures A.1, A.2 and A.3 present a comparison between the meshed interior and surface impedance in relation to the measured results in all the fabricated inductors. It is possible to notice that the meshed interior configuration presents a better accuracy in lower frequencies and is observed mainly in the quality factor.

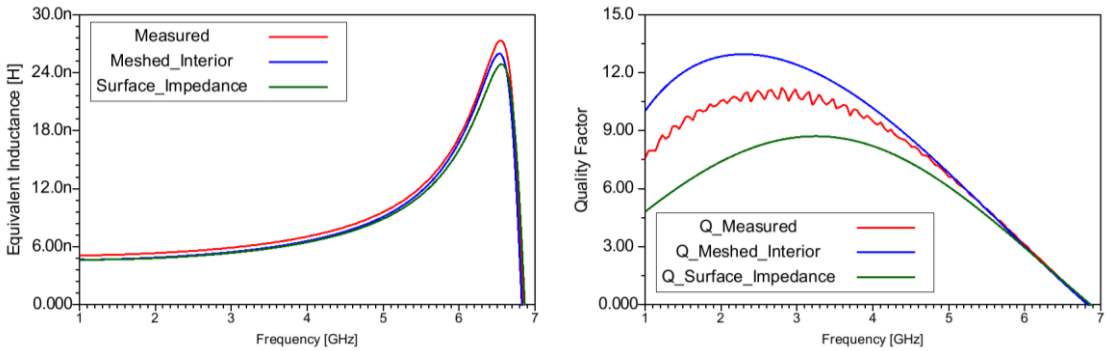

Figure A.1 – Figures of merit from Ind2xM1

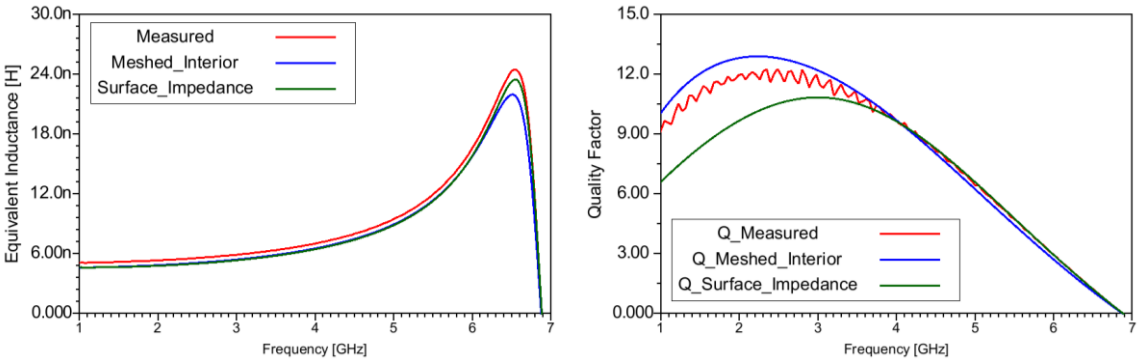

Figure A.2 – Figures of merit from Ind2xBFMOAT

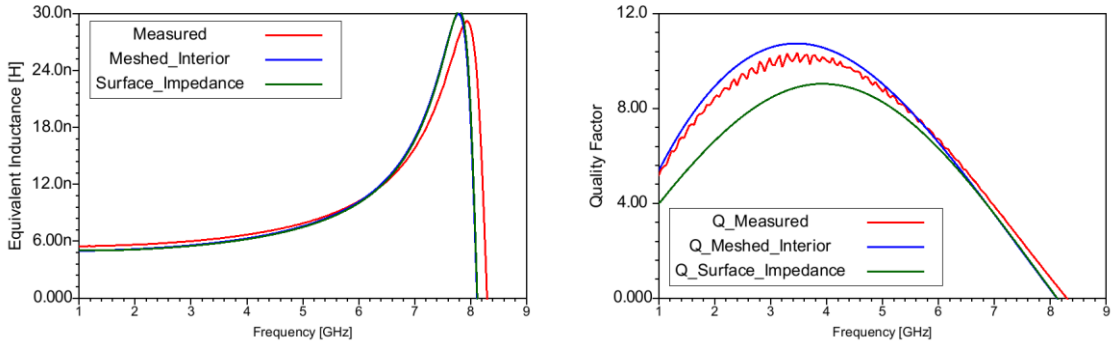

Figure A.3 – Figures of merit from Ind1xM1

APPENDIX B: ELECTROMAGNETIC SIMULATIONS GENERATED MESH

Figures B.1, B.2 and B.3 show a portion of Ind2xM1, Ind2xBFMOAT and Ind1xM1 along with the initial mesh generated for their electromagnetic simulation. The final mesh is obtain through the refining of this mesh, according to the simulations settings selected.

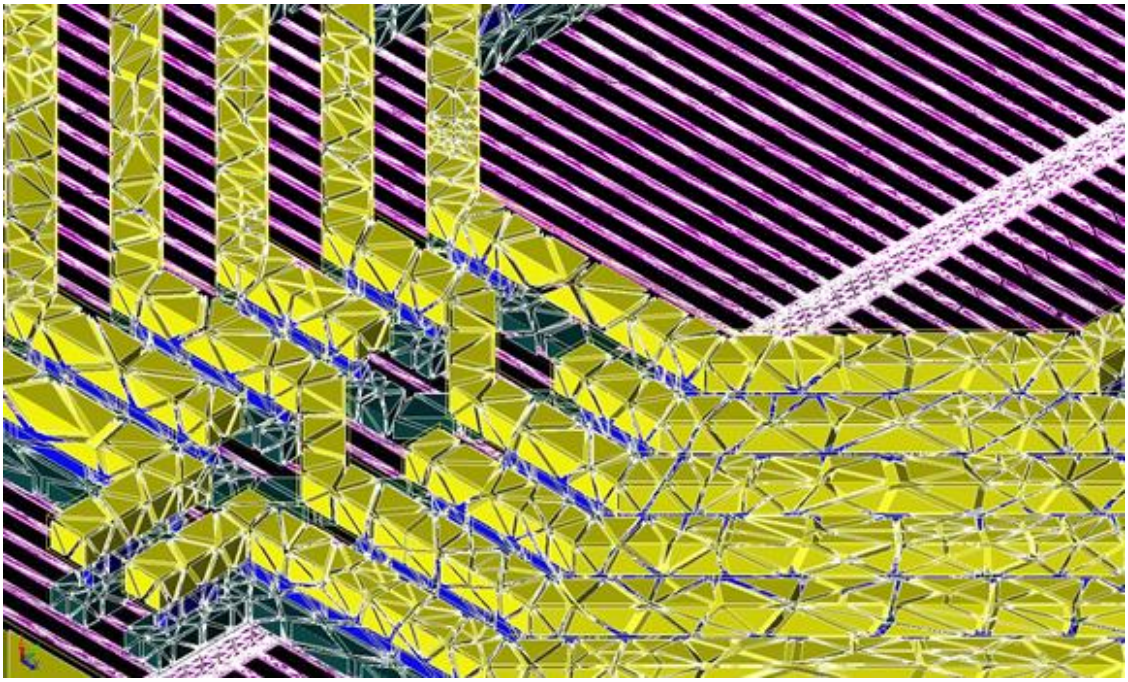

Figure B.1 – Ind2xM1 created mesh

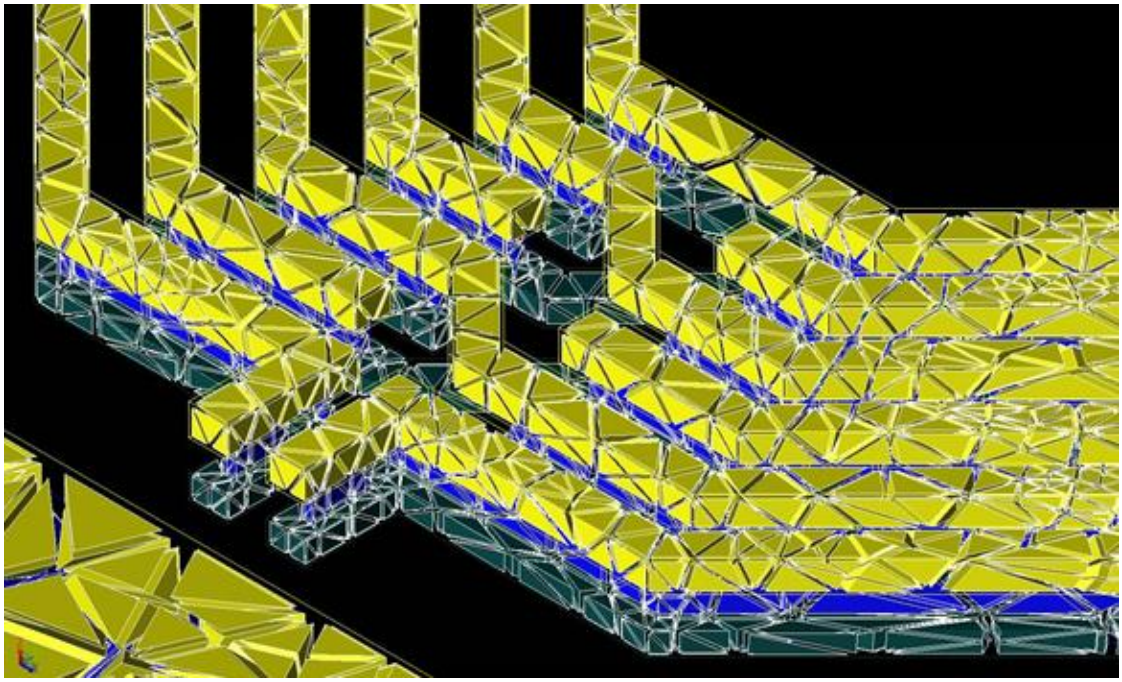

Figure B.2 – Ind2xBFMOAT created mesh

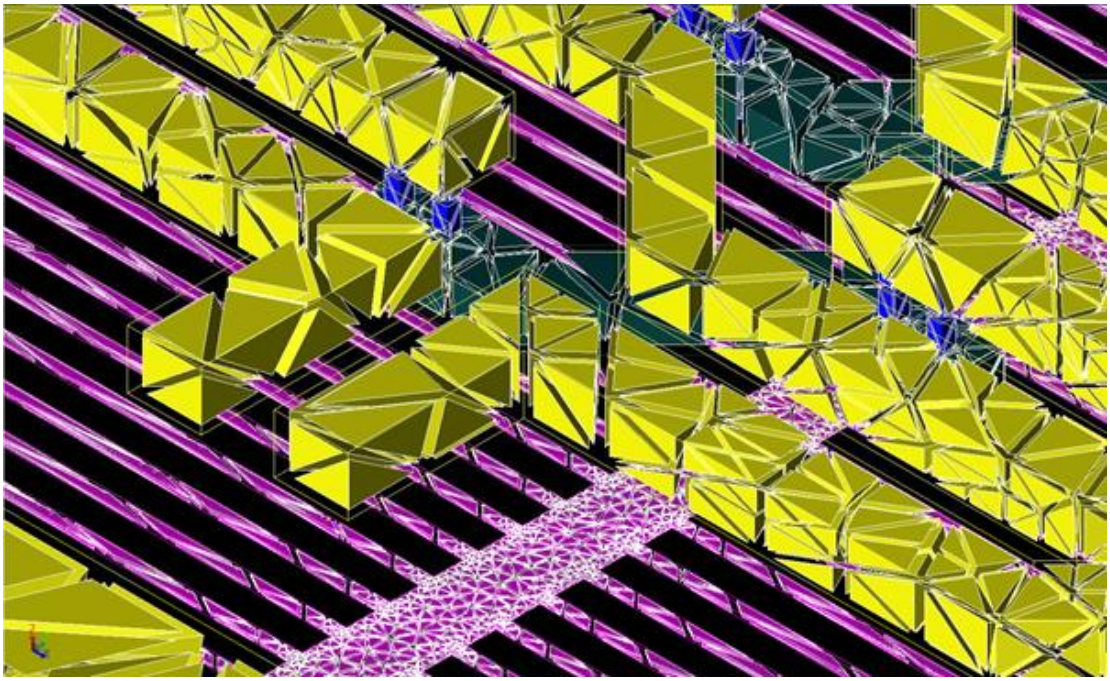

Figure B.3 – Ind1xM1 created mesh

APPENDIX C: ELECTROMAGNETIC SIMULATION SERIES AND PARALLEL ANALYSIS.

Ind2xM1

- *Series Resistance*

The series resistance is presented in figure C.1. This parameter indicates the real part of a π model based on the admittance parameters, and can be interpreted as the series resistance in a π behavior model. At DC, the inductor behaves like a series resistor, therefore, there should be no difference between the DC series resistance from the simulated and measured results. However, the data analyzed is for a frequency of 1 GHz, well above DC. This may be the reason for the perceived discrepancy.

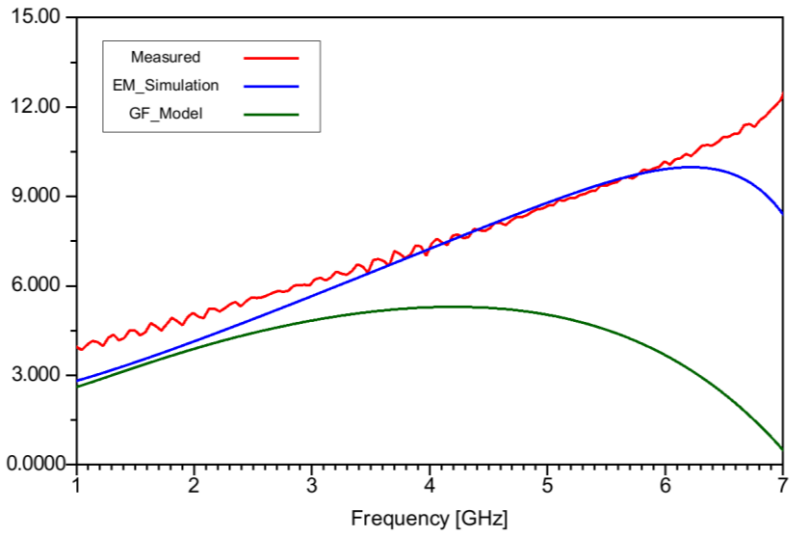

Figure C.1 – Ind2xM1 series resistance

By analyzing the form of the curves, it is not likely that the series resistance would be the same at DC. This means that there could be a discrepancy at each other inductor's cross sections (for manufacturing variations, or simulation misconfiguration), but as the length of the analyzed inductor is relatively high, this is unlikely as this would probably propagate through the entire coil and the difference would probably be more significant.

This divergence in the series resistance reflects directly in the quality factor analysis. As seen before, a small deviation in the resistance appears as a large discrepancy at the low frequency quality factor.

- *Series Inductance*

Figure C.2 shows the series inductance from Ind2xM1. The interpretation of the curves is similar to the series resistance. The low frequency GF model data is close to the measurement results and the simulated, once again, shows a closer proximity in the higher frequencies. The low frequency analysis is preferred because of the impact that the parasitic capacitance and skin effect applies to the series inductance as the frequency increases, which convolutes the variables involved in the analysis.

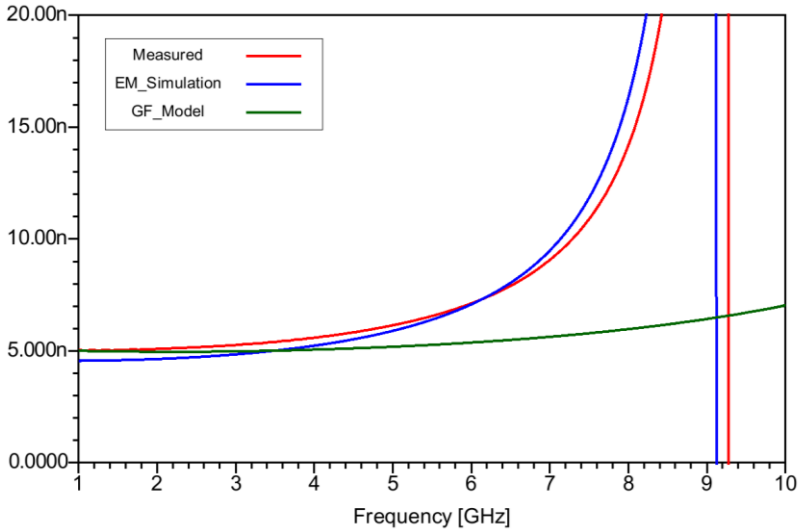

Figure C.2 – Ind2xM1 series inductance

The low frequency electromagnetic simulation data present a lower series inductance than the measured data. The ground ring surrounding the manufactured inductor can induce this effect, as the layout of the simulated data is not exactly the same as the manufactured, allowing some discrepancies to appear. The layer's oxide configuration may also play a role in the series inductance disparity. Overall, though, the simulated data is relatively close to the goal that is the measured inductor.

- *Parallel Capacitance*

The parallel capacitance, shown in figure C.3, depicts a good result for the electromagnetic simulation. Despite the natural variation of the measurement, it is

possible to notice that the simulated data is within the same magnitude range through all of the considered frequency. Incidentally, the model data is not optimal and performs poorly to describe the capacitance of the shunt branches.

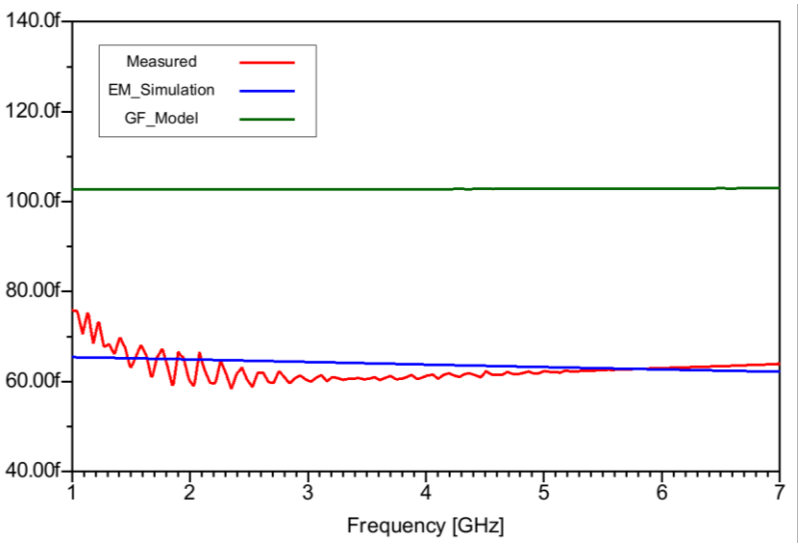

Figure C.3 – Ind2xM1 shunt capacitance

- *Parallel Resistance*

Figure C.4 shows the shunt resistance of Ind2xM1. The discrepancy between the low frequency measured and simulated data, despite being impressive (1089 Ω for the measured data versus 79.60 Ω for the simulated and 68.43 Ω for the Global Foundries model) is less relevant, as this impedance is mainly influenced by the oxide's capacitance at low frequencies. Even so, this can be caused by underestimating the losses present in the substrate when configuring the simulation. That could be produced by a lapse in defining the BFMOAT layer's characteristics, as the technology manual was not very clear in the conductive attributes of said layer.

As the imported technology file did not consider the lower layers in its configuration, it is possible that the substrate was not properly configured either. However, without further investigation it is not possible to precise the cause. As the GF model and simulated data present a similar response, an error in the measurement or de-embedding process can be considered possible causes for this discrepancy.

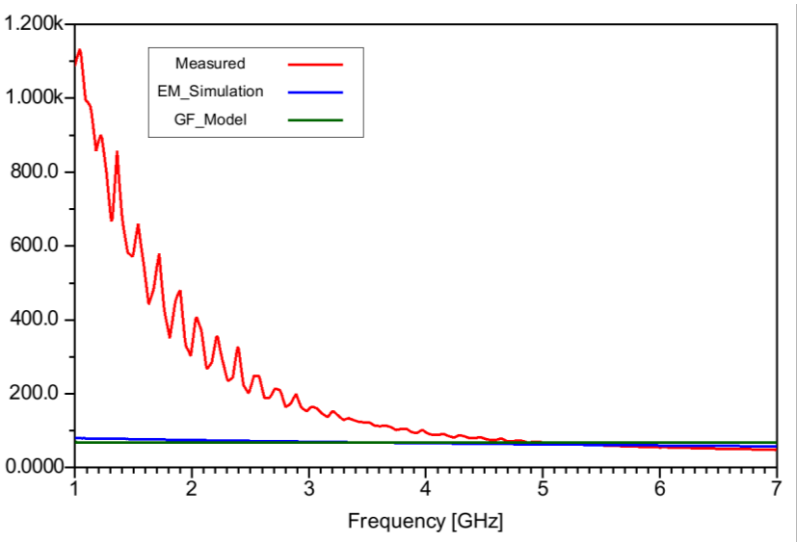

Figure C.4 – Ind2xM1 shunt resistance

Ind2xBFMOAT

- *Series Resistance*

Figure C.5 shows the series resistance for Ind2xBFMOAT. As before, the low frequency analysis suggests a small difference between the measured and simulated (GF model and electromagnetic) data. However, this discrepancy is smaller for the *shieldless* inductor.

At higher frequencies, the model is more accurate to the measured data than the electromagnetic simulation. Nevertheless, a higher frequency investigation indicates that the behavior of the curve for the electromagnetic simulation is more similar to the measured data than the model.

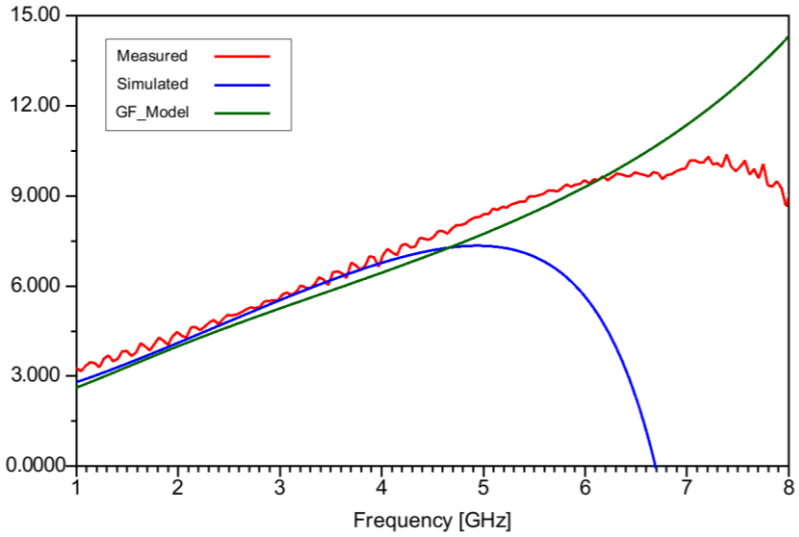

Figure C.5 – Ind2xBFMOAT series resistance

- *Series Inductance*

The series inductance is presented in figure C.6. This result is similar to the obtained with Ind2xM1, where the model presents an accurate low frequency response and the EM simulation an overall better result. The GF model resonant frequency is also greatly different.

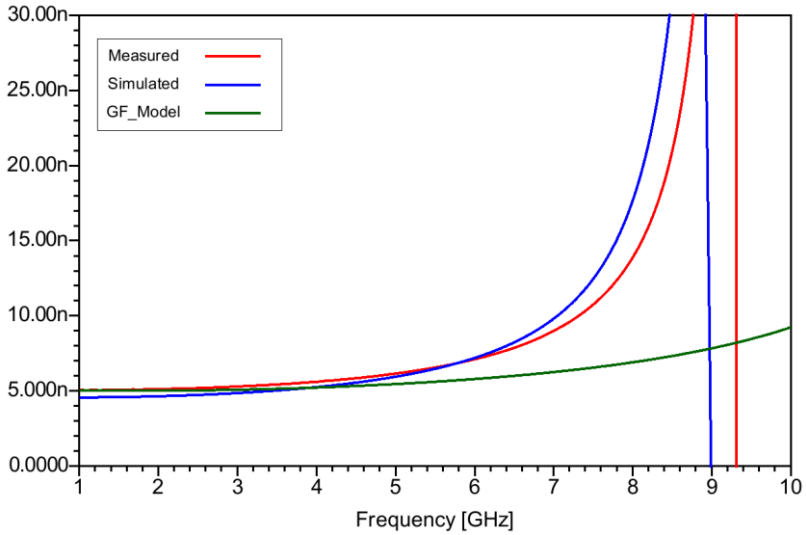

Figure C.6 – Ind2xBFMOAT series inductance

- *Parallel Capacitance*

As mentioned before, the lower frequency is mainly affected by C_{ox}. This can be seen here, as the shield breaks down the parasitic capacitance present at the oxide,

the shunt capacitance for lower frequencies is lower for Ind2xBFMOAT than for Ind2xM1. The parallel capacitance is shown in figure C.7.

The simulation's performance analysis is the same as before, with the electromagnetic simulation displaying a very good accuracy and the GF model with a visible disparity.

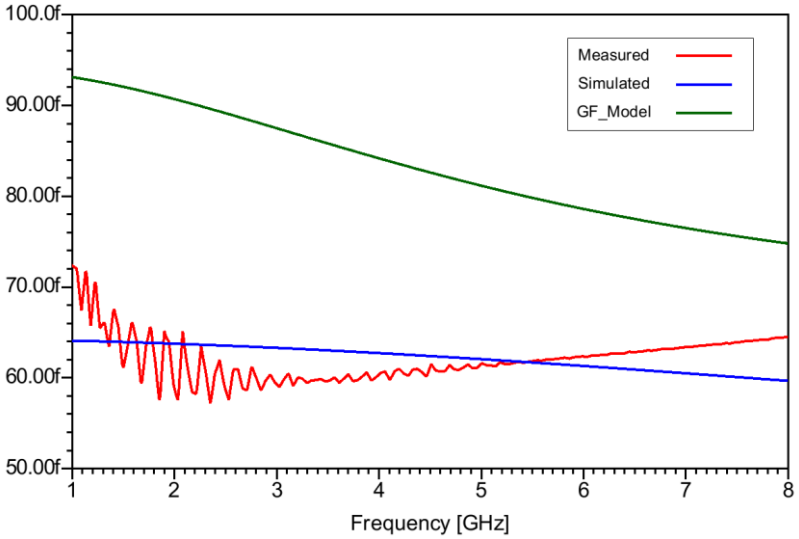

Figure C.7 – Ind2xBFMOAT shunt capacitance

- *Parallel Resistance*

The shunt resistance is shown in figure C.8. This result is practically the same as Ind2xM1's result. This is expected, as the substrate is not altered by adding the shield. The same considerations, directed to the Ind2xM1 shunt resistance, can be repeated here.

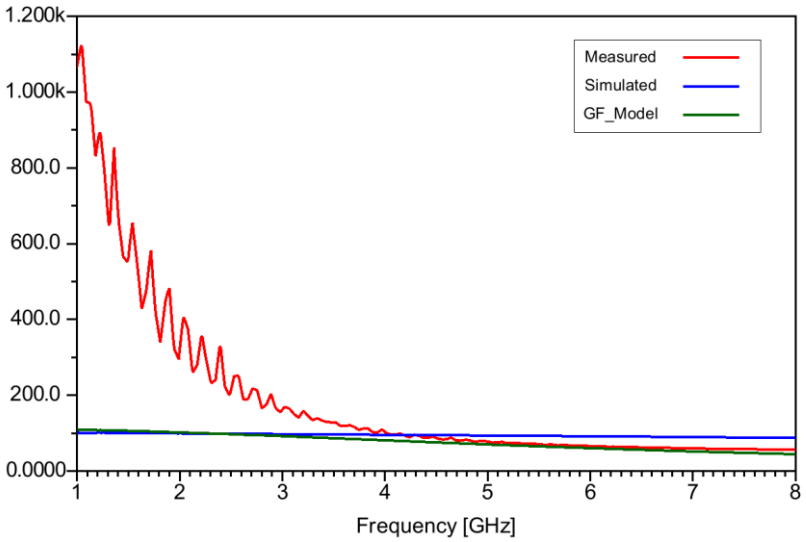

Figure C.8 – Ind2xBFMOAT shunt resistance

Ind1xM1

- *Series Resistance*

The series resistance for IndxM1 is shown in figure C.9, and it is possible to notice the proximity between the measured and simulated data. The simulated data present a smaller series resistance for all the investigated range. As expected, the series resistance is higher than the previous elements. In this case, the difference becomes significant only for higher frequencies.

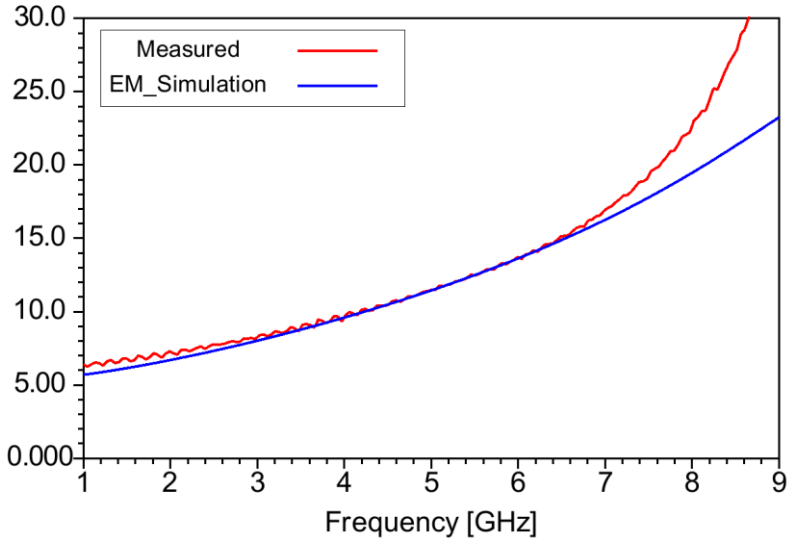

Figure C.9 – Ind1xM1 series resistance

- *Series Inductance*

The series inductance presents the same behavior as the previous analysis, with the simulated low frequency series inductance being lower than the measured. The single-layered data present a modest increase in the series inductance than its double-layered equivalent. The series inductance is represented in figure C.10.

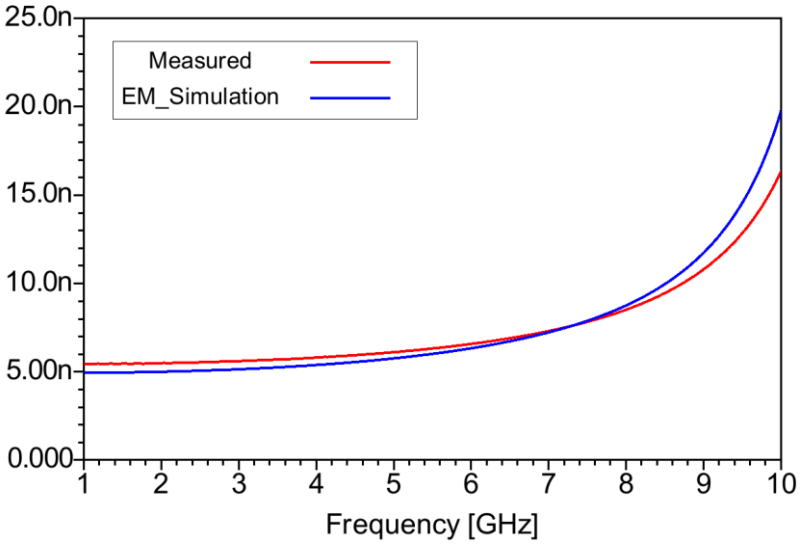

Figure C.10 – Ind1xM1 series inductance

- *Parallel Capacitance*

The shunt capacitance is presented in figure C.11. The same behavior presented in the previous elements is displayed here: an overall accurate representation of the parallel capacitance. As expected, this parameter is lower for the single-layered inductor than for its double-layered counterparts.

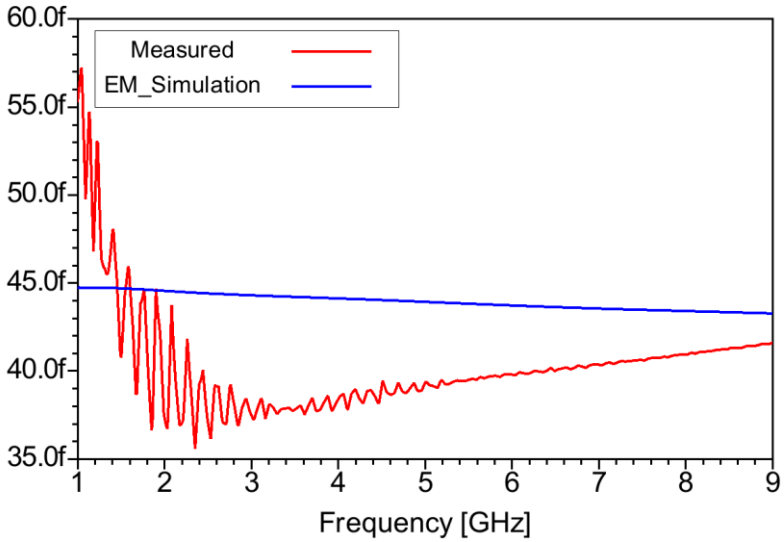

Figure C.11 – Ind1xM1 shunt capacitance

- *Parallel Resistance*

As before, the shunt resistance's low frequency analysis presents a huge discrepancy between the measured and simulated data. This is even more relevant in the single-layered case, in which the parallel resistance effect is enhanced by the addition of an extra oxide (present in the E1 layer). The addition of said oxide to the element skyrocketed the low frequency shunt resistance of the inductor, almost doubling its value, when compared to its double-layered counterparts. The shunt resistance is presented in figure C.12.

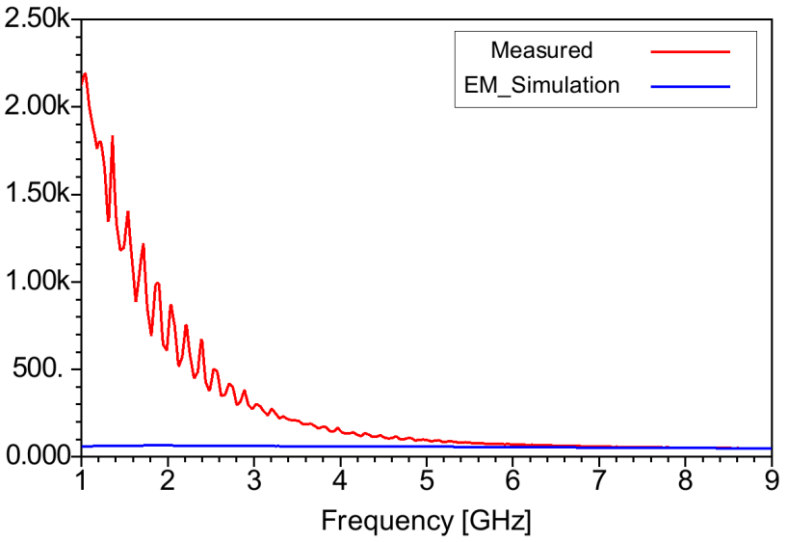

Figure C.12 – Ind1xM1 shunt resistance