UNIVERSIDADE FEDERAL DO PARANÁ

FÁVERO GUILHERME SANTOS

AMPLIFICADOR DE POTÊNCIA CMOS EM 2.4 GHZ COM POTÊNCIA DE SAÍDA PROGRAMÁVEL

CURITIBA

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Dissertação apresentada como requisito parcial à obtenção do grau de Mestre em Engenharia Elétrica, no Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal do Paraná.

Orientador: Prof. Dr. Bernardo Rego Barros de Almeida Leite
Coorientador: Prof. Dr. André Augusto Mariano

CURITIBA

2016

S237a Santos, Fávero Guilherme
Amplificador de potência CMOS em 2.4 Ghz com potência de saída programável / Fávero Guilherme Santos. – Curitiba, 2016.
90 f. : il. color. ; 30 cm.

Dissertação - Universidade Federal do Paraná, Setor de Tecnologia, Programa de Pós-Graduação em Engenharia Elétrica, 2016.

Orientador: Bernardo Rego Barros de Almeida Leite – Co-orientador: André Augusto Mariano.
Bibliografia: p. 89-90.

1. Amplificadores de potência. 2. Sistemas de energia elétrica. I. Universidade Federal do Paraná. II.Leite, Bernardo Rego Barros de Almeida. III. Mariano, André Augusto . IV. Título.

CDD: 621.3815

MINISTÉRIO DA EDUCAÇÃO
UNIVERSIDADE FEDERAL DO PARANÁ
PRÓ-REITORIA DE PESQUISA E PÓS-GRADUAÇÃO
Setor TECNOLOGIA
Programa de Pós-Graduação ENGENHARIA ELÉTRICA

ATA Nº210

ATA DE SESSÃO PÚBLICA DE DEFESA DE MESTRADO PARA A OBTENÇÃO DO GRAU DE MESTRE EM ENGENHARIA ELÉTRICA

No dia doze de Dezembro de dois mil e dezesseis às 16:00 horas, na sala Sala de videoconferências, Setor de Tecnologia, do Setor de TECNOLOGIA da Universidade Federal do Paraná, foram instalados os trabalhos de arguição do mestrando **FAVERO GUILHERME SANTOS** para a Defesa Pública de sua Dissertação intitulada **Amplificador de Potência de Radiofrequência Programável Digitalmente em Tecnologia CMOS 130nm.** A Banca Examinadora, designada pelo Colegiado do Programa de Pós-Graduação em ENGENHARIA ELÉTRICA da Universidade Federal do Paraná, foi constituída pelos seguintes Membros: BERNARDO REGO BARROS DE ALMEIDA LEITE (UFPR), LUIS HENRIQUE ASSUMPÇÃO LOLIS (UFPR), ANTONIO AUGUSTO LISBOA DE SOUZA (UFPB/J.P.), EDUARDO GONÇALVES DE LIMA (UFPR), ANDRÉ AUGUSTO MARIANO (UFPR). Dando início à sessão, a presidência passou a palavra ao discente, para que o mesmo expusesse seu trabalho aos presentes. Em seguida, a presidência passou a palavra a cada um dos Examinadores, para suas respectivas arguições. O aluno respondeu a cada um dos arguidores. A presidência retomou a palavra para suas considerações finais e, depois, solicitou que os presentes e o mestrando deixassem a sala. A Banca Examinadora, então, reuniu-se sigilosamente e, após a discussão de suas avaliações, decidiu-se pela APROVAÇÃO do aluno. O mestrando foi convidado a ingressar novamente na sala, bem como os demais assistentes, após o que a presidência fez a leitura do Parecer da Banca Examinadora. Nada mais havendo a tratar a presidência deu por encerrada a sessão, da qual eu, BERNARDO REGO BARROS DE ALMEIDA LEITE, lavrei a presente ata, que vai assinada por mim e pelos membros da Comissão Examinadora.

Curitiba, 12 de Dezembro de 2016.

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AGRADECIMENTOS

Bernardo Rego Barros de Almeida Leite,
André Augusto Mariano,
Sibilla Batista da Luz França,
Oscar da Costa Gouveia Filho,
Eduardo Gonçalves de Lima,
Luis Henrique Assumpção Lolis,
Edson Leonardo dos Santos,
Magali de Matos,
SBMicro,
MOSIS,
GICS at Universidade Federal do Paraná,
Laboratoire IMS at Université de Bordeaux,
Sonia Aparecida Biscaia Santos,
Fabson Santos,
Talita Keite dos Santos Camargo,
and to all those who inspired me.

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LISTA DE ABREVIATURAS E SIGLAS

MOSIS	-	Metal Oxide Semiconductor Implementation Service
OCP_{1dB}	-	Output-referred 1 dB compression point
P_{DC}	-	DC power
P_{OUT}	-	Output power
P_{IN}	-	Input power
PAE	-	Power Added Efficiency
CMOS	-	Complementary Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
RF	-	Radio frequency
PA	-	Power amplifier
LTE	-	Long term evolution
PVT	-	Process-Voltage-Temperature
CS	-	Common source
CG	-	Common gate

RESUMO

A potência DC (P_{DC}) em um sistema móvel sem fio é um critério determinante de projeto. O amplificador de potência (PA) é um dos subsistemas que mais consome P_{DC}, uma vez que é responsável por amplificar sinais de baixa potência para sinais de alta potência de saída (P_{OUT}). Para que o uso da P_{DC} seja eficiente, o sistema transmissor deve ser capaz de selecionar os níveis de P_{OUT} do PA conforme a necessidade da aplicação, relacionando de maneira ótima P_{DC} e P_{OUT}. Em arquiteturas de PAs nas quais não é possível selecionar a P_{OUT}, o consumo da P_{DC} é aproximadamente constante, independente da P_{OUT} utilizada. Dessa maneira, se a aplicação demanda uma P_{OUT} baixa, a P_{DC} consumida será aproximadamente a mesma que aquela consumida por uma P_{OUT} alta. Ao contrário, em arquiteturas de PAs nas quais a P_{OUT} é selecionável, o consumo da P_{DC} é modulado conforme a demanda da P_{OUT}. Dessa maneira, se é necessária uma P_{OUT} alta, a P_{DC} consumida será proporcionalmente maior. Se a P_{OUT} é baixa, a P_{DC} consumida será proporcionalmente menor. O fato da P_{DC} ser modulada em função da P_{OUT} caracteriza a utilização inteligente da energia disponível em um sistema móvel sem fio.

Essa dissertação de mestrado apresenta o projeto, a implementação e a caracterização de um PA em tecnologia CMOS 130 nm em 2,4 GHz com P_{OUT} selecionável.

O projeto do PA consiste em compreender o que é um PA, qual o seu papel e impacto em um sistema transmissor, onde ele se insere em um sistema transceptor de rádio frequências (RF) e em quais padrões de comunicação sem fio ele se enquadra. Também são demandas de projeto o estudo da tecnologia utilizada (características e ferramentas), CMOS RF8-DM, quais os benefícios e desafios encontrados na microeletrônica de potência em RF, quais arquiteturas atendem aos requisitos de projeto, acompanhar um *tape-out*, e determinar quais são as métricas utilizadas para a caracterização do circuito.

A implementação, por sua vez, consiste em estudar a literatura referente às topologias de PAs com P_{OUT} selecionável, em compreender os blocos construtivos de um PA, em propor a captura de esquemático da solução definida, em realizar o leiaute e simulações do circuito.

Por fim, a caracterização neste trabalho consiste em apresentar os resultados pós-leiaute e medições preliminares; em apresentar a comparação entre os resultados de pós-leiaute e o estado da arte; a comparação entre os resultados pós-*layout* e medições; a análise de variações de processo, tensão e temperatura (PVT) e Monte Carlo do circuito, e a apresentação dos resultados do PA em alguns padrões de comunicação digital.

Diferentemente da literatura estudada, o PA proposto utiliza um estágio de potência composto por três células de amplificação que são ativadas ou desativadas independentemente. Dependendo da combinação em que tais células são ativadas ou desativadas, sete níveis diferentes de P_{OUT} e de P_{DC} são obtidos. Por exemplo: quando todas as células são ativadas, o PA é capaz de entregar a maior faixa de P_{OUT} possível, entretanto, o consumo de P_{DC} é também o maior. De forma contrária, se apenas uma célula for ativada e as demais desativadas, a faixa de P_{OUT} e o consumo de P_{DC} são reduzidos. Dessa maneira, é possível adequar o PA para uma operação com consumo de P_{DC} mínima dependente da P_{OUT} desejada. O circuito proposto possui sete modos de operação unívocos em termos de ganho de pequeno sinal, ponto de compressão

de 1 dB referenciado à potência de saída (OCP_{1dB}) e potência saturada (P_{SAT}). O PA é incondicionalmente estável em todos os modos de operação.

O PA proposto é totalmente integrado, significando que componente externo algum é necessário para o seu funcionamento. Os blocos-núcleo do circuito são: rede de adaptação de impedância de entrada, estágio de ganho, componente de acoplamento interestágios, estágio de potência reconfigurável e rede de adaptação de impedância de saída. Os blocos periféricos do projeto são um *buffer* e um circuito gerador de polarização. O circuito é composto por *pads* para que seja possível aplicar e ler as tensões e sinais de RF. As redes de adaptação de impedância de entrada e de saída são responsáveis por adaptar a impedância de 50 Ω à impedância de entrada do estágio de ganho e a impedância de saída do estágio de potência a 50 Ω, respectivamente. Os estágios de ganho e de potência são responsáveis respectivamente por dar ganho de potência ao sinal RF de entrada e fornecer um sinal de saída com alta potência e baixas distorções. Ambos estágios são baseados em transistores em topologia cascode: a fonte de um transistor em configuração fonte comum (CS) conectada ao dreno de um transistor em configuração porta comum (CG). Em especial no estágio de potência, para se selecionar os diferentes modos de operação, as células cascode de potência devem ser ligadas ou desligadas. Para que as células sejam ligadas, deve-se aplicar a tensão V_{DD} nas portas dos CGs. De forma contrária, para que as células cascode de potência sejam desligadas, deve-se aplicar a tensão *gnd* nas portas dos CGs.

O leiaute do circuito foi realizado considerando a presença de parasitas dos metais, o fluxo e intensidade da corrente RF, o desacoplamento da interferência RF na alimentação e a dispersão de potenciais de terra e de alimentação por todo o circuito. Nenhum erro impactante de fabricação foi encontrado durante o *design rule check* e o layout Vs. schematic e a verificação de modo ortogonal não apresentaram erros. Após o leiaute, as componentes parasitas R e C foram extraídas, o arquivo de fabricação encaminhado para a MOSIS e simulações pós-leiaute foram conduzidas.

A simulação pós-leiaute apresentou os seguintes resultados para o modo de menor potência: P_{SAT} de 8,1 dBm, ganho de 13,5 dB e consumo de P_{DC} de 171 mW para entregar 6 dBm de OCP_{1dB}. O modo de maior potência, por sua vez, apresentou P_{SAT} de 18,9 dBm, ganho de 21,1 dB e P_{DC} de 415 mW para OCP_{1dB} de 18,2 dBm. Em relação à literatura estudada, este trabalho possui a maior faixa de OCP_{1dB} e de P_{SAT}. Em termos de medição, apenas o modo de operação de maior potência foi medido. Ele apresenta um P_{SAT} de 12,6 dBm, OCP_{1dB} de 9,4 dBm, ganho de 12,8 dB e P_{DC} de 252 mW para o OCP_{1dB}. Em termos comparativos, o modo de maior potência medido situou-se entre os modos de menor potência de simulação pós-leiaute. Na tentativa de determinar a fonte da diferença entre o circuito medido e simulado, algumas hipóteses foram testadas, tais como alteração da tensão de polarização do circuito, métodos alternativos para extração de parasitas e influência dos *pads* no descasamento de impedâncias. Os resultados obtidos não foram suficientes para explicar a discrepância encontrada e espera-se que com as medições faltantes seja possível determinar a fonte de diferenças.

Palavras-chave: Amplificador de potências. PA CMOS em 2,4 GHz. Potência de saída selecionável.

ABSTRACT

The DC power consumption (P_{DC}) of a mobile wireless system is a determinant project criterion. The power amplifier (PA) is one of the most P_{DC} consuming subsystem, as it is responsible for amplifying low power signals into high output power (P_{OUT}) signals. In order to use P_{DC} efficiently, the transmitter system must be capable of selecting levels of P_{OUT} according to the amplification demand, optimizing the P_{DC} and P_{OUT} relation. This masters dissertation presents the design, implementation and characterization of a selectable P_{OUT} 2.4 GHz 130 nm CMOS PA. Employing a power stage composed of amplification cells that are independently enabled or disabled, different levels of P_{OUT} and P_{DC} are achieved. The designed amplifier is composed of seven univocal power modes and is fully integrated, meaning that no external components are needed for operation. The characterization of the circuit is composed of small and large-signal continuous-wave metrics, as well as digital channel metrics. The post-layout simulations showed a lowest power mode with a P_{SAT} of 8.1 dBm, gain of 13.5 dB and P_{DC} consumption of 171 mW to deliver an OCP_{1dB} of 6 dBm. The highest power mode performs a P_{SAT} of 18.9 dBm, gain of 21.1 dB and P_{DC} of 415 mW for an 18.2 dBm OCP_{1dB}. The circuit was fabricated and preliminary measurements were conducted. The comparison between measurement and simulation results showed that the fabricated circuit performs bellow expected. Some hypotheses and tests were conducted to determine the difference, but no conclusive results were obtained as further measurements are necessary.

Key-words: Power amplifier. 2.4 GHz CMOS PA. Selectable output power.

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1 INTRODUCTION

1.1. MOTIVATION

A determinant characteristic when selecting a cell phone over another one is its battery lifetime. Depending on battery size, battery lifetime indicates how long a cell phone will last until next recharge cycle. One of the most energy consuming components of a cell phone is in its wireless transmitter circuit, the power amplifier (PA). The PA is responsible for strengthening low power signals and promoting them into high power signals. Those high power signals are transmitted via an antenna.

In order to comply with modern consumer power requirements for mobile devices, the transmitter system must be capable of managing PA power consumption. For example, if transmission is not required, the PA must be turned off, in order to reduce system power consumption. In other cases, when the transmitter and receiver are close by, transmitting high radio-frequency (RF) power is not required. In short-range communication, if excessive power is transmitted, the receiver will likely saturate, and no communication link will be stablished – the energy consumed by the transmitter will be wasted, in this case. On the other hand, if the communication is a long-range link, the PA must transmit high power signals, as these signals are attenuated through space.

This work proposes a PA architecture that can adapt its consumed DC power depending on the aimed output power. Embracing long-range and short-range applications, this PA is capable of reducing its output power when needed for backoff operation. To achieve selectable output power, this transmitter sub-system is composed of independent power cells in the power stage. Those power cells can be activated or deactivated by a combinational cell selector: if higher power is needed, power cells must be activated, on the contrary, if low power is needed, power cells must be deactivated. When deactivating such cells, DC power is reduced, meaning that if lower output power is needed, lower DC power will be consumed. A traditional PA differs from the proposed architecture, as the consumed DC power remains approximately the same independently if the output power is high or low.

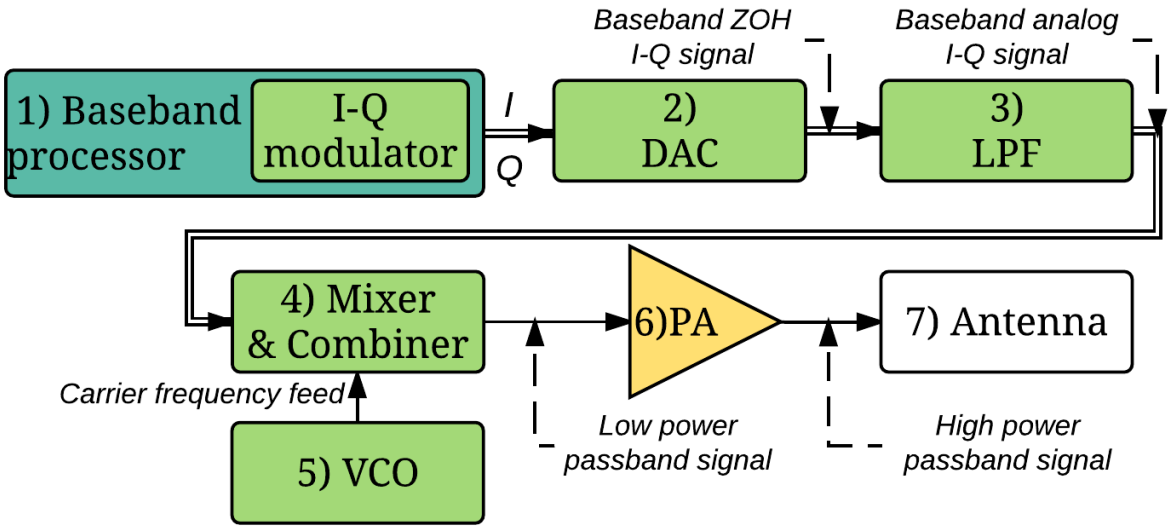
1.2. THE TRANSMITTER POINT OF VIEW IN A WIRELESS COMMUNICATION SYSTEM

An RF transmitter is an electrical sub-system specialized in transmitting high-frequency electrical signals for wireless communication. Its main task is to promote low-power baseband signals into high-power passband signals in a way that the transmitted data may be received on the other side of the communication link. To do so, RF transmitters perform modulation, upconversion and power amplification [1]. These subsystems are found in several commercial products, as integrated circuit (IC) transceivers, as peripherals for microcontrolled systems, or as a transmitter-only ICs.

A common transmitter architecture, known as direct conversion I-Q transmitter, is presented in FIGURE 1. It is composed by seven blocks: 1) baseband processor, 2) digital to analog converter (DAC), 3) low-pass filter (LPF), 4) mixer & combiner, 5) voltage-controlled oscillator (VCO), 6) power amplifier, and 7) antenna.

A baseband signal processor outputs information as separated in-phase (I) and quadrature (Q) bit streams to two DACs. Each DAC converts its input stream into zero-order hold baseband signal. Reconstruction filters smooth these signals. The smoothed I and Q signals are mixed with the carrier frequency (generated by the VCO) and combined into a single, low power I-Q signal. The resulting low power I-Q signal is amplified by the PA and transmitted wirelessly by the antenna [1].

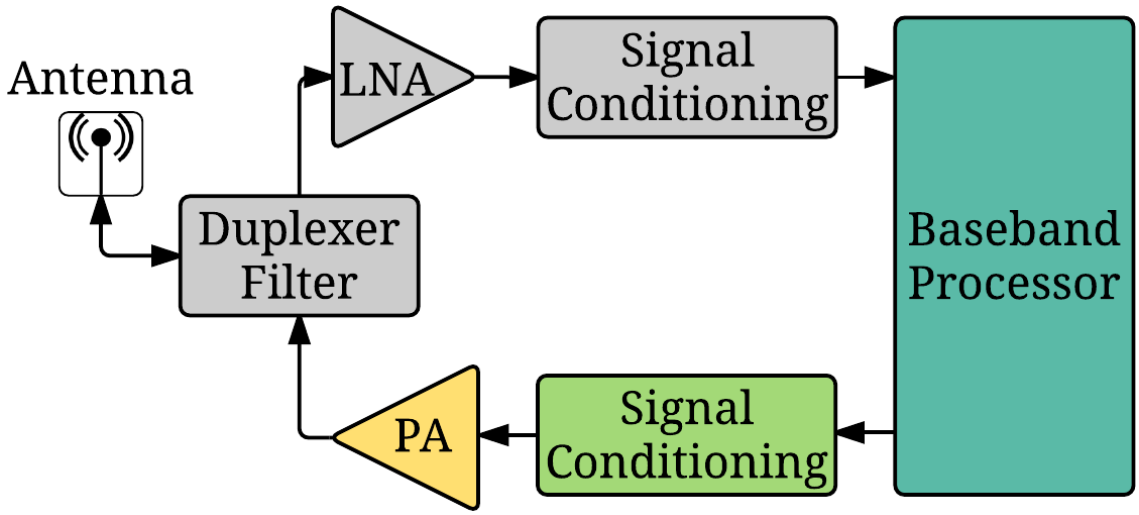
FIGURE 1 – A Direct-conversion I-Q RF transmitter chain and its building blocks.



1.3. THE ROLE AND IMPACT OF THE POWER AMPLIFIER IN A RADIO FREQUENCY TRANSMISSION CHAIN

The PA is the last active component in a wireless transceiver system (FIGURE 2). It handles high current levels and, consequently, has the highest continuous power consumption of the transmitter. An approach to quantify the impact of power consumption of the PA is by dividing the power consumed only by the PA by the power consumed by the whole transmission system. According to [2], while testing Bluetooth standard, the measured impact of power consumption by the PA is between 36.2 % and 44.7 %. In this sense, it is important for the PA to be power efficient, i.e. to be able to transmit high RF power levels without consuming excessive DC power.

FIGURE 2 – A simplified transceiver architecture. The PA is the last active building block in the transmission path. Redrawn from [3].



Being the PA such a large power consumer, high efficiency is expected. This requisite becomes even more relevant as an environmentally aware culture is widely spread. Technical examples of this trend are the 802.15.1 and 802.15.4 standards, issued by IEEE. Those standards aim to provide guidelines to the design, test and regulation of low power, low-cost and battery efficient networks and devices. In order to accomplish this task, IEEE and other standardization groups generally limit the maximum output power levels of the PA and openly promote and encourage solutions that are capable of reducing power consumption when transmission is not required – being the Bluetooth Low Energy standard an exponent of this trend. The power saving effects are, in a general approach, based on symbol effective modula-

tion schemes, short-range networks and simplified data frames. Lastly, modern CMOS fabrication processes also allow greener, low-power and cost effective RF devices. One example of such processes is the GlobalFoundries' 130 nm CMOS, which aims the mobility market segment – where low power and high efficiency are requisites.

Due to the amount of wireless devices in operation, standards are constantly reviewed by interest groups (such as IEEE 802.11 working group), regulatory agencies (as FCC – USA, Anatel – Brazil and ETSI – Europe), and tech users worldwide. Their strict observation aims to better use the limited (and over-populated) frequency spectrum and avoid conflicting and interfering communications. Once more, the PA is a building block that must comply with strict regulations, as standards normally determine (not extensively) a maximum output power, frequency band of operation, and maximum allowable leakage power over other bands. Amongst the unlicensed frequency bands, the 2.4 GHz is one of the most employed in industry, scientific and medical (ISM) applications – a band where microwave ovens, cordless phones, remote controls, wireless routers, and Bluetooth devices operate, each one following its set of communication rules.

1.4. SOME IEEE 802 STANDARDS FOR ISM 2.4 GHZ BAND

IEEE 802 is a family of standards that establish guidelines for wired and wireless networking. Examples of standards included in this family are 802.15.1, 802.15.4, and amendments 802.11n and 802.15.4g – all crafted to operate in the 2.4 GHz band.

Those standards guide on how to properly access the medium when communicating wirelessly. In other words, the medium access (MAC) and physical (PHY) layers are the objects of standardization. This dissertation will focus on PHY requirements, as the object of the study is a PA.

PHY is the lowest layer in the OSI model and is responsible to transmit and receive electrical signals. Some of its responsibilities are bit-to-electrical pulse translation, channel selection and assessment and radio power management. In this way, transmitted power, bit rate and frequency usage are concerns dealt by PHY.

1.4.1. 802.15.1-2005 standard overview

802.15.1-2005 standardizes PHY and MAC for wireless personal area networks (WPANs). This type of network requires little or no infrastructure, allowing small, power-efficient and inexpensive devices to communicate.

Even though this standard defines the original Bluetooth PHY, this discussion will be based on the Bluetooth Low-Energy (BT-LE) PHY. This PHY is standardized in [4] and is built upon the core definitions of 802.15.2-2005, expanding it and providing an even lower power consumption option for wireless networking.

BT-LE operates exclusively on the 2400-2483.5 MHz regulatory frequency range and employs 40 channels with 2 MHz guard. Its modulation scheme is based on GFSK and employs a frequency hopping spread spectrum (FHSS) technique to alternate channels. Some of the radio transmitter definitions are [4]:

- Spectrum emission mask: less than -20 dBm for $|f - f_c| = 2$ MHz and less than -30 dBm for $|f - f_c| \geq 3$ MHz. The definition of spectrum emission mask will be discussed in the section 2.5.3.
- Data symbol rate and definition: up to 1 Msymbols/s, being a binary 1 a positive frequency deviation and a binary 0 a negative frequency deviation.
- Minimum and maximum output power: -20 dBm and 10 dBm, respectively;

1.4.2. 802.15.4-2015 standard overview

802.15.4-2015 standardizes the PHY and MAC layers for devices operating under low-rate wireless personal area networks (LR-WPANs). LR WPANs are simple, low-cost, low-power networks used to convey information to short distances using minimum or no infrastructure. An example of 802.15.4-2015 based network is ZigBee.

Part 15.4 assigns channels depending on the modulation used. For example, for 2450 MHz operation using O-QPSK modulation, the band is divided into 16 channels with 5 MHz of guard. One of the standard PHYs defined is the O-QPSK PHY, which relies on direct sequence spread spectrum (DSSS) technique to switch between channels. Some of the RF transmitter definitions are [5]:

- Spectrum emission mask: less than -30 dBm for $|f - f_c| > 3.5$ MHz;
- Data symbol definition and rate: 62.5 ksymbols/s (or 250 kb/s) with 16-ary quasi orthogonal pseudo-random noise (PN);

- Error vector magnitude (EVM): less than 35 % when measured for 1000 chips (chips are the transmitted constellation symbols by the PA);
- Minimum output power: -3 dBm;

1.4.3. 802.15.4g-2015 standard amendment overview

802.15.4g-2015 is an amendment to 802.15.4 IEEE standard, introducing three new PHYs to support mainly outdoor, low data-rate, wireless smart metering utility networks (SUNs). Focusing on the 2450 MHz band and on O-QPSK PHY, this modulation scheme can access 16 channels with 5 MHz band guard. Some of the radio definitions are [6]:

- EVM: less than 35% when measured for 1000 chips;
- Data symbol rate: 2000 chips/s;
- Minimum output power: -3 dBm. Devices should transmit lower power when possible.

1.4.4. 802.11n-2009 standard amendment overview

802.11n-2009 is an amendment to IEEE 802.11 and standardizes PHY and MAC for wireless local area networks (WLANs) with even higher data rate than that specified by 802.11 by using multiple antennas and doubling the 20 MHz band. Based on OFDM, this high throughput (HT) PHY may operate on modulations such as BPSK, QPSK, 16QAM and 64QAM while operating at 2.4 GHz or 5 GHz. Some of the radio specifications are [7]:

- EVM: less than -5 dB for BPSK, less than -13 dB for QPSK, less than -19 dB for 16QAM and less than -28 dB for 64QAM;
- Adjacent channel rejection: depending on the modulation, varies from -2 dB (64QAM) to 16 dB (BPSK);
- Non-adjacent channel rejection: depending on the modulation, varies from 14 dB (64QAM) to 32 dB (BPSK).

1.5. LONG TERM EVOLUTION (LTE) STANDARD OVERVIEW

LTE is a 3GPP standard that provides higher communication rates for wireless mobile devices while benefiting on the existing GSM/EDGE and UMTS/HSPA cellular infrastructure. LTE employs separate PHYs for downlink and uplink, OFDM

and SC-FDMA, respectively, which may operate over the frequency bandwidth of 700 MHz to 2600 MHz. In this dissertation, the operating band of 2500 MHz will be focused. The channel spacing varies from 1.25 MHz to 20 MHz – the larger the channel, the faster the communication speed – and may be chosen depending on the application and local regulations. Available modulation schemes are QPSK, 16QAM and 64 QAM. Some of the radio specifications are [8]:

- EVM: less than 17.5 % for QPSK, less than 12.5 % for 16QAM and less than 8 % for 64QAM while DUT output power is greater or equal to -40 dBm;
- Maximum output power of 23 dBm;
- Carrier leakage: for $-30 \leq P_{OUT}\,(dBm) \leq 0$, the relative limit should not exceed -25 dBc.

1.6. OBJECTIVES OF THIS WORK

1.6.1. General objective

The general objective of this dissertation is to develop and test a power selectable PA operating at 2.4 GHz employing 130 nm CMOS technology.

1.6.2. Specific objectives

The specific objectives of this dissertation are:

a) To evaluate available techniques for designing programmable power amplifiers operating at 2.4 GHz identifying benefits and challenges and to employ the best suited topology for the intended application;
b) To study GlobalFoundries' 130 nm RF CMOS process technology and components, identifying benefits and challenges;
c) To implement an output power programmable power amplifier operating at 2.4 GHz using the chosen technology having power consumption as a key requirement;
d) To identify the operating limits of the power amplifier;
e) To test with which wireless standards the PA comply;
f) To compare the obtained results with the state of the art;

1.7. DOCUMENT ORGANIZATION

Chapter 2 addresses the CMOS technology for RF PA design. It presents the employed IC fabrication service (MOSIS), benefits and drawbacks of CMOS in RF PA design, two basic CMOS amplifier topologies, details on the employed fabrication technology (GF RF CMOS 130 nm) and lastly the metrics employed to characterize the PA.

Chapter 3 addresses the PA design. It disserts on different techniques to obtain selectable output power, presents a top-down PA design, including layout and post layout processing (parasitic extraction).

Chapter 4 presents the obtained results. A brief discussion on the employed simulations is made, the obtained post-layout, schematic and measurement results are presented. A comparison with the state-of-art circuits and post-layout results is made, as well as a comparison between measured and post-layout results. The results of a Process, Voltage and Temperature (PVT) and Monte Carlo analyses are presented and lastly digital channel simulation results are presented.

2 HIGHLIGHTS OF CMOS TECHNOLOGY AND CIRCUITS

In this chapter, some highlights on the CMOS technology and circuits will be discussed. Firstly, some details will be presented on MOSIS and later on CMOS devices from a PA point of view.

2.1. THE METAL OXIDE SEMICONDUCTOR IMPLEMENTATION SERVICE

Metal Oxide Semiconductor Implementation Service, MOSIS, is a multi-project wafer (MPW) service provider. Its role is to combine multiple IC designs into one wafer mask (known as shared mask) and to subcontract a foundry to manufacture it. As it merges multiple customers' designs (or diverse designs of one costumer) into one mask, the fabrication cost is reduced. MOSIS is especially suited for prototyping, as it allows to debug and test circuits before making large investments. After receiving the fabricated wafer from the foundry, MOSIS is responsible to electrically test, to cut and to deliver the ICs. If desired, IC packaging may be also contracted. If not, MOSIS sends the ICs as loose dies placed inside ESD protected bare die trays, as is presented in FIGURE 3. Apart from MPW service, MOSIS also offers design kits and additional documents for development. Those process design kits (PDKs) are software packages that contain the library files used to develop ICs in a specific technology. Each PDK is foundry specific.

To employ MOSIS tools, one should have a MOSIS account. MOSIS offers four types of accounts: one commercial type and three educational (known as MEP accounts – MOSIS Educational Program) types.

The Group of Integrated Circuits and Systems (GICS) at Universidade Federal do Paraná (UPFR) holds a MEP Research Program account, providing Electrical Engineering students (undergraduates, graduates and researchers) the possibility to have their circuits fabricated. MEP Research Accounts runs are totally founded by MOSIS [9].

FIGURE 3 – ESD protected tray with samples of fabricated ICs in die format. These dies are from 2015 GICS tape-out.

2.2. CMOS PAS: BENEFITS AND CHALLENGES

In the point of view of IC design, several technologies may be employed to design PAs, such as those based on SiGe, GaAs and silicon. Amongst them, silicon-based CMOS benefits from being scalable and widely available at foundries (and, thus, low-cost) while occupying small areas and withstanding high operation speeds [9] [10].

Nonetheless, challenges arise if CMOS power RF design is intended: hot carrier degradation [9], low oxide breakdown voltage, and silicon substrate, impedance transformation and transistor device losses [11]. Besides, due to supply scaling, high currents are necessary to obtain high output power. This leads to higher passive parasitic values, power dissipation issues and efficiency degradation due to high temperatures [2].

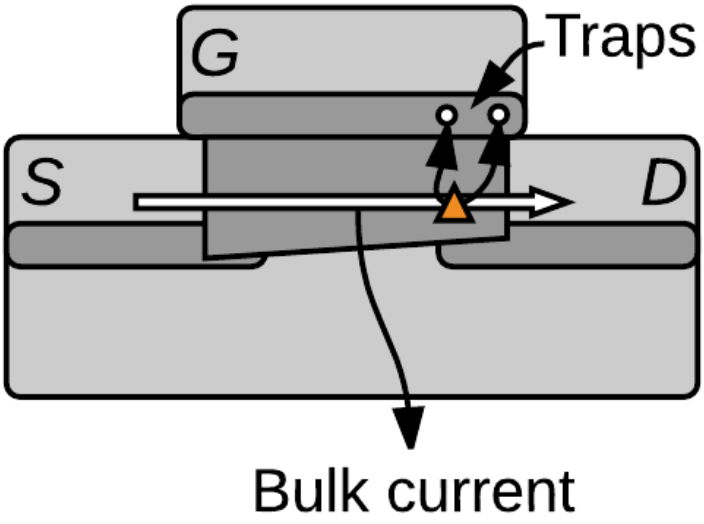
2.2.1. Hot carrier degradation

Hot carrier degradation is the reduction of the conductive capacity of a device's channel due to substrate and gate current leakages (FIGURE 4). Those current leakages are caused by each component of a conductive pair being attracted to the substrate (hole) and gate (electron). The conductive pair is created due to impact ionization when a high kinetic energy charged carrier collides within the gate dielectric. The high kinetic energy is supplied when a high voltage is applied between the drain and source of a MOS device [2], [11]. For the technology employed in this work,

it is pointed in [12] that the maximum potential difference allowed across source-drain during normal regular device operation is 1.6 V.

Due to the reduced conductive capacity, the device's transconductance gain (g_m) is reduced and its threshold voltage (V_{TH}) is increased. A way to prevent hot carrier degradation effect is by avoiding high currents when high drain-source voltage is applied, a scenario in which linear operating PAs are not inserted [2].

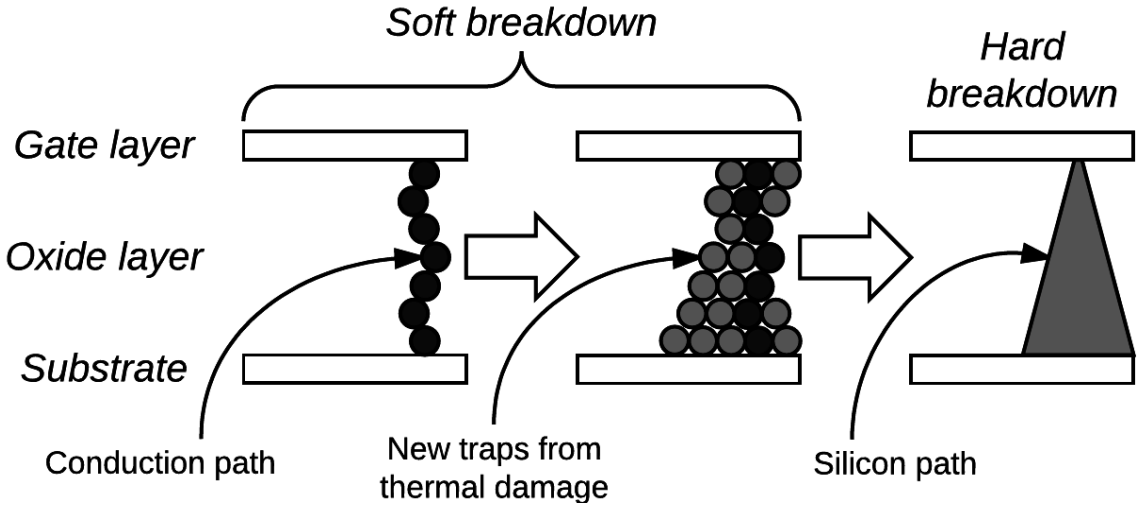
FIGURE 4 – An example on how hot carrier degradation occurs. A high kinetic energy charged carrier collides with the conductive channel of a MOS device. The collision causes the creation of an electron-hole pair. The hole is attracted to the substrate and the electron to the gate, causing leakage currents. Redrawn from [2].



2.2.2. Oxide breakdown

Oxide breakdown is the creation of a conductive path between the channel and the gate of a CMOS device (FIGURE 5). The conductive path occurs when a high voltage is applied across the gate and the substrate of a CMOS device. It is a considerable effect on CMOS devices due to the channel width shortening and the isolation oxide thickness thinning as the technology scales down [2]. The voltage across the device gate should be limited to 1.5 V per nm of gate thickness oxide. This means that if a given transistor has an oxide thickness (t_{OX}) of 1 nm, voltages below or equal to 1.5 V should be applied for reliable long-term operation [11].

FIGURE 5 – An illustration of oxide breakdown effect. If the voltage applied across the gate and the substrate is above the maximum stated rating, defects on the oxide (traps, or simply put, electrons or holes without any mobility) occur. Due to temperature rise, more traps occur in the oxide causing a conductive, but reversible, path (soft breakdown). If the stress is maintained, a silicon path is made between the substrate and the gate. This non-reversible path renders the device unusable as the current leaks thought the damaged area (hard breakdown). Adapted and redrawn from [2].



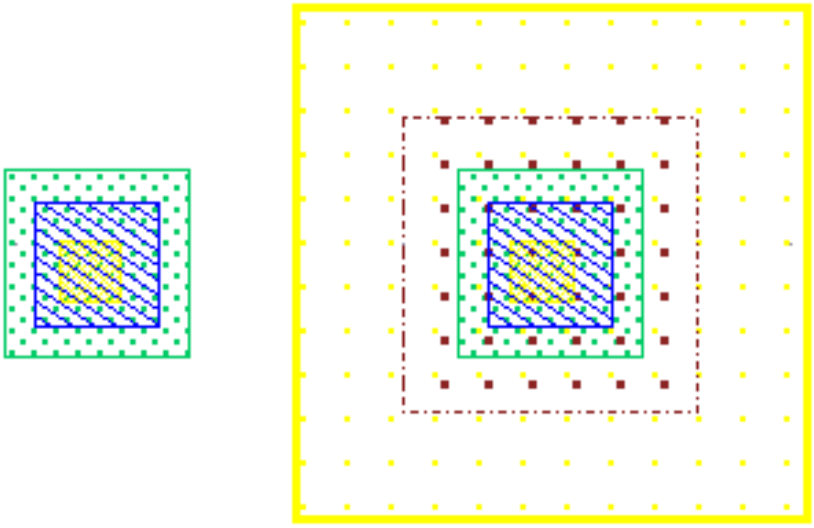
2.2.3. Silicon substrate losses

Being the substrate conductive (approximately 10 Ω-cm) [11] [2], current leaks to the ground may be present. Those leakages affect directly passive and active components, as the substrate potential (frequently used as a reference) is not at the same potential as the ground is. The substrate's potential variations occur on different sections of the circuit, depending on the components activity of that region. An approach to bring the local substrate potential as close to ground potential is by using "tie-downs". Tie-downs are standard cell frames that connect the substrate to ground locally – FIGURE 6 presents an illustration of a tie-down [9] – and thus, distributed ground level over the IC is necessary.

Another undesired effect of substrate current leak is the degradation of the quality factor (Q) of inductive devices. Q is reduced due to the short distance between its constructive metal and the substrate (presence of coupling capacitances).

Lastly, the substrate current leakages may even cause stability degradation as feedback currents may exist between PAs amplifying stages. A way to overcome this challenge is by inserting tie-downs between stages as needed [2].

FIGURE 6 – Examples of tiedowns in CMRF8SF PDK. From the left to the right: nTiedown and pTiedown. The metal 1 (blue block) connects the reference of a component through via CA (small yellow block) to substrate connection RX (green block).



2.2.4. Impedance transformation losses

As the PA is the last active building block of an RF transmission chain, its output impedance must be matched to the input impedance of the antenna. Depending on the output impedance of the PA, the transformation to the characteristic impedance of the antenna requires large passives. Reactive on-chip components such as capacitors and inductors do not behave as ideal components. This is due to the parasitic impedances inherent to its fabrication materials and topologies. By using these non-ideal components as part of the matching network, the aimed matching is not fully obtained, and thus, power is not fully transferred [11].

2.2.5. Transistor losses

As CMOS power transistors are usually large (up to several millimeters), it is common to place the device as a sum of smaller devices, in a grid fashion. In order to do so, fingers width and finger number are altered. Larger width means higher gate resistance, while shorter means higher parasitic capacitance. Considering the finger number, a lower count means lower substrate loss and higher gate resistance [11].

Besides those losses, intrametal connections losses are also representative. This is due to the connection of metals to the gate/source/drain of the transistors. As

they are expected to deal with high currents, any presence of resistance due to intra-connection means unwanted power dissipation [11].

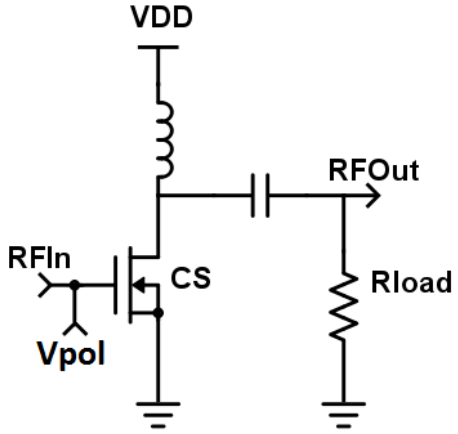
2.3. TWO CMOS AMPLIFIER ARCHITECTURES: COMMON SOURCE AND CASCODE

In the next section, two different amplifier architectures are briefly discussed, common source (CS) and cascode. CS is a single stage amplifier architecture that provides the designer an intuitive topology with some interesting benefits. Cascode, in its turn, is a two stage CS based amplifier architecture that further improves CS qualities and solves some of its drawbacks.

2.3.1. The common source architecture

The CS architecture is based on connecting the source of a MOSFET to the ground potential, its gate to the RF input signal, and its drain to the RF output signal, as presented in FIGURE 7. This architecture benefits from high power gain, high input impedance, ease of design and only one drain current. However, it also experiences narrow input band (due to Miller effect), low isolation, and it is not temperature nor process stable [13]. Another important drawback is that this type of architecture, if used in a series of CS stages, is not easily turned on and off. This is critical to this work, as turning on and off power stages is the core idea of output selectable power for the presented PA. Those drawbacks are overcome by using the cascode topology.

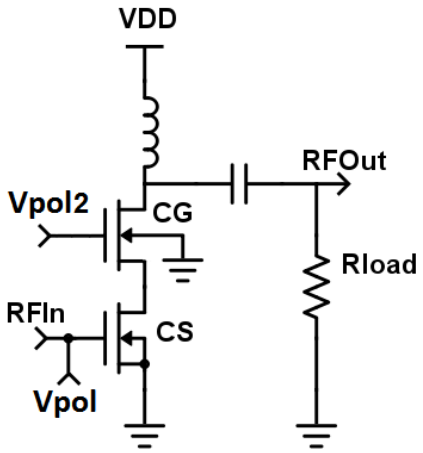
FIGURE 7 – A common source architecture.



2.3.2. The CMOS cascode architecture

A cascode architecture is based on stacking two transistors (FIGURE 8) – connecting the drain of a CS to the source of a common gate (CG). Biasing voltages are applied to the gates of the transistors. This architecture benefits from a high power gain, a better high frequency performance, high stability, ruggedness to low oxide breakdown, ease of design, and presence of only one drain current for both transistors [2]. This structure, however, also has its drawback: as there are now two stacked devices, the voltage drop across the transistors may reduce the range of voltages in which a cascode may operate. This may be an issue if ultra-low voltage is a design requirement.

FIGURE 8 – The cascode architecture. The lower MOSFET is in CS configuration while the higher is in CG configuration. This architecture benefits from high power gain and is rugged to low voltage oxide breakdown.



2.3.2.1. High power gain, better high frequency performance, and high stability

It may seem contradictory to obtain high frequency performance and high power gain simultaneously: to obtain high power gain, high current and high voltage gains are needed; if the voltage gain is too high, Miller capacitance increases and reduces bandwidth.

Cascode architecture solves this riddle as its CS stage has a low voltage gain, but a high current gain and its CG has a high voltage gain but a unitary current gain. This is due to the load impedance of the CS. Being the CG the load to the CS, the impedance load seen by CS is the input impedance of the CG (the input impedance of CG is very low). As the voltage gain of a CS depends on its output impedance, its voltage gain is maintained low. If the voltage gain is maintained low, Miller capacitance is also maintained to a low value [13].

High stability of cascode amplifiers is obtained due to the fact that the output is isolated from the input signal physically: the output is located in the upper transistor drain while the input in the lower transistor gate.

2.3.2.2. Ruggedness to low oxide breakdown, ease of design, and only one drain current

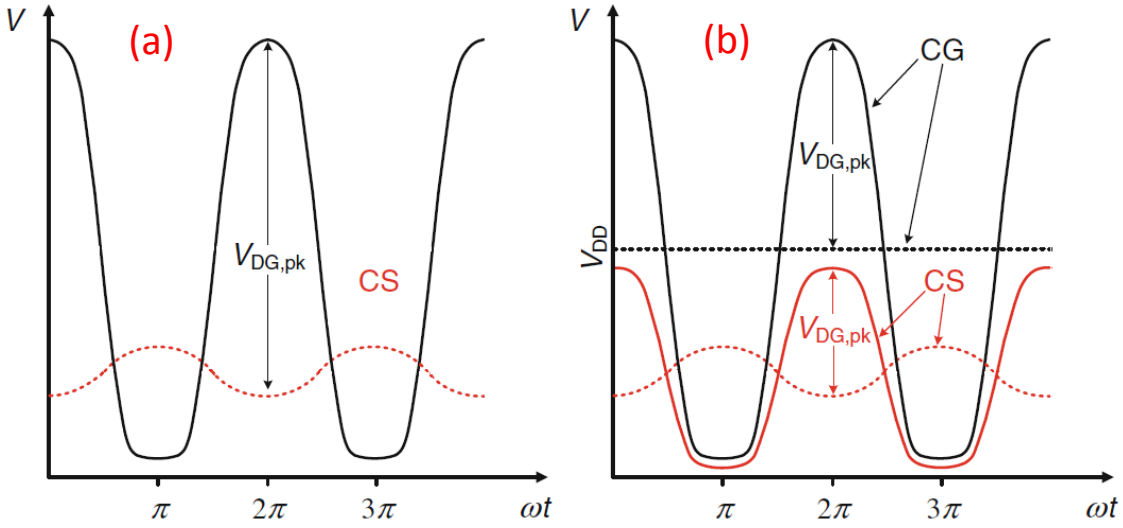
A cascode structure is less lean to experience oxide breakdown than single transistor structures. FIGURE 9 (a) presents the waveform of a typical CS amplifier. The black continuous line represents the drain voltage and the red dashed line the gate voltage. The voltage difference between gate and drain is V_{DG} and it presents a high peak value. Depending on the usage, if this peak voltage is higher than the oxide voltage threshold, the device may be damaged. However, as FIGURE 9 (b) presents, $V_{DG,peak}$ is reduced if the CG is biased with V_{DD}. In a cascode structure, both transistors share the gate stress.

When discussing oxide breakdown on a cascode structure, V_{DG} of the upper transistor is the focus. This voltage is the one subjected to the highest voltage swing of the structure. FIGURE 9 (b) presents waveforms of a conventional cascode structure: the sinusoidal red dashed line represents the sum of the biasing voltage and the input RF signal of the CS, the continuous red line represents the V_{DG} of the CS, the

constant black dashed line represents the gate bias voltage of the CG and the continuous black line represents the V_{DG} of CG.

Concerning ease of design and presence of only one drain current, the cascode structure is easily layoutable, as the CG's source is connected to the CS's drain. If compared to other cascaded transistor structures, such as Doherty amplifiers [13], the cascode output DC current flows through only one path. This current flow alone grants the PA an efficient use of DC current and, consequently, of P_{DC}.

FIGURE 9 – VG (dashed line) and VD (solid line) waveforms of the CS (red line) and CG (black line) transistors of a conventional cascode PA. Adapted from [2].



2.4. GLOBALFOUNDRIES' 130 NM CMOS RF PROCESS

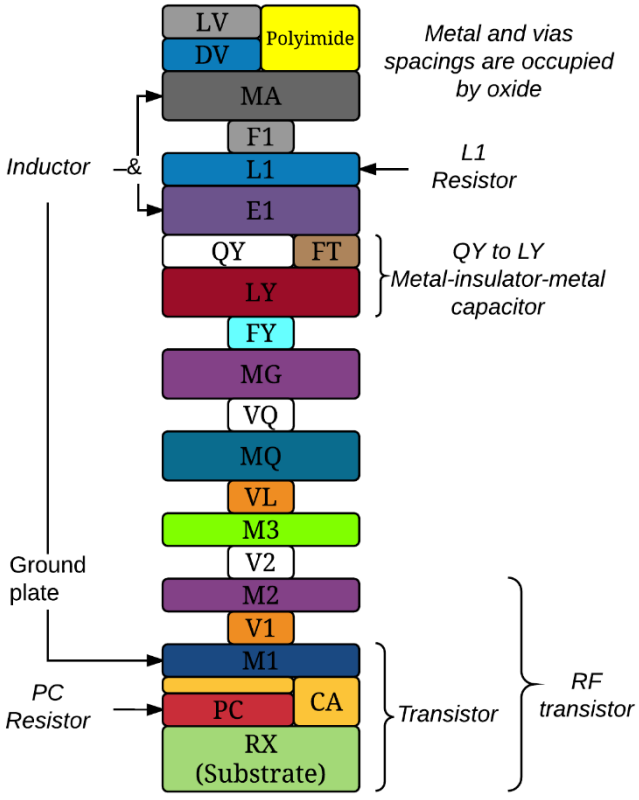
The employed foundry technology was GlobalFoundries' 130 nm CMOS 8RF-DM (former IBM 130 nm CMOS 8RF-DM). This technology is a related technology based on industry standard IBM 130 nm CMOS 8SFG with added passive components and aluminum metal layers (LY and QY are aluminum while L1 is tantalum nitride – others are all copper). The cross section of the back-end of the line of the process is presented in FIGURE 10, where the layer RX is closest to the substrate and polyimide the furthest. CMOS 8RF-DM includes eight metal levels – three thin metals (M1, M2 and M3), two thick metals (MQ and MG) and three thick RF top metals (LY, E1 and MA). All vias are also copper-based, except the tungsten vias FT and FY. DV is used as an opening in the polyimide and LV for bond pads. Final chip passivation is formed by a sequence of oxide, nitride and polyimide films – being the nitride used as anti-ionic contamination barrier and the polyimide as a mechanical

protection. Process' wafer size is 203.2 mm and 760 µm thick (including bumps). One wafer is capable of providing up to 60 dies measuring 18 mm by 20 mm, each one of them 250 µm thick.

Other features of CMOS 8RF-DM are devices isolated by shallow trenches (0.35 µm deep into silicon, nominally); thin oxide FETS (for 1.2 V or 1.5 V operation); n-well, silicided PC and optional metal resistors; series or parallel inductors placed in higher metals and metal-insulator-metal capacitors, achieving 2.05 fF/µm^2 (or even greater, if dual configuration is employed). RF top metals are under 10 mΩ/□ and up to 4 µm of thickness – further reducing parasitics if RF design is intended.

Furthermore, the process possesses its own PDK (CMRF8SF), meaning that devices & passives and their respective libraries are ready to use, electrical and design rules files are set and parasitic extraction is available.

FIGURE 10 – CMOS 8RF-DM cross section (dimensions not to scale) and placement of some components. L1 is an optional layer.



2.5. PA CHARACTERIZATION METRICS

In order to design the proposed PA, different types of analyses were chosen: small and large signal continuous-wave tests and digital channel analysis. Each one of these analysis reports important metrics that assist the development of the PA.

2.5.1. Small-signal metrics

Small-signal metrics can be extracted when small-signal computational analysis or measurements are ran in an electrical circuit. In this way, nonlinear effects such as saturation are masked whereas a simpler mathematical description of the circuit is achieved. This impacts directly on the computational effort to solve the circuit – and that is why small signal metrics are often used when designing and validating a circuit before compromising a computer on a long simulation run. Examples of small signal metrics are the scattering parameters and μ stability factor.

2.5.1.1. Two-port scattering parameters – S parameters

When an amplifier can be represented as a two-port component, with the input at port 1 and the output at port 2, the following scattering (S) parameter matrix can be obtained:

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \text{ (dB)} \quad \textit{(1)},$$

where:

S_{11}: input impedance matching. Indicates how well the input impedance of the port is matched to the reference impedance (usually 50 Ω).

S_{12}: reverse gain or isolation. Indicates the signal isolation from the output port to the input port.

S_{21}: direct gain. Indicates the signal power gain from the input port to the output port.

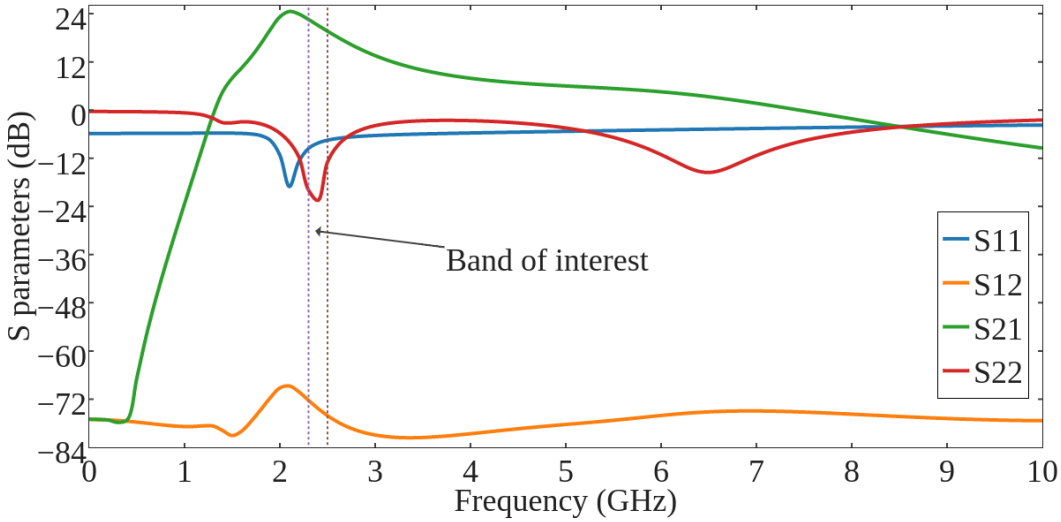
S_{22}: output impedance matching. Indicates how well the output impedance of the port is matched to the reference impedance.

Differently from other characterization matrices that use opens and shorts in its terminations, S parameters use a fixed value (often 50 Ω) for its input and output terminations. This is to simplify the measurement process in a port-modeled circuit.

S parameters are frequency dependent. Being so, these parameters are analyzed over a larger frequency bandwidth than the operation bandwidth (or center frequency), in order to observe the tendency of the circuit when frequency changes, as presented in FIGURE 11. The main design idea, however, is to optimize those parameters around the operating frequency bandwidth (or center frequency). The anal-

ysis of these values indicate how well a certain frequency is transmitted or reflected on the device.

FIGURE 11 – Two port S parameters over a 10 GHz bandwidth. The operating frequency band is much narrower than the measured bandwidth. Those parameters indicate how well a frequency is transmitted or reflected.



2.5.1.2. Two-port output μ stability factor

Stability, in the context of this work, refers to whether the PA operation is oscillator-like or amplifier-like. If the PA behaves as an oscillator, controlled amplification is not achieved, and thus, the designed circuit does not work as expected. Considering a practical description, PA operation regarding stability may be separated into two states: stable or unstable. A stable PA means that the operation as an amplifier is guaranteed over a specified condition – on the other side, being the PA unstable means that the PA operates as an oscillator. Since the stability of a circuit depends on the impedances applied to its input and output, unconditional stability is defined as the condition in which the circuit is stable for any pair of values of source and load passive impedances.

Two-port output μ stability factor rates the stability of a two-port network by evaluating the distance between the center of the Smith chart to the nearest output stability circle. In this sense, as a distance is being measured, the higher the μ, the more stable the two-port device will be. The stability threshold that defines if a system is unconditionally stable is μ equal to one. If μ is lower than one, the system may be unstable for certain source and load impedance values. If μ is greater than one for all

frequencies, the system is unconditionally stable. FIGURE 12 presents μ over a 10 GHz bandwidth. Notice that near DC the two-port device achieves its global minimum value and is nearly unstable. Two-port output μ stability factor is defined as:

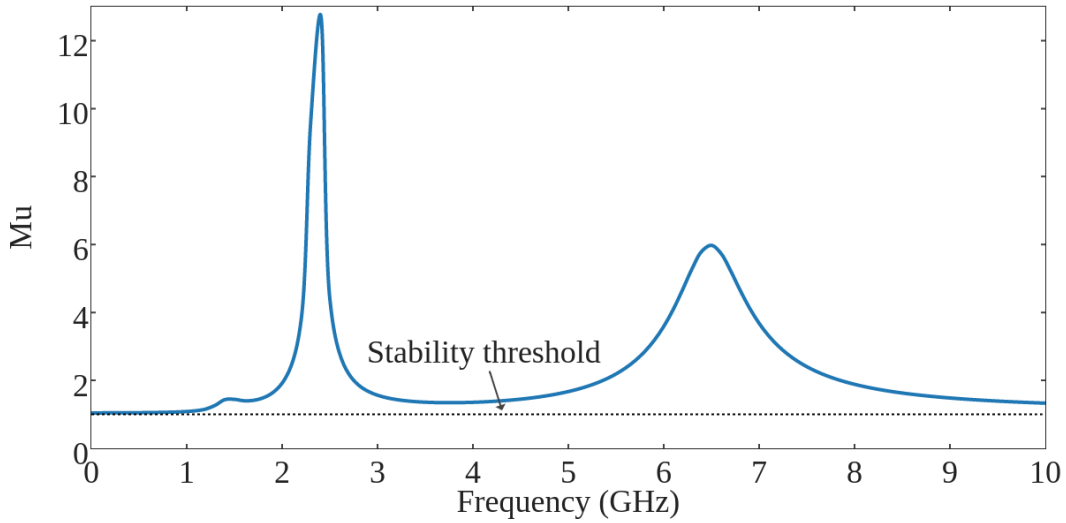
$$\mu = \frac{1-|S_{11}|^2}{|S_{11}^{*}\Delta^{*}S_{22}|+|S_{12}S_{21}|} \quad (2),$$

where:

$\Delta = S_{11}S_{22} - S_{12}S_{21}$ and

S^{*}_{11} the complex conjugate of S_{11}.

FIGURE 12 – Two-port output μ stability factor over a 10 GHz frequency bandwidth. Near DC the device is nearly unstable, reaching its global minimum. If μ is greater than one for all frequencies, the two-port device is unconditionally stable.



2.5.2. Large-signal continuous-wave metrics

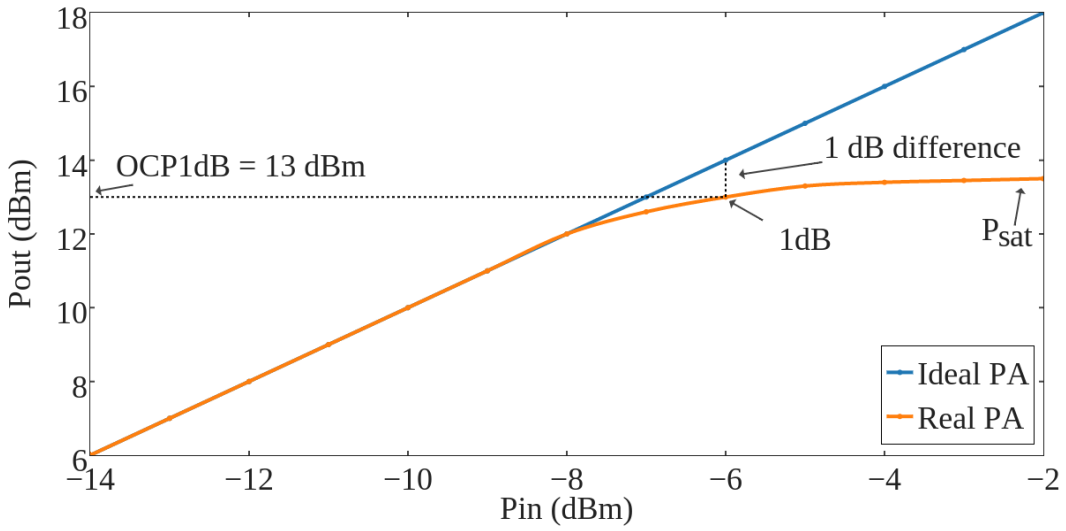
Large-signal metrics, in their turn, are metrics based on large signal circuit analysis or measurement. This analysis accounts non-linear effects of the device, and thus, effects such as saturation are considered. In order to run this type of simulation, the nonlinear device is replaced by its respective model. Those models may be empirical models (models that result from measurements), physical models (models that result from equating the device physics) or both. This analysis is computer demanding, but returns a more accurate view of the device operation. An example of large signal metric is the power performance of a PA (output power vs. input power).

2.5.2.1. Output-referred 1 dB compression point

Before presenting the concept of compression point, a brief illustration will be presented. Consider a perfectly linear PA. For this PA, no matter how large the input power (P_{IN}) is, it will always deliver univocal output power (P_{OUT}) that is proportional to a constant rate (power gain) greater than one. The blue line in FIGURE 13 represents this situation. Real devices, however, have to deal with parasitic impedances, temperature rise and technologic limitations. This means that the PA may operate linearly up to a certain P_{IN}, but not indefinitely. It comes to a limit where even if P_{IN} - increases, P_{OUT} maintains a constant (or nearly constant) value (if the input power increases even further, the device may be damaged). It is said, in this situation, that the PA has saturated. The saturated output power measurement, P_{SAT}, arises from those considerations - P_{SAT} measures the maximum and clipped output power the PA is capable of delivering during non-linear operation. The orange line in FIGURE 13 represents this situation.

The 1 dB compression point (P_{1dB}) is a metric used to evaluate how far a linear PA can be driven before entering saturation. P_{1dB} is the point where the practical power behavior of a PA deflects of 1 dB from the linear power behavior. The output-referred 1 dB compression point (OCP_{1dB}) is where the obtained P_{1dB} is referred to the P_{OUT} scale.

FIGURE 13 – Large signal performance of an ideal (blue line) and real PA (orange line). Output-referred 1 dB compression point is the output power when a real PA deflects 1 dB from the linear operation.



2.5.2.2. Power added efficiency

Power added efficiency (PAE) is a measure of efficiency that accounts the gain of the device. In this way, PAE indicates how much power is added to the input power. By doing so, a fair comparison amongst PAs is provided. PAE is defined as:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (3).$$

2.5.3. Large signal digital channel metrics

When evaluating if a PA complies with global and local communication standards, digital channel metrics are employed. In order to evaluate the PA performance in a digital channel point of view, a modulated signal is applied to the input. This signal must be in accordance with the specified standard, meaning that different standards will have differently modulated and shaped pulses and transmitted power, and the length of data will also be different. By applying different digitally modulated sources and observing the output, it is possible to verify if the proposed architecture complies with different regulations.

Common examples of metrics used to evaluate PA performance under digital channel operation are adjacent channel power ratio (ACPR) and error vector magnitude (EVM). The first one, responsible for off-band spurious emissions must be considered as it affects the quality of signal in surrounding networks. The later one, EVM, measures how accurate the PA is when it transmits modulated signals.

2.5.3.1. Adjacent channel leakage power, adjacent channel leakage ratio or adjacent channel leakage rejection

When a PA is under two tones (or carriers) operation, several other tones, generated due to the nonlinearities of the device, are created. The off-band emissions of most relevance are the third order intermodulation tones (IM3). Those tones have considerable amplitude and their frequencies are close to the frequencies of the two original tones. Depending on the frequency proximity of the two carriers, the third order intermodulation may affect the transmitted message or add undesired power to the adjacent/alternate channels [2] [14] [6].

If the IM3 power added to the adjacent channels is high enough, it may affect the operation of other device's communication [4]. As modern standards use small guard bands (2 MHz for 802.15.1 and 5 MHz for 802.15.4), power leakage meas-

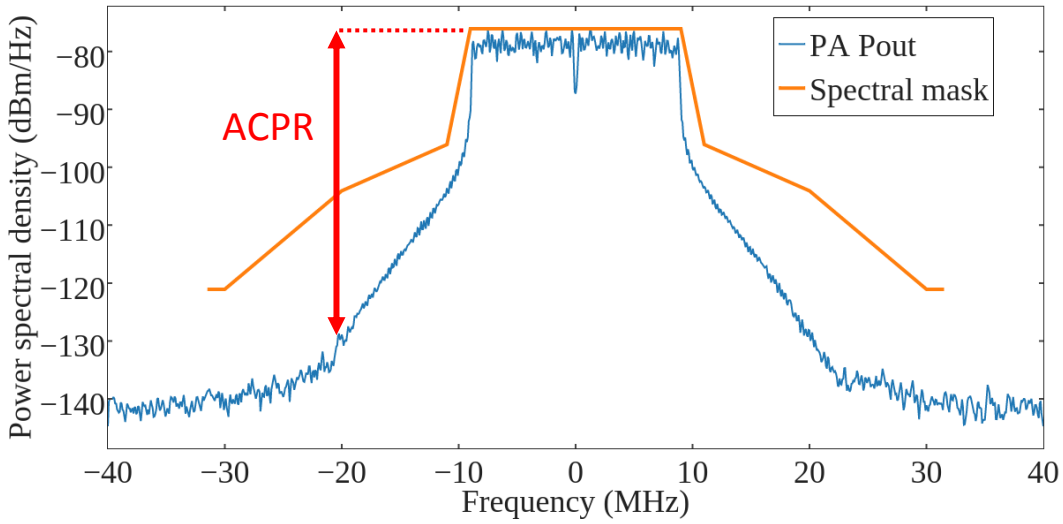
urement is a restrictive transmitter characteristic for both standard and regulation agencies. In this way, measurement definitions such as adjacent channel power (ACP), ACPR and adjacent channel leakage rejection (ACR) are important to ensure harmonic operation among various networks.

Adjacent channel leakage power indicates the absolute acceptable amount of undesired power (in dBm) that leaks to adjacent channels. In BT-LE PHY it is standardized that in a 1 MHz frequency band, no power higher than -20 dBm should be measured in adjacent channels.

When the transmitted power is considered, the amount of undesired power is standardized as a ratio, dBc (decibels to carrier). In such situation, ACPR value is employed. For example, 30 dBc is standardized as ACPR value for 3GPP LTE standard [2]. Lastly, ACR is employed when a receiver must reject a certain power that is interfering in its receiving frequency band. 802.15.4, for example, standardizes 0 dB of rejection in adjacent channels.

Another object of standardization is the power of undesired in-band emissions. Those emissions, in the same way as off-band emissions, are created due to nonlinearities in the PA. In order to ensure proper functionality, the PA must comply with a mask of power levels. This mask is called Spectrum emission mask [2] and an example is presented in FIGURE 14. The objective of the spectrum mask is to provide a graphical representation of maximum allowed transmitted power for in-band and off-band emissions for the standard under test.

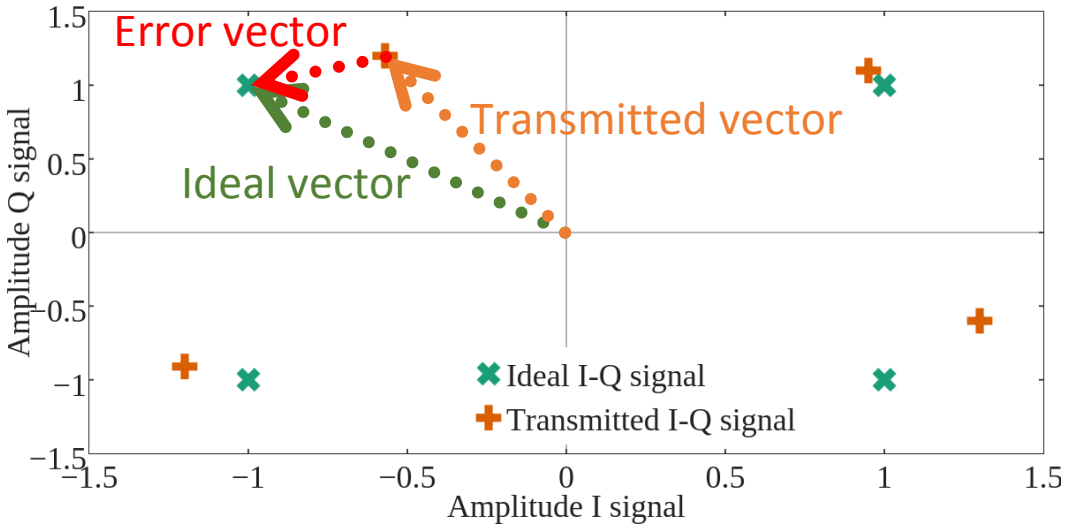
FIGURE 14 – An example of spectrum emission mask for 802.15.4 (orange trace) and ACPR (red trace).



2.5.3.2. Error vector magnitude

When transmitting, the PA introduces distortion to the input signal. This is due to its nonlinear nature. These distortions cause the transmitted constellation to deviate from the ideal constellation, as the markings in FIGURE 15 indicate. As long as the added errors are not significant enough to change drastically the transmitted signal, the transmission will remain a true positive. In order to evaluate the accuracy of the transmitter, the error vector magnitude (EVM) is employed [2]. To do so, in a set of *N* samples, an error vector is considered. This error vector (FIGURE 15, red dotted line) is equal to the distance vector between the ideal constellation point (FIGURE 15, green dotted line) and the transmitted constellation point (FIGURE 15, orange dotted line). EVM is the root mean square value of the error vector for the N samples [2]. Depending on the obtained EVM, it is possible to evaluate if the linearity of the PA must be improved or if its output power reduced (in order to PA operate in a more linear region). As EVM values are object of standardization, its maximum value is normally presented for each standardized modulation scheme. EVM values are stricter as the complexity of the modulation increases.

FIGURE 15 – An illustration of a transmitted constellation and how the error vector is defined. The green, orange and red dotted lines represent the ideal, transmitted and error vectors. If the RMS value is calculated from *N* error vector samples, EVM is obtained.



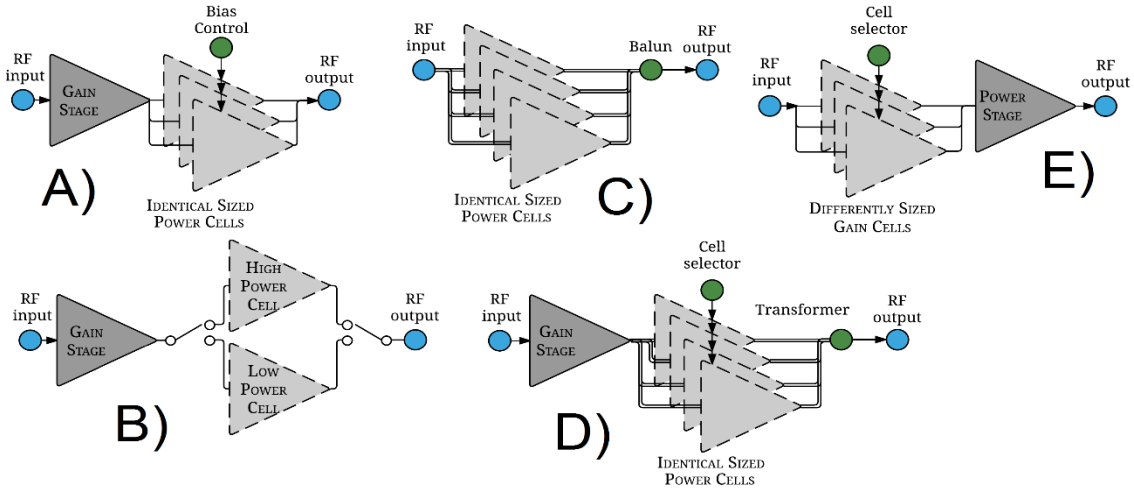
3 POWER AMPLIFIER DESIGN

3.1. DIFFERENT TECHNIQUES TO ACHIEVE SELECTABLE POUT

Distinct attempts on the development of power selectable architecture for CMOS PAs are found in the literature. For example, An *et al.* [15] use a combination of two techniques: gate bias adaptation and identical sized parallel power amplifiers, as presented in FIGURE 16, A). These parallel power amplifiers are activated or de-activated by setting the bias to a certain threshold. For example, if a bias of 0.6 V is applied, only one parallel stage is enabled, and thus, output power is the lowest. If a bias of 0.7 V is applied, all parallel stages are enabled and the output power is the highest. As the bias control affects all parallel stages, this structure cannot enable independently each stage. In their turn, Yoon *et al.* [16] use a control circuit to enable or disable two parallel cascode power stages: a low power stage and a high power stage, as is show FIGURE 16, B). These parallel stages are enabled by applying high voltage to the CG in the cascode structure, enabling the CS to operate. This PA is dual mode only, meaning that the combination of low power mode + high power mode is not feasible. In [17], Raeynaert *et al.* propose the implementation of a control circuit to switch on and off four independent identical differential amplifiers which are balun coupled to a common load, as depicted in FIGURE 16, C). By activating and deactivating each one of the differential amplifiers, selectable P_{OUT} is achieved. Lastly, Tuffery *et al.* [18] propose using four parallel power cells that can be independently enabled or disabled to achieve selectable power, as presented in FIGURE 16, D). These power cells are identical and are all coupled to the load by using a transformer. By enabling all power cells, P_{OUT} is the highest. By enabling only one, P_{OUT} is the lowest. As these cells are identical, enabling cell “A” and “B” has the same power effect of enabling cell “C” and “D”.

Apart from power control, Santos *et al.* [19] implemented a control circuit to enable or disable differently sized transistors in the gain stage using cascode structures to obtain selectable efficiency levels, as shown in FIGURE 16, E). This structure showed itself promising, as differently sized transistors are used, gain stages can be enabled or disabled independently and load coupling was done via an output matching network.

FIGURE 16 – An illustration of distinct attempts on obtaining selectable output power. A), designed by An *et al.* [15], B) designed by Yoon *et al.* [16], C) designed by Raeynaert *et al.* [17], D) designed by Tuffery *et al.* [18] and E) designed by Santos *et al.* [19].

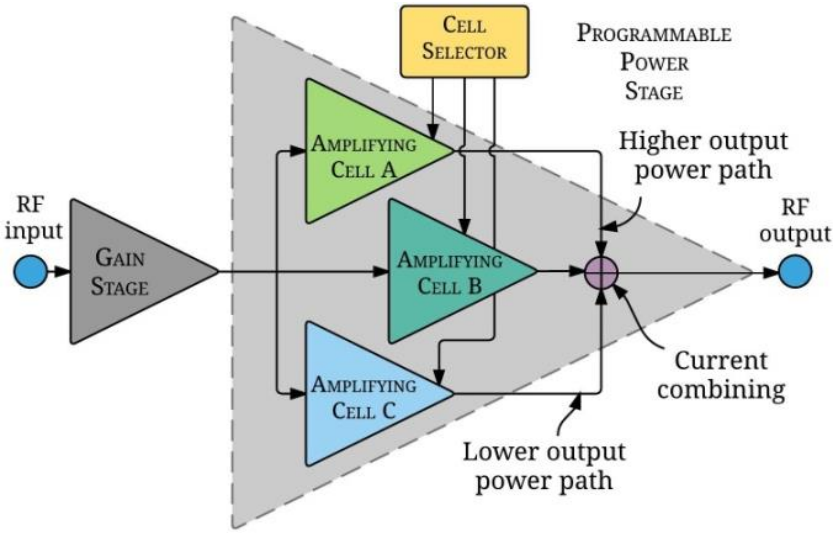


3.2. CIRCUIT DESIGN

3.2.1. An output power selectable architecture PA

Based on the studied literature, a two-stage PA composed of a fixed gain stage and a programmable power stage is proposed in this dissertation (FIGURE 17). The programmable power stage is composed of a set of amplifying cells and a cell selector. The cell selector is responsible to switch on or off each one of the amplifying cells, delivering, in this way, selectable P_{OUT}.

FIGURE 17 – Proposed topology for enabling or disabling differently dimensioned amplifying cells. If a certain P_{OUT} is achievable by each cell individually, solely C will be enabled, as it consumes less P_{DC}. From [20].



A feasible way to achieve this design is by parallelizing cascode power cells with different widths. The cascode structure is used as its CG can be easily used as a way to switch on and off the amplification. In this way, the cell selector is the CG transistors being enabled or disabled, while the amplifying cells are the cascode structure.

In order to deliver different power levels, the amplifying cells are sized differently. This is because the transconductance of a MOSFET depends directly on its gate width. In this way, transistors with greater widths achieve higher output power levels.

3.2.2. Project requirements

The project requirements were based on wireless standards requirements, previous experiences on PA design and on consumer electronics requirements. In some aspects, those requirements were adapted, in order to better address the object of study. For example, the output power and univocal operating modes are guidelines from the standard 802.15.1-2005, which states that the output power must comply with a maximum of 20 dBm and a minimum of 0 dBm for a power class 1 device. The power steps must be a monotonic sequence with maximum 8 dB step size and minimum 2 dB step size. The operating frequency of 2.4 GHz was chosen due to this frequency being located inside the ISM band. The supply voltage is a common design requirement and the temperature voltage was based on the consumer electronics range of 0 ºC to 85 ºC, with an offset of 40 ºC, due to the temperature rise of the PA operation. The project requirements are presented in TABLE 1.

TABLE 1 – Summary of the project requirements for the CMOS PA.

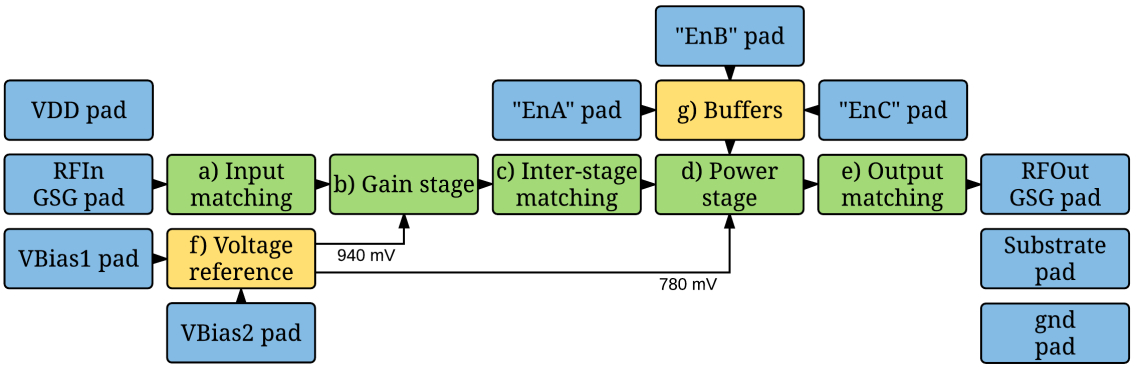
Requirements description	***All***	***Highest power mode***
Number of univocal operating modes	7	
Input matching	to 50 Ω	
Output matching		to 50 Ω
P_{SAT} (dBm)		20
Operating frequency (GHz)	2.4	
Working temperature range	from 40 °C to 125 °C	
P_{DC} (mW)		≤ 500

3.2.3. Top level view of the proposed PA

As presented in FIGURE 18, the top view of the PA is composed of three different color-coded layers – blue, yellow and green. The blue layer is composed of the interface pads, such as supply, ground & substrate connection and RF input & output pads. The yellow layer represents auxiliary circuits, such as logic buffers (for power selecting) and an on-chip biasing voltage generator. Finally, the green layer represents the core circuit of the PA, such as gain and power stages.

The supply voltage and references for ground and substrate are set in the blue layer. In the proposed work, V_{DD} is set to 1.8 V and substrate & ground pads must be tied to the global ground reference. V_{Bias1} and V_{Bias2} are also set to 1.8 V. “EnA”, “EnB” and “EnC” are logic inputs and, thus, V_{DD} or ground voltage should be applied to those pads. By selecting a different logic combination in those pads, the operating power mode of the PA is chosen.

FIGURE 18 – Top view of the proposed PA. It is composed of three color-coded layers: blue for the pads, yellow for auxiliary circuits and green for core PA circuits. The core is composed of five blocks - a) through e).



The yellow layer, although not strictly required for the project, is employed to guarantee the proper operation of the PA. For example, all logic inputs are buffered by the buffer block (g), which ensures logic high and low levels for the core circuit. The voltage reference circuits for biasing – block (f) – sets the proper biasing voltage (940 mV and 780 mV) for the gain and power stages as long as 1.8 V is set in its pads.

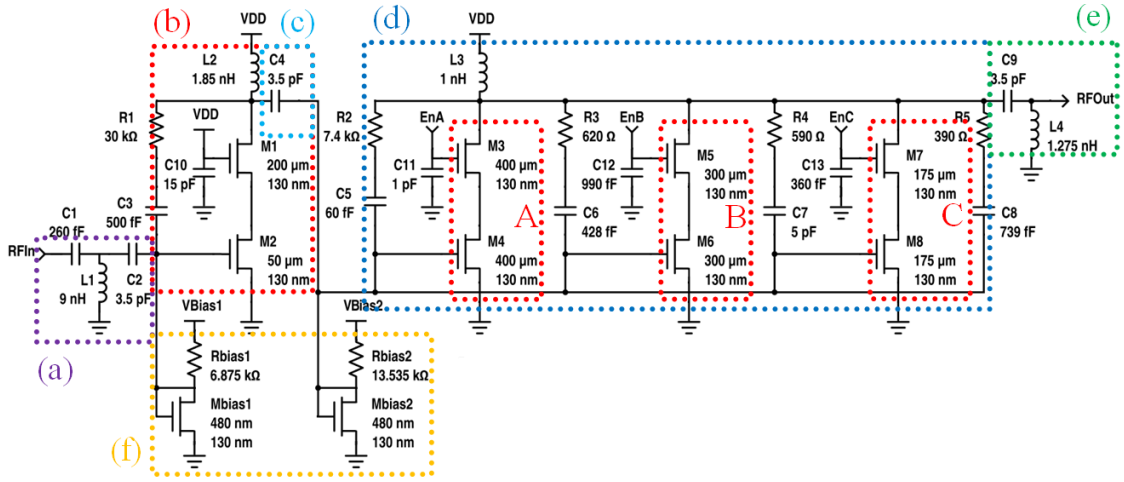
Finally, the green layer is composed of input impedance matching network (a), gain stage (b), inter-stage impedance matching and coupling (c), programmable power stage (d) and output impedance matching network (e).

The top view operation of the PA is as follows: RF low power signal is set in the RF_{IN} GSG pad. The source impedance is matched from 50 Ω to the gain stage impedance via block a). The signal is amplified by block b). The high amplitude signal is then fed into block d) via block c), which matches block b) output impedance to block d) input impedance. The signal is amplified by block d). The high power signal impedance is matched to 50 Ω by block e). Finally, the amplified signal is available in the RF_{OUT} GSG pad.

3.2.4. Schematic of the proposed PA

In this section, the bottom level view of the proposed work will be presented. Each labelled block in FIGURE 18 is now detailed and the component level is presented in FIGURE 19.

FIGURE 19 – Schematic of the proposed PA. It is composed of: (a) input matching network, (b) gain stage, (c) inter-stage matching and coupling passive, (d) power stage, (e) output matching network and (f) voltage reference for bias. The amplifying cells are represented by A, B and C. From [20].



Block a), the input matching network, is composed of a “T” high pass filter (C1, L1 and C2) and was designed to provide conjugate match between the gain stage’s input impedance and 50 Ω signal source signal impedance.

The gain stage, or block b), consists of a cascode gain amplifier (M1 and M2), a choke inductor (L2) and an RC feedback circuit (R1 and C3). The cascode structure works as a voltage amplifier, adding gain to the input signal. The RC network is employed to guarantee stability. To couple gain and power stages, block c), the inter-stage matching component C4 was placed.

Block d), the power stage consists of three cascode power amplifiers cells (M3 through M8), a choke inductor (L3), four RC feedback circuits (R2 through R5 and C5 through C8) and three capacitors to further improve stability at 2.4 GHz (C11 through C13).

The power cascodes are implemented in three cells: “A” presents the transistors with the largest widths (400 µm), “B” presents intermediate widths (300 µm) and “C” presents the smallest widths (175 µm). Those structures are enabled by applying a high logic level on the gate of the upper cascode transistor. Thus, one can enable only “B” by applying high logic to “EnB” and low logic to “EnA” and “EnC”. Consequently, the resulting output power delivered to the load is driven only by “B”. TABLE 2 shows the possible operating modes for the proposed architecture.

The output matching network, block e), is composed by an LC high pass filter. Along with L3 inductor, C9 and L4 are responsible for power matching.

In order to correctly bias the gain and power stage cascodes, two voltage reference circuits were designed. They are composed by transistors Mbias1 and Mbias2 and resistors Rbias1 and Rbias2. When applying 1.8 V into the biasing pads, the proper reference voltages are generated for the gain and power stage.

TABLE 2 – Gate widths of power cascodes and designation of operating modes. From [20].

Mode (ABC)	***W_{total} (µm)***	***Observation***
001	175	Lowest power level
010	300	
100	400	
011	300 + 175 = 475	Intermediate power levels
101	400 + 175 = 575	
110	400 + 300 = 700	
111	400 + 300 + 175 = 875	Highest power level

3.2.5. Cell level view of the employed devices

CMRF8SF provides the designer a set of fabrication options – indp and inds, for example. Those two components are both inductors, but they differ in their structural construction: indp is an inductor that uses parallel metals to achieve specified inductance while inds uses serial metallization. This affects the resulting parasitics, inductor size and inductance range of values. Depending on the objective, those trade-offs must be considered. The same happens with other components, such as

capacitors, resistors and MOSFETs. In this section, those differences will be considered and an explanation on which type of component that was used will be presented.

The MOSFET devices employed throughout the core blocks of the PA are the “lvtnfet_rf” cell. This cell features lower threshold voltage than the regular nfet structure. The lower threshold voltage provides a higher on-current at expense of a higher leakage current (compared to the regular nfet). The suffix “_rf” in this cell stands for a controlled RF layout geometry, which possesses pre-determined parasitic values and, thus, provides the most accurate simulation of electrical behavior. The MOSFETs for the voltage references are standard nfet cells.

The passive components cells employed throughout the project were “mimcap_inh”, “indp_inh” and “oprppres_inh” for the capacitor, inductor and resistor, respectively. “mimcap_inh” is a single insulated layer aluminum capacitor, specific for the DM option. “indp_inh”, in its turn, is an inductor cell that employs parallel metals to achieve the specified inductance. The advantages of using such a cell is that it occupies less space than a series inductor (for the same inductance) and has the lowest series resistance (amongst available inductor cells). The drawback of this cell is the higher turn-to-turn capacitance, if compared to the standard inductor cell. Finally, “oprppres_inh” is an optional precision polysilicon resistor that features the lowest tolerance (amongst available resistor cells) at cost of a relatively large area. As for the prefix “_inh”, it stands for an implicit schematic representation (there is no additional pin for substrate connection), simplifying schematic capture. The designer, however, must pay attention on the fact that the backplate of each component must be connected to the proper reference during layout.

During layout phase, the error “ESD01” was generated for inputs and outputs pins during design rule check. This error verifies if ESD protection devices are placed in ESD susceptible pins. In order to correct it, additional ESD protection diodes were added to the schematic and to the layout. These diodes were “dipdnw” cells – standard forward bias diodes [12].

3.2.6. Process to determine the adequate transistor widths

After setting the aimed topology for the PA, transistor widths must be chosen. This decision is crucial to the design, as the transistor must be dimensioned to deliver the aimed output power while consuming the least P_{DC} - this means that under-

dimensioning a transistor results in not meeting the power requirement while over-dimensioning it results in an unnecessary wider area and power consumption. There are at least four processes of dimensioning a MOSFET: experience-based, experimentally based, analytical determination, and optimization based.

The first process is based on the designer's experience on the employed technology – considering the aimed output power and supply voltage, the designer knows, to a certain extent, the approximate transistor width for the application. By using this first approximation, it is possible to fine-tune the transistor width for the application. The drawback of this process is the dependency of a very experienced professional and a consequent optimization step.

The second one, experimental based, dismisses the need of an experienced professional at the cost of manually setting design parameters to achieve the proper transistor width. The drawback of this process is that several simulation steps are required; each one of those depending on the last simulation result, as the designer incrementally alters the circuit to meet the requirements. This process is excessively time and effort consuming.

The analytical process is based on the device model's analytical equations to determine the transistor width. Even though this process may be the most assertive and optimal, model equations of the technology are not always available & simple to use and some process variables are not promptly available to the designer (meaning that prior simulation steps to determine some constant values are required).

The last one, optimization based, relies on using the computational power to determine transistor width. It is based on setting targets to the simulator (such as maximum OCP_{1dB}, maximum gain, etc.) and degrees of freedom. Those degrees of freedom are, for example, the transistor width, number of fingers and multiplicity and the range values they can vary. The simulator, then, runs until all the requirements are met or the best scenario achieved.

Further details should be considered when determining the adequate transistor width: output matching affects on achievable output power for a fixed transistor width, only a set of finger numbers or widths are feasible due to certain design rules and stability must also be considered.

In this work, the optimization method was chosen. A test bench was prepared and optimization simulation ran to determine the transistor width. This is done in ADE GXL by setting the simulation method to "Local optimization" (field a) in FIGURE 20)

and setting targets and degrees of freedom. Specifications are set by locking simulation “spec” field with the aimed project requirements (field b) in FIGURE 20 while the degrees of freedom are set by parameterizing the schematic (FIGURE 21) and setting the range of variation in the “global variables” box (field c) in FIGURE 20. The power characteristics for different widths transistors in a cascode topology are presented in TABLE 3. For a step of 200 µm (comparing 150 µm to 200 µm) the OCP_{1dB} (in the latter case) is increased by 2.61 dB, P_{SAT} by 2.53 dB, PAE at OCP_{1dB} by 1.75 percentage points and P_{DC} at OCP_{1dB} by 21.41 mW.

FIGURE 20 – Example of optimization set-up in ADE GXL. Detail a) shows were optimization as simulation method should be chosen, b) shows target values and c) shows example of parameterized transistor widths and their range of values to be altered during simulation.

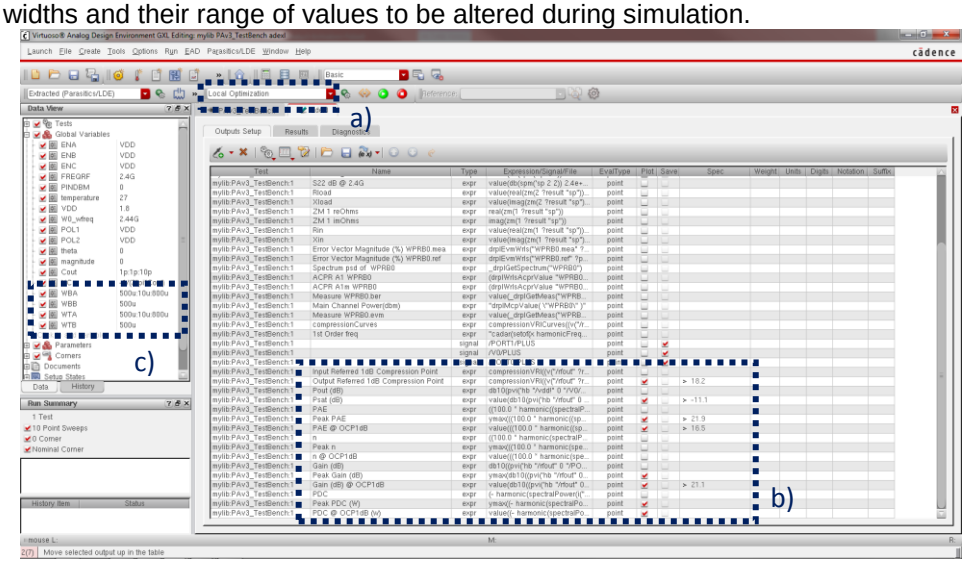


FIGURE 21 – Example of parameterized schematic. The figure presents a cascode topology. Settings of the highlighted upper transistor are shown in the object properties box. Note that the field “Width all fingers” is set with the value “WTA”, an example of parameterization for optimization simulation.

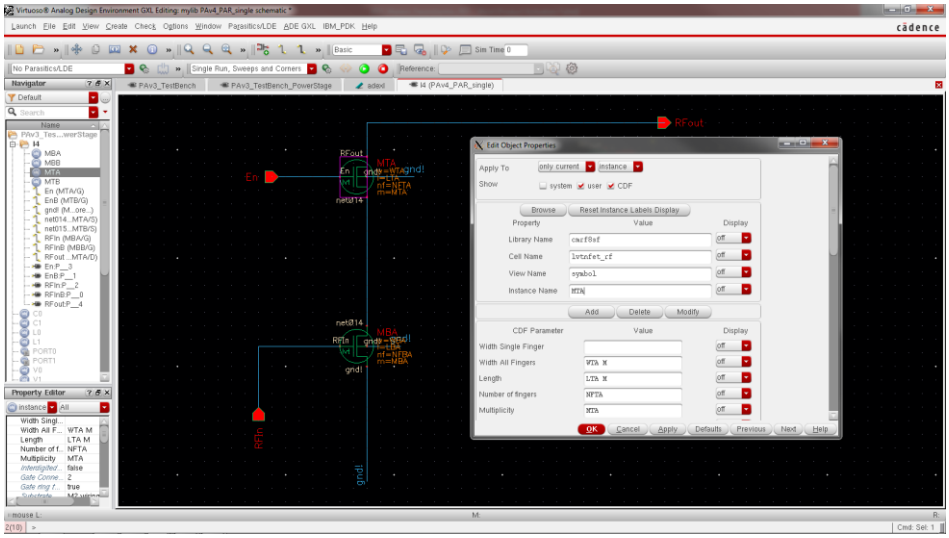


TABLE 3 – Example of width impact in a power amplifier design. The first row shows the obtained results for a 150 µm gate width transistor, the second column for a 175 µm transistor and the third for a 200 µm transistor. All transistors are biased by the same voltage; the input is matched to 50 Ω; the gain stage is the same for all tests; the output is matched to 50 Ω. The presented results are schematic only, and thus, perform better than parasitic extracted circuit.

Transistor width (µm)	***150***	***175***	***200***
OCP_{1dB} (dBm)	5.0	6. 7	7.6
P_{SAT} (dBm)	5.5	6.7	8.0
Peak PAE (%)	4.8	6.0	7.2
PAE @ $OC1P_{dB}$ (%)	3.4	4.2	5.1
Peak small signal gain (dB)	19.9	21.1	22.0
Peak P_{DC} (mW)	96.3	107.0	117.7
P_{DC} @ OCP_{1dB} (mW)	91.7	101.0	110.8

3.2.7. Process to determine power cells width

After determining the width capable of achieving the highest power mode requirements (875 µm), the device was divided into three separate cells, each one containing its own width. In order to obtain selectable power, different distributions of widths were tested. This design step is critical, as univocal power modes (and some low power mode characteristics) are a project requisite. Those cells were firstly dimensioned in a $1{:}\frac{1}{2}{:}\frac{1}{4}$ fashion, meaning that the widest cell width measured is 500 µm, the intermediate measuring 250 µm and the shortest 125 µm (computing 875 µm). When experimentally testing this first approach, power modes were not evenly distributed across available selectable powers. This fashion was experimentally modified until an even distribution and no overlapping power modes were observed, as shown in TABLE 4.

TABLE 4 – Example of width distribution impact. The results of a 1:1/2:1/4 fashion is presented. All modes are univocal, but power distribution is not approximately even among all modes – from mode "001" to mode "010" the $OCP1_{dB}$ varies more than 6 dB while from power mode "110" to "111" the variation is only 0.92 dB. The final fashion obtained spreads the possible power over all selectable modes. All modes are biased by the same voltage and the gain and output matching stages are the same in all sets. This is a schematic only simulation, and thus, perform better than parasitic extracted circuit.

Power mode	***001***	***010***	***011***	***100***	***101***	***110***	***111***
Total transistor width (µm)	***125***	***250***	***375***	***500***	***625***	***750***	***875***
OCP_{1dB} (dBm)	3.3	9.8	13.3	15.0	16.6	18.1	19.1
P_{SAT} (dBm)	3.8	10.6	13.7	14.6	16.3	17.5	18.6
Peak PAE (%)	3.6	10.7	16.9	19.2	22.8	26.8	29.3
PAE @ OCP_{1dB} (%)	2.5	7.3	12.0	15.0	17.8	21.4	23.0
Peak small-signal gain (dB)	17.9	23.0	25.7	25.0	26.4	27.4	28.2
Peak P_{DC} (mW)	85.7	139.8	193.7	248.0	302.1	356.5	410.7
P_{DC} @ OCP_{1dB} (mW)	81.9	130.8	179.2	210.3	258.0	303.4	349.1

3.2.8. Input and output matching networks design

Each matching network, even though essentially intended for adapting impedance from/to 50 Ω, is designed for different operation. For the input matching network, a gain match was employed while for the output network, a power match. The gain match essentially matches 50 Ω to the input impedance of the gain stage; the power match, in its turn, matches the output impedance that delivers the highest power of the power stage (not necessarily the output impedance of the power stage) to 50 Ω.

3.2.8.1. Input impedance matching – "gain match"

The steps to design the input matching network were:

a) Run an S parameter simulation and determine the input impedance of the gain stage;
b) Design the input matching filter with an impedance matching calculator;
c) Implement the filter with ideal components and observe results;
d) Implement the filter with real components and observe results;
e) If results in c) and in d) are equivalent, the design ended. Else, adjust the network until results in c) and in d) are proper.

Running an S parameter simulation returned the PA's input impedance Z_{in} = 308.893 - j1069.17 Ω. In order to increase the reactance and facilitate matching, a 3.5 pF series capacitor was added before the gain stage. The updated Z'_{in} is 210.7706 – j492.9897 Ω. The Z'_{in} value was fed into the online impedance matching calculator from [21] which returned the tuning values of C = 259 fF and L = 12.1 nH for an "L" DC block filter topology, as presented in FIGURE 22. The results of steps c), d) and e) respectively as scenarios "Ideal", "Real" and "Accomplished", are displayed in TABLE 5. "Ideal" scenario presents the performance of the PA with ideal passives. "Real" scenario with real passives with parasitics and "Accomplished" scenario presents the adjusted values of real passives for the input match. The difference between "Real" and "Accomplished" resides in the fact that passive values of the later are not equal to those found in "Ideal". This is due to the parasitics in real passives. Those parasitics affect the impedance of the matching network, and thus, it is necessary to adjust capacitance and inductance in order to improve the match. This adjustment was done using optimization.

FIGURE 22 – A print from the matching calculator available from [21]. The source impedance (red box) is Z'_{in}. The purple dotted boxes show the network topology and components values.

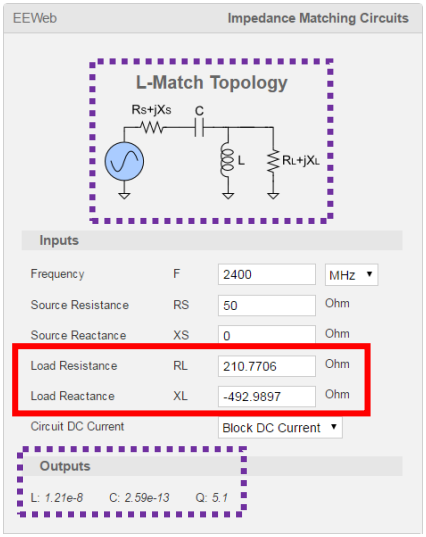


TABLE 5 – Comparison of PA's performance in three scenarios: ideal, real and accomplished for input impedance matching networks at 2.4 GHz.

Power mode		***111***	
Scenario	Ideal	Real	Accomplished
Network passive values	C = 259 fF and L = 12.1 nH	C = 259.09 fF and L = 12.108 nH	C = 260.24 fF and L = 9 nH
Total transistor width (µm)		875	
S_{11} (dB)	- 18.5	- 6.3	-12.5
S_{21} (dB)	31.0	28.3	29.0
Z_{in} (Ω)	49.96 –j0,136	115.9 +j56.83	65.65 – j20.9
OCP_{1dB} (dBm)	19.4	19.3	19.3
P_{SAT} (dBm)	18.5	18.6	18.6
Peak PAE (%)	31.3	31.2	31.6
PAE @ $OC1P_{dB}$ (%)	24.8	24.5	24.4
Peak small-signal gain (dB)	31.0	29.5	29.2
Peak P_{DC} (mW)	408.8	411.0	410.6
P_{DC} @ OCP_{1dB} (mW)	350.0	351.6	351.8

3.2.8.2. Output impedance matching – "power match"

In order to design the proper output matching network, the following steps were followed:

a) Run a loadpull simulation to determine the best combination among OCP_{1dB}, Gain and PAE for the PA;
b) Determine the impedance in which a) is placed;
c) Design the output matching filter with an impedance matching calculator;
d) Implement the filter with ideal components and observe results;
e) Implement the filter with real components and observe results;
f) If results in d) and in e) are equivalent, the design ended. Else, adjust the network until results in d) and in e) are proper.

A loadpull simulation is a PA design tool. It is a simulation in which the load impedance of the PA is systematically altered and the output power registered. In this way, the results of a loadpull simulation are a set of constant power contours in the Smith chart – as is presented in FIGURE 23. By evaluating the impedance placed in

a constant power circle, the designer can determine the output impedance of the PA, and thus, determine the output power.

The results of the loadpull simulation are presented in FIGURE 23. The purple dotted circles are the PAE curves. The external curve is PAE = 3.16 % while the most internal is PAE = 26.04 %. The red circles are the power gain at 2.4 GHz curves. Those curves vary from 26 dB (external) to 30 dB (inner curve). The blue dashed curves are the OCP_{1dB} curves. The external curve is OCP_{1dB} = 15 dBm and the most internal curve is OCP_{1dB} = 19.56 dBm. As those curves are not equally centered, it is possible to identify an impedance that favors any combination of those three parameters – it depends on the project requirements. For this work, the matching impedance Z_{match} = 7.541 + j1.635 Ω was chosen, favoring OCP_{1dB} and PAE over Power Gain.

The complex conjugated value of Z_{match} is then fed into an impedance matching calculator which returned C = 4.08 pF and L = 1.4 nH for a “L” DC blocking network, as is presented in FIGURE 24. The results of steps d), e) and f), in three scenarios, “Ideal”, “Real”, and “Accomplished” are displayed in TABLE 6. “Ideal” scenario presents the power performance of the PA when the matching network is composed of ideal passives. “Real” scenario, in its turn, presents the performance when the matching network is composed of real passives. “Accomplished” scenario presents the results of the adjusted matching network using a later optimization step to improve “Real” scenario performance.

FIGURE 23 – Loadpull contours. The set of constant Power Gain curves at 2.4 GHz is represented by the red circles, the set of constant OCP_{1dB} curves is represented by blue dashed circles and the set of constant PAE curves is represented by the purple dotted circles. Power Gain varies from 26 dB to 30 dB, PAE from 3.16 % to 26.04 % and OCP_{1dB} from 15 dBm to 19.56 dBm. Power and PAE increases as the circles diminishes. This is a schematic only simulation, and thus, results are better than the parasitic extracted circuit.

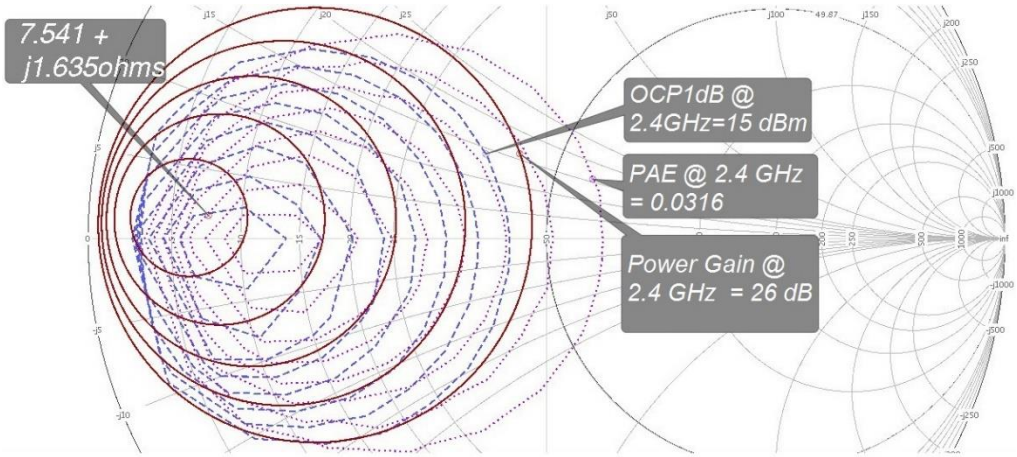


FIGURE 24 – A print from the matching calculator results found at [21]. The source impedance (red box) is the complex conjugate of Z_{match}. The purple dotted boxes show the network topology and components values.

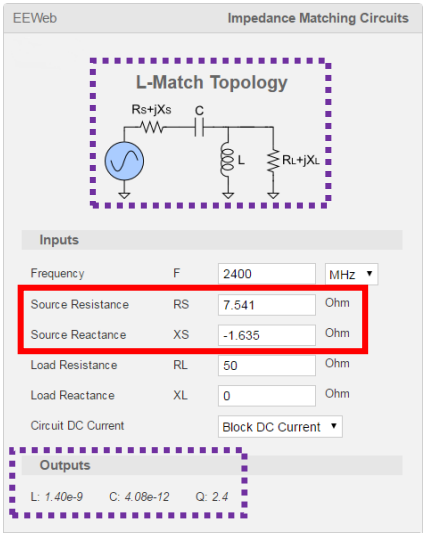


TABLE 6 – Comparison of PA's performance in three scenarios: ideal, real and accomplished output impedance matching networks.

Power mode	***111***		
Scenario	Ideal	Real	Accomplished
Network passive values	C = 4.08 pF and L = 1.4 nH	C = 4 pF and L = 1.4 nH	C = 3.5 pF and L = 1.275 nH
Total transistor width (µm)		875	
OCP_{1dB} (dBm)	19.5	19.0	19.3
P_{SAT} (dBm)	18.6	18.1	18.6
Peak PAE (%)	30.0	27.3	31.6
PAE @ OCP_{1dB} (%)	25.0	22.8	24.4
Peak small-signal gain (dB)	30.4	29.5	29.2
Peak P_{DC} (mW)	409.9	410.2	410.6
P_{DC} @ OCP_{1dB} (mW)	355.7	351.4	351.8

3.3. LAYOUT AND PARASITIC EXTRACTION

FIGURE 25 shows the proposed layout measuring 1320 µm by 1285 µm including pads. It is also possible to identify the building blocks presented in the schematic: (a) input matching network, (b) gain stage, (c) interstage matching component, (d) power stage, (e) output matching network, (f) voltage reference circuits and other peripheral blocks, such as (g) logic buffers, (h) supply decoupling capacitors and (i) ground potential distribution blocks.

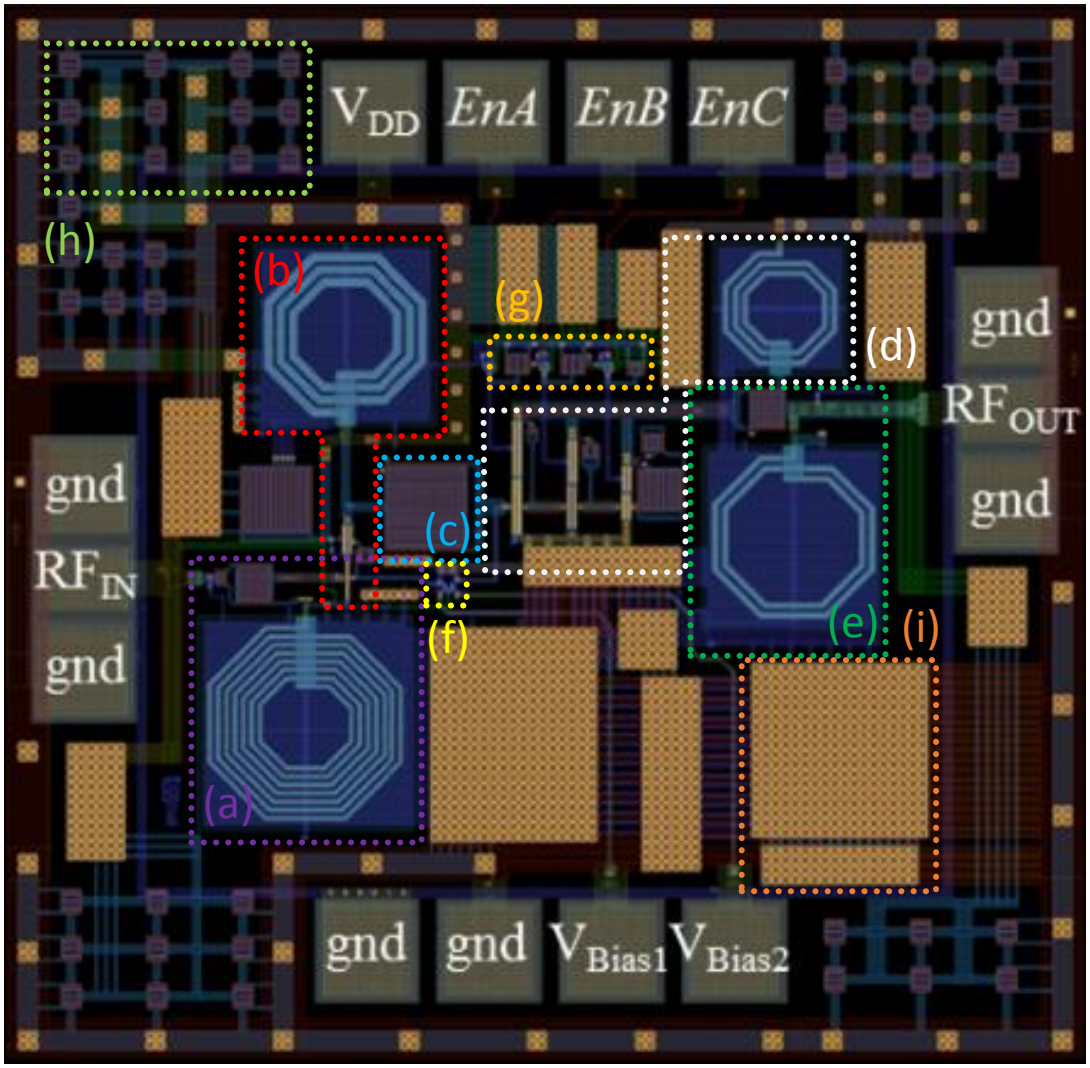
In order to build this PA, each building block was floor planned and routed independently. This block-by-block process grants the designer the ability to step check each section with the Design Rule Check (DRC) and Layout Vs. Schematic (LVS) tools, providing fewer and easier DRC errors to resolve and reducing conflicting errors when all sections are routed and placed together. The drawback of this method is that the composite final layout is not the most area-efficient design. Line mode – orthogonal check – was also performed, as MOSIS establishes. This last verification checks if all routing paths are orthogonal and grid spacing are set correctly. This verification should also be ran block-by-block and later ran on the composite layout.

During all levels layout, the RF signal flux was taken into account. Higher, wider and parallel layer metals were used where the RF current is high; decoupling

capacitors were placed parallel to the supply voltage across the circuit; ground and supply potentials were distributed across the chip by using multi-metal connection blocks.

No fabrication impacting errors were found during DRC verification, LVS and line mode ran errorless. After layout verification, parasitic resistances and capacitances were extracted using Quantus QRC and post-layout simulations were performed using the extracted circuit view in Cadence Spectre RF.

FIGURE 25 – The proposed layout presenting metals, transistors, passives and pads. From the top, clockwise: pads for voltage supply, control logic, RF GSG output, biasing voltages, and RF GSG input. The building blocks are: (a) input matching network, (b) gain stage, (c) interstage matching component, (d) power stage, (e) output matching network, (f) voltage reference circuits, (g) buffers, (h) supply decoupling capacitors and (i) ground potential distribution blocks. The background black layer is the substrate.



3.3.1. Advantages and drawbacks of the proposed circuit

The strong points of the proposed circuit are:

a) Fully integrated circuit: no external components or auxiliary voltages are required;
b) Only one supply voltage is necessary;
c) One biasing voltage for all power cells: all power cells were optimized to deliver the best operation under the in-chip generated biasing voltage;
d) Low component count;
e) Seven univocal selectable power modes;
f) Wide range output power selection.

while its drawbacks are:

a) Fixed biasing voltage of gain and power stages: during physical measurements, it will be not possible to vary the biasing voltage in the power cells independently;
b) If the power stage is turned off, the operation of the gain stage as an amplifier is irrelevant as virtually no power is delivered to the load;
c) Quantity of inductors: there are four inductors in this circuit, two used as chokes and two as part of matching circuits. Inductors occupy large space in the layout.

4 OBTAINED RESULTS AND DISCUSSION

In this section, a brief presentation of the employed simulator and the discussion of obtained results will be presented.

In the exposed results, three different terminologies will be employed: schematic-only, post-layout and measured. Schematic-only refers to the obtained results from a schematic simulation, meaning that no parasitic effects are accounted during simulation. Post-layout refers to the obtained results from a simulation after a layout parasitic extraction. Lastly, measured refers to physical measurement of the chip.

4.1. EMPLOYED SIMULATOR AND ANALYSES

Throughout this project, the employed simulator was Virtuoso Spectre Circuit Simulator and Accelerated Parallel Simulator RF Analysis (SpectreRF) version 15.1. Three types of analysis were employed: small-signal (SS), large-signal (LS) and DC (dc). For the SS category, S-parameters (sp). For the LS, Harmonic Balance (hb) and Envelope (envlp). Differently from the LS analysis that accounts LS effects (such as compression), SS analysis does not. In this way, SS runs are faster than LS runs. Another effect that makes simulation time longer is the presence of extracted parasitics. In this way, the most time-consuming simulations are combinations of LS with extracted layout parasitics while the least time-consuming are SS without extracted parasitics.

This discussion of simulation time is important as this work presents a seven-mode PA. In this way, LS extracted simulations were run at least seven times, meaning that time and computational power were limitations in this work.

Those four simulations were used for specific tasks: dc was used to obtain biasing voltages for the gain & power stages, sp was used to determine S parameter values, hb for loadpull & power performance and envlp for EVM and in-band & off-band power measurements.

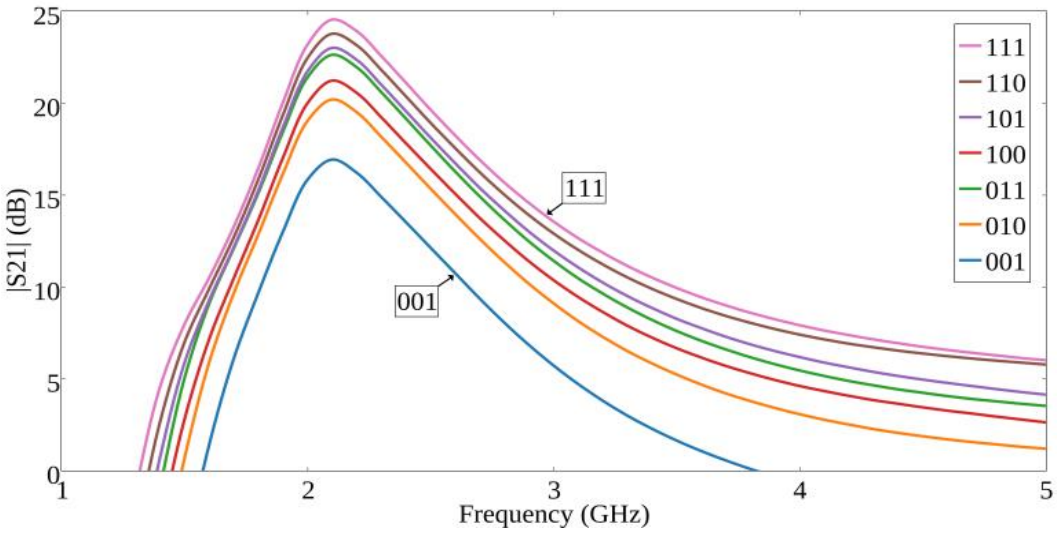
4.2. POST-LAYOUT RESULTS

The chosen metrics to evaluate the proposed PA are: S_{11}, S_{12}, S_{21}, S_{22}, μ, OCP_{1dB}, P_{SAT}, P_{DC} and PAE. From those last four measurements, composite measurements were defined, such as PAE at OCP_{1dB} and P_{DC} at OCP_{1dB}. The following

data are results for each of the available power modes. The chosen extracted parasitics were capacitance and resistance. These extractions were performed at a simulated temperature of 70 °C.

FIGURE 26 shows the S_{21} as a function of frequency for all seven modes. Each stage presents univocal power gain from 1 GHz to 5 GHz. At 2.4 GHz, the power gain ranges from 13.5 dB for the lowest power mode to 21.1 dB for the highest power mode.

FIGURE 26 – Post-layout direct gain vs. frequency for each configuration of the PA. Every stage performs univocal gain at 2.4 GHz, varying from 13.5 dB to 21.1 dB. From [20].



S_{11} as a function of frequency is presented in FIGURE 27 for all power modes. All stages perform almost the same, as the input matching is a function of the gain stage. At 2.4 GHz a slight difference is visible, but not relevant enough to change drastically PA's operation. It is also possible to observe that the circuit is not perfectly tuned to 2.4 GHz. This is because power was favored over gain in the design, and the input matching was slightly drifted from 2.4 GHz to improve power capabilities of the PA as a whole.

FIGURE 27 – Post-layout input matching vs. frequency for each configuration of the PA. All stages perform almost identically.

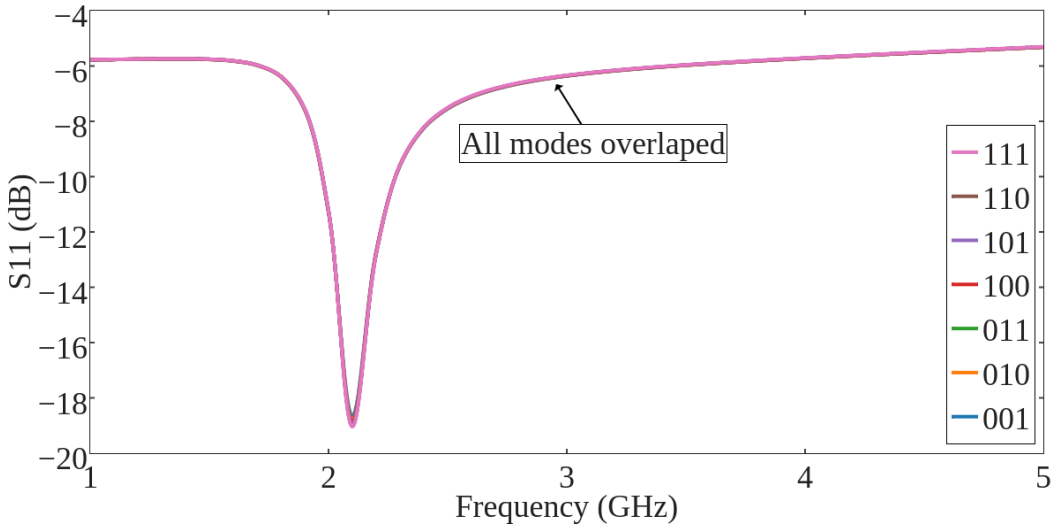


FIGURE 28 displays S_{12} for all selectable power modes vs. frequency. As the output matching was realized for mode “111”, its curve possesses the highest isolation possible for all modes, while “001” the lowest. It is important to observe that obtained results resides in the -62 dB to -82 dB range, showing that output is well isolated from input for all modes.

FIGURE 28 – Post-layout isolation vs. frequency for each configuration of the PA. As the output matching was realized for the highest power mode, this mode possesses the best isolation performance.

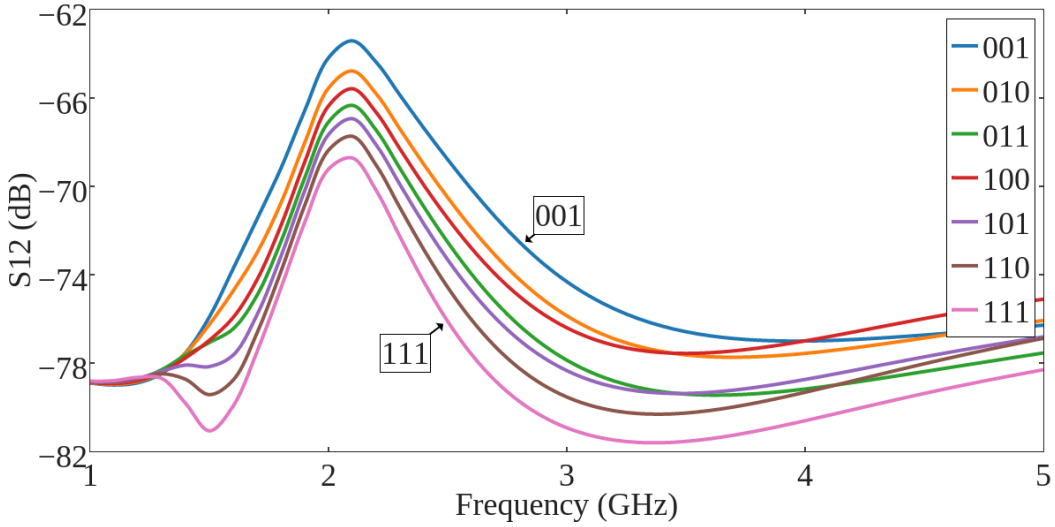


FIGURE 29, in its turn, presents the post-layout S_{22} as a function of frequency for all operating modes. As mentioned earlier, the output impedance of the PA was matched for the highest power mode. This project decision is observable in this

figure, as the curve “111” performs the best output matching values over all modes at 2.4 GHz. It is also possible to observe local minima, such as those at approximately 1.6 GHz. The more relevant minima are those for the lower power modes, “001”, “010” and “100”. This is due to output impedance of those stages and the matching network. As the output impedance of those stages are far from being matched to the chosen loadpull Z_{match} at 2.4 GHz, the output matching at 1.6 GHz also occurs. Other interesting observation is that mode “001” is not output matched to the load at 2.4 GHz. This means that the performance of that mode could be enhanced drastically. A way to “remove” those local minima would be by implementing an adaptive output matching network tuned at 2.4 GHz. In this way, when a lower power mode was selected, a different output matching would be automatically selected to improve the performance.

FIGURE 29 – Post-layout output matching vs. frequency for each configuration of the PA. The highest power mode presents the best output matching for all modes. Lower power modes, such as “001”, “010” and “100” perform a better output matching at approximately 1.6 GHz.

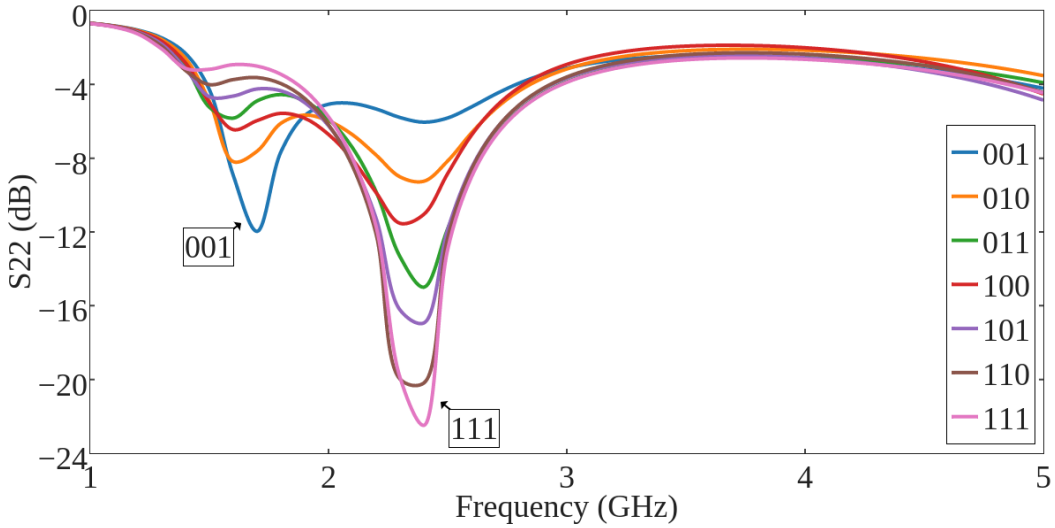


FIGURE 30 presents the simulated μ factor. As the obtained global minimum μ was 1.05 at 100 Hz, the PA is unconditionally stable for all modes.

FIGURE 30 – Post-layout μ vs. frequency for each selectable mode. The proposed circuit is unconditionally stable. From [20].

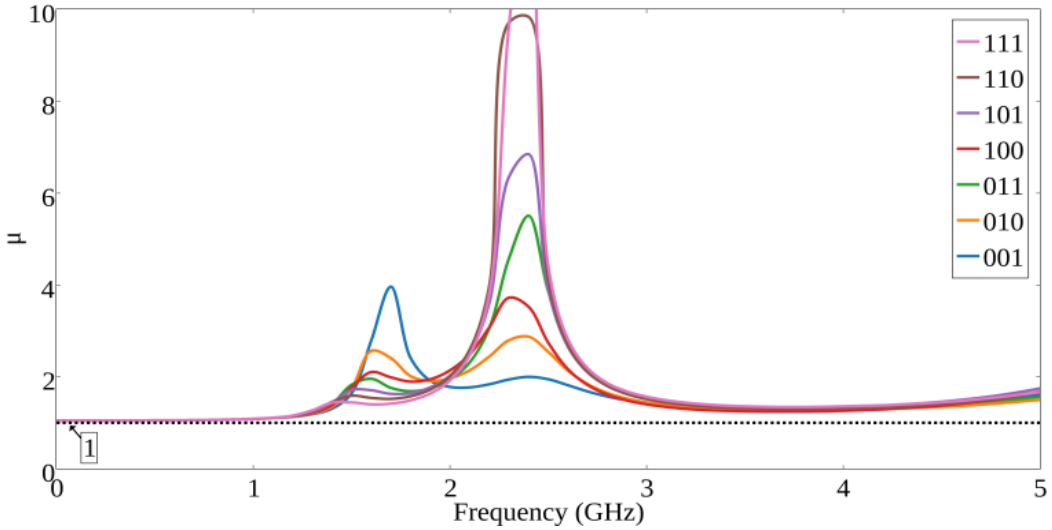


FIGURE 31 presents the simulated RF output power of the PA at 2.4 GHz. The low power mode reaches a 6 dBm OCP_{1dB} and an 8.1 dBm P_{SAT}, whereas the high power mode presents an 18.2 dBm OCP_{1dB} and an 18.9 dBm P_{SAT}. The OCP_{1dB} of each mode is, on average, 1.4 dB apart from each other, excepting “001” and “010” modes. Those modes are 5 dB apart due to the transistors in “C” being half as wide as those in “B”.

FIGURE 31 – Post-layout P_{OUT} vs. P_{IN} at 2.4 GHz for each selectable configuration of the proposed PA. The highest and lowest modes are approximately 12 dB apart. From [20].

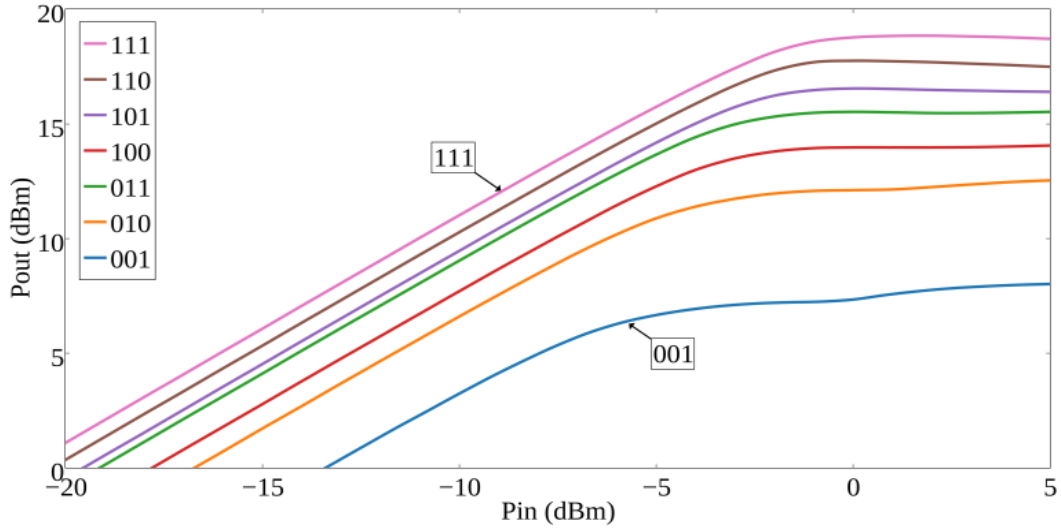


FIGURE 32 depicts the simulated consumed P_{DC} as a function of P_{OUT}. This graph acts as a decision provider when selecting one mode over another, as one can evaluate the P_{DC} consumption for a fixed P_{OUT} in every mode. For example, if the PA

is required to operate linearly at back-off with a P_{OUT} of 12 dBm, modes “011”, “100”, “101”, “110” and “111” would be eligible. However, considering the lowest P_{DC} consumption, mode “100” would be selected as it consumes a P_{DC} of approximately 40 mW less than “011” mode, 80 mW less than “101” mode and 209 mW less than “111” mode. This figure also examples why this PA operates saving P_{DC}. Contrary to conventional non-P_{DC} selectable PAs that operates consuming an approximately constant P_{DC}, this PA’s P_{DC} range may be selected between each operating mode, as long as the selected operating mode is capable of delivering the aimed P_{OUT}. For example, let us consider power mode “111” as a separate PA. If P_{OUT} of 10 dBm is aimed, P_{DC} would be approximately 475 mW. If P_{OUT} of 5 dBm is aimed, P_{DC} would still be approximately 475 mW. On the other hand, considering this work’s PA, if P_{OUT} = 10 dBm is aimed, mode “010” would be the best suited for the operation, as P_{DC} consumption is approximately 240 mW. In the same way, if P_{OUT} = 5 dBm is aimed, mode “001” would be the best fit, as P_{DC} consumption would be approximately 180 mW. This is how this PA saves energy and this why it is suited for long and short communications scenarios.

FIGURE 32 – Post-layout P_{DC} vs. P_{OUT} at 2.4 GHz for each selectable mode. The “111” mode and “001” are approximately 300 mW apart. From [20].

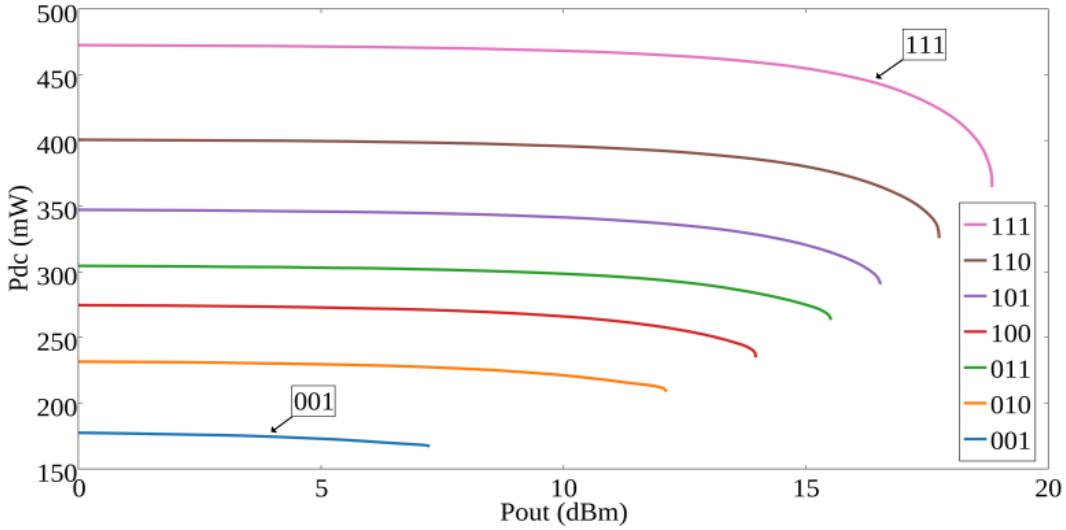
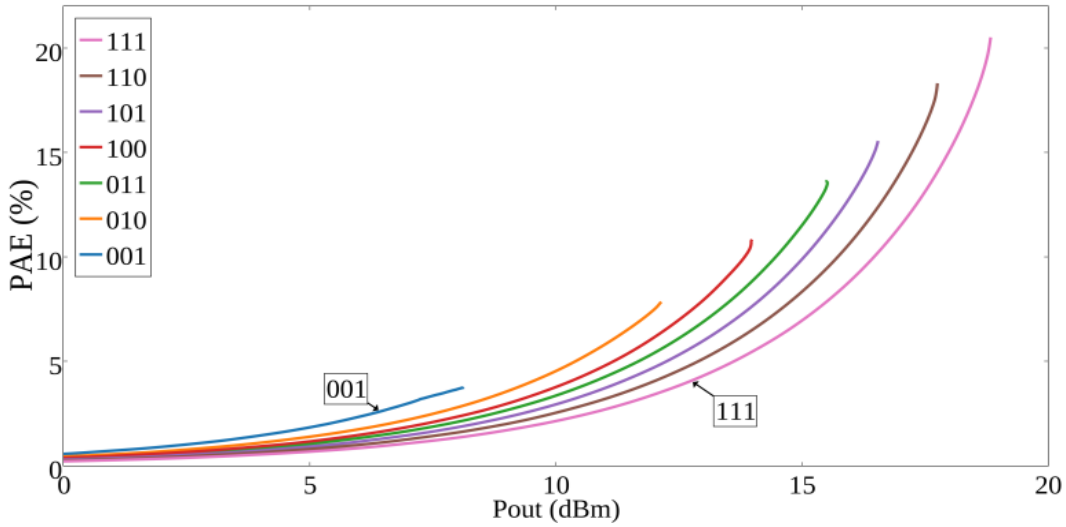


FIGURE 33 shows the simulated PAE in terms of P_{OUT} for all modes. For a P_{OUT} of 12 dBm, mode “100” possesses the highest PAE of 6.3% and, consequently, this mode is best suited for the application. As P_{DC} and PAE are inversely proportional, for a fixed P_{OUT}, the highest PAE means the lowest P_{DC} consumption.

FIGURE 33 – Post-layout PAE vs. P_{OUT} at 2.4 GHz for each selectable mode. From [20].



The obtained post-layout results for each operating mode are summarized in TABLE 7.

TABLE 7 – Post-layout results of each selectable operational mode at 2.4 GHz. Adapted from [20].

Mode	*OCP_{1dB} (dBm)*	*P_{SAT} (dBm)*	*Peak PAE (%)*	*PAE @ OCP_{1dB} (%)*	*P_{DC} @ OCP_{1dB} (mW)*	*S_{21} (dB)*	*S_{12} (dB)*	*S_{11} (dB)*	*S_{22} (dB)*
001	6.0	8.1	3.8	2.4	171	13.5	-67.4	-8.2	-6.0
010	11.0	12.9	8.7	5.9	218	16.8	-69	-8.2	-9.2
100	13.2	14.6	11.8	7.9	249	17.8	-70.9	-8.2	-15
011	14.8	16.1	14.7	11.2	278	19.2	-69.9	-8.2	-11.0
101	15.9	17.0	16.7	13.5	307	19.6	-71.7	-8.2	-16.9
110	17.3	17.9	19.2	15.3	350	20.4	-72.9	-8.2	-20.2
111	18.2	18.9	21.9	16.5	415	21.1	-74.3	-8.2	-22.5

4.3. COMPARISON TO STATE OF THE ART

A comparison with other published multimode PAs and obtained post-layout data is presented in TABLE 9. The compared PAs use 65 nm, 130 nm or 180 nm CMOS technology, the same approximate operating frequency and supply voltages varying from 1.5 V to 3.3 V. The proposed circuit presents the widest OCP_{1dB} and P_{SAT} ranges, 12 dB and 11 dB, respectively, the second lowest P_{DC} at OCP_{1dB} range (244 mW) and the second widest gain range (8 dB). The highest OCP_{1dB} and P_{SAT} values are achieved respectively by [17] and [18], which employ differential amplifiers architectures and occupy significantly more silicon area than the other works. Among

the circuits that do not use differential topologies, such as [16], [19] and this work, [16] achieves the highest OCP_{1dB} and P_{SAT} by using a higher supply voltage and off-chip biasing voltage and choke inductors. If compared at a P_{OUT} of 18 dBm, [17] consumes 1.6 times more P_{DC} than this work and occupies a 3.2 times larger area. Due to reconfigurability in gain stage, [19] achieves a peak power gain 15 dB higher than this work.

TABLE 8 – Comparison to state of art PAs. Redrawn from [20] .

Reference	***Tech. node (nm)***	***V_{DD} (V)***	***Gain (dB)***	***Area (mm^2)***	***P_{DC} @ OCP_{1dB} (mW)***	***OCP_{1dB} (dBm)***	***P_{SAT} (dBm)***
[16]	180	3.3	15 / 23	0.88	145 / 445	16 /22	17 /23
[19] [1]	130	1.8	27 / 36	1.2	179 / 225	16	17
[17]	130	1.5	NA [2]	5.48	239 / 688 [3]	NA	18 /23
[7]	180	3.3	NA / 35	2	429 / 2574	NA /27	21 /31
[18]	65	NA	NA	4.9	385 / 2840	17 /26	24 /28
This work [1]	130	1.8	13 / 21	1.7	171 / 415	6 /18	8 /19

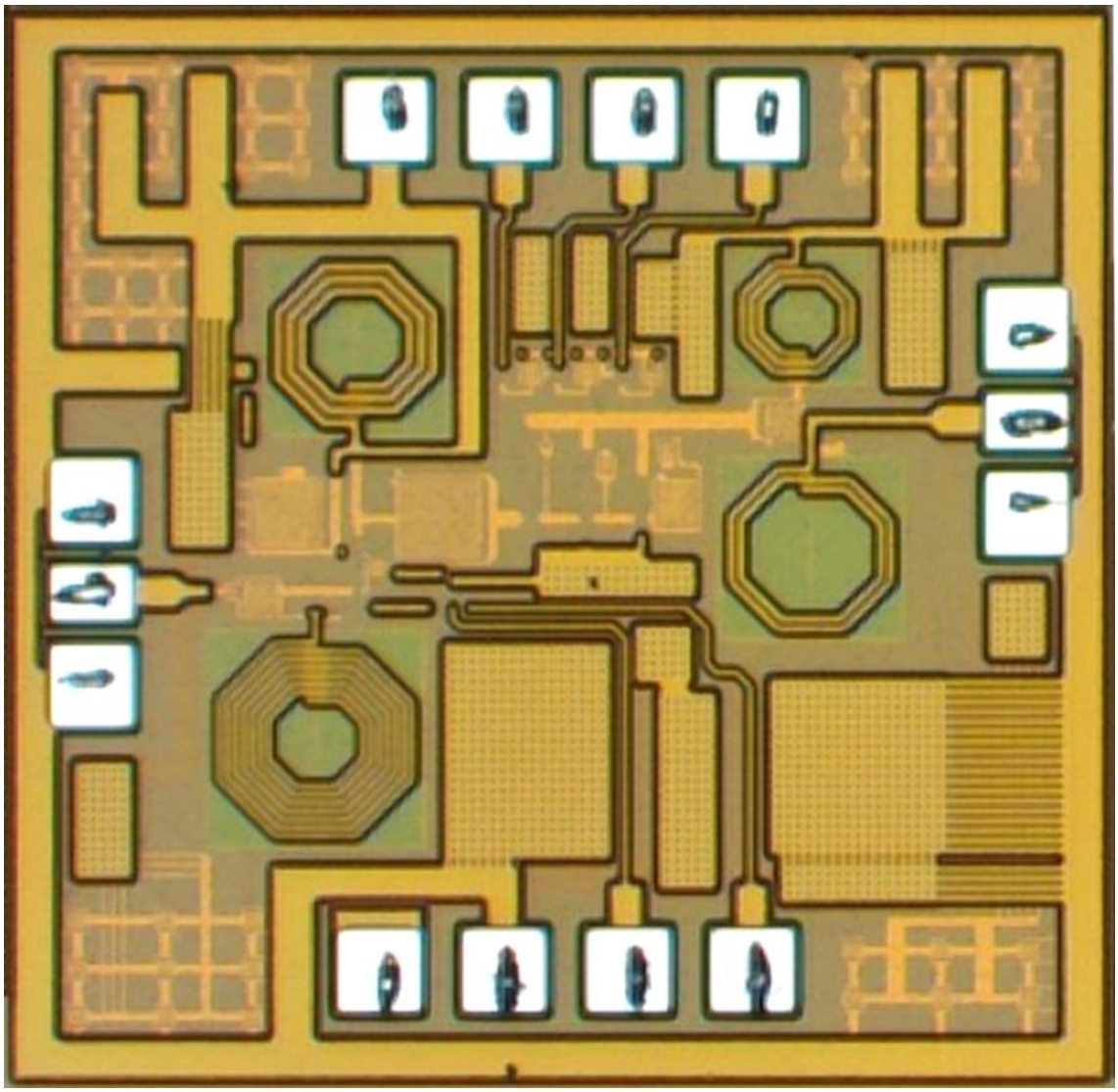
[1] Post-layout results. [2] Not available. [3] Peak value.

4.4. PRELIMINARY MEASUREMENT RESULTS

In this section, the measurement results of the PA will be discussed. After fabrication, the chip was sent to the Laboratoire de l'Intégration du Matériau au Système (IMS) at University of Bordeaux, where S parameters and preliminary large-signal continuous wave measurements for power mode “111” were conducted. For the power sweep measurements, the employed equipment were SMF100A signal generator from Rohde & Schwarz, E441B power meter and 8485A power sensor, both from Keysight. For the S parameters measurements, Keysight’s E8361A Programmable Network Analyzer and millimeter test heads were employed. As the general setup, the probe station PM8 and |Z| Probe from Cascade Microtech were employed. DC power supply is Keysight’s E3631A. A microphotograph of the fabricated PA is presented in FIGURE 34. The small markings in the pads are probe’s contact

markings. As the measurement was accomplished by a professional at IMS laboratory, a measurement guide was written. This measurement guide possesses information such as orientation markings, pads definitions, measurement method, measurement conditions and expected results.

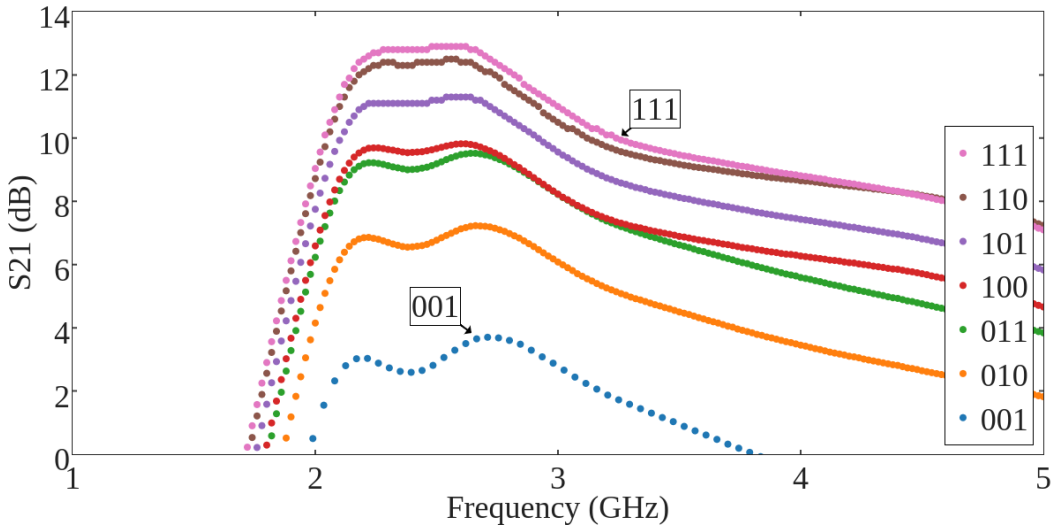
FIGURE 34 – Microphotograph of the PA. Acknowledgments: Laboratoire IMS at University of Bordeaux, France.



The metrics used for chip characterization were: S_{11}, S_{12}, S_{21}, S_{22} and μ. For the power evaluation, only mode “111” at 2.5 GHz was measured.

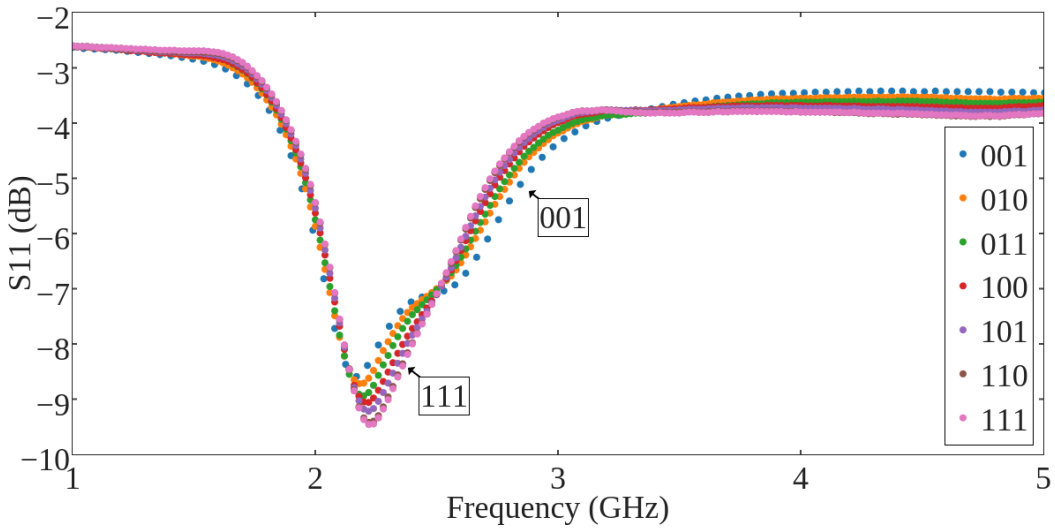
The measured S_{21} as a function of frequency is presented in FIGURE 35 for all seven modes. The PA no longer presents univocal power modes operation for the 4 GHz bandwidth, but presents univocal S_{21} at 2.4 GHz. The gain ranges from 2.6 dB for the lowest power mode to 12.8 dB for the highest power mode, at 2.4 GHz.

FIGURE 35 – Measured direct gain vs. frequency for each configuration of the PA.



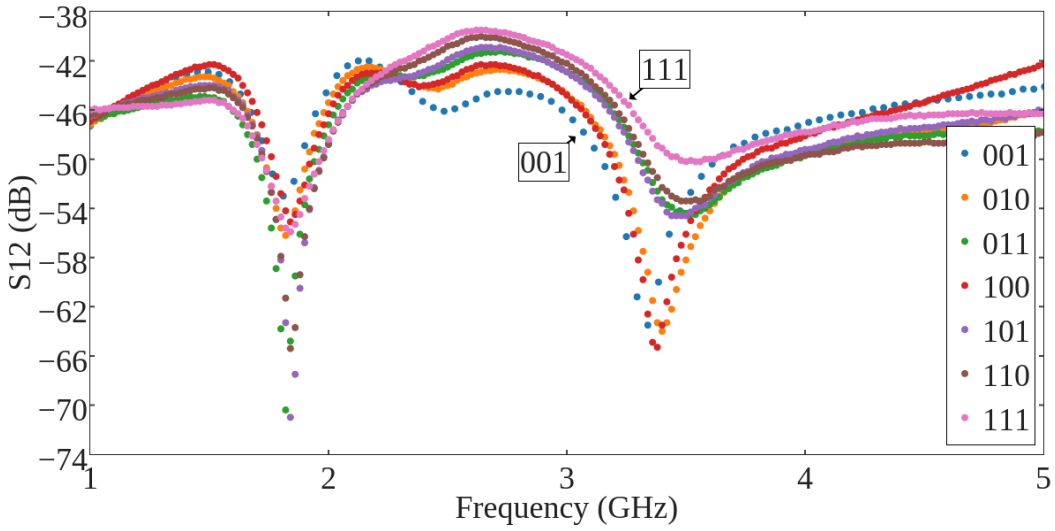
In FIGURE 36 S_{11} as a function of frequency for all power modes is presented. For all modes, the curves possess almost the same shape, apart from some visible attenuation at lower power modes. Measured results are near post-layout results, being measured results at maximum 1.0 dB higher.

FIGURE 36 – Measured input matching vs. frequency for each configuration of the PA. All stages perform almost identically.



S_{12} for all selectable power modes vs frequency is shown in FIGURE 37. Isolation results performed well below expected. Post-layout results ranged from -74.3 dB to -67.4 dB at 2.4 GHz, while measured from -45.3 dB to -41.2 dB. This translates to a maximum difference of 29 dB lower for post-layout results. It is also possible to observe no global minima at 2.4 GHz; instead, minima are found near 1.8 GHz and 3.4 GHz.

FIGURE 37 – Measured isolation vs. frequency for each configuration of the PA.



In FIGURE 38, S_{22} of all power modes are presented from 1 GHz to 5 GHz. From the post-layout results, power mode “100” and higher modes should be tuned to 2.4 GHz. This does not happen to measured results, as all modes drifted to a lower tuning frequency, being “111” the closest to 2.4 GHz. The best performance obtained was from the highest power mode, achieving -8.3 dB for 2.4 GHz. FIGURE 39 presents μ as a function of frequency for all power modes. All seven modes are unconditionally stable.

FIGURE 38 – Measured output matching vs. frequency for each configuration of the PA.

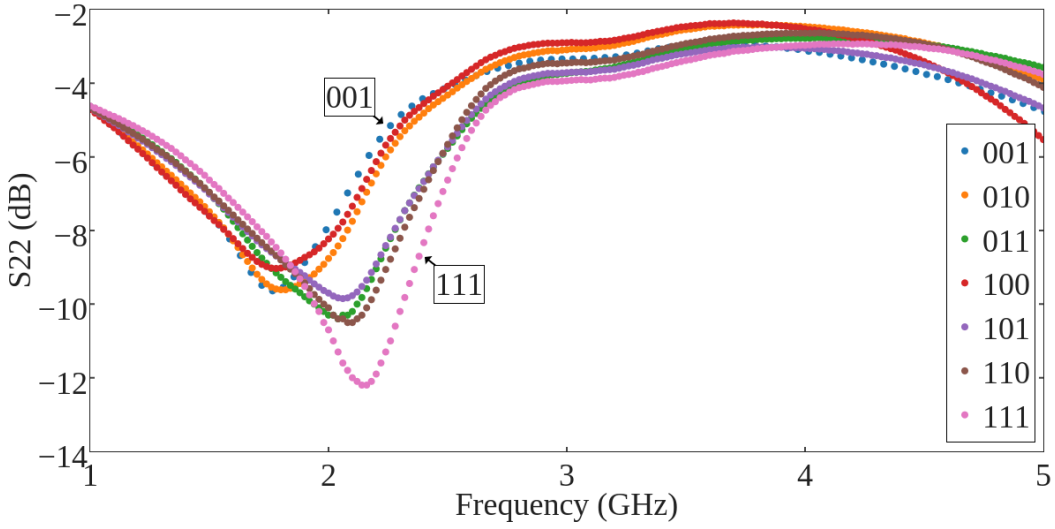
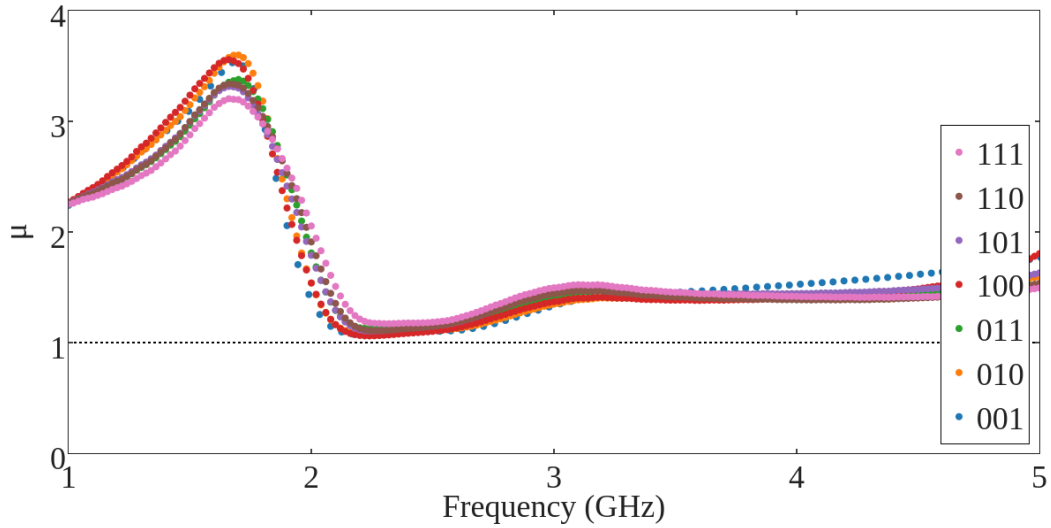


FIGURE 39 – Measured μ vs. frequency for each selectable. The proposed circuit is unconditionally stable.



The power performance for mode “111” at 2.5 GHz is presented in FIGURE 40. Post-layout results performed OCP_{1dB} = 18.2 dBm and P_{SAT} = 18.9 dBm, while measured results performed OCP_{1dB} = 9.4 dBm and P_{SAT} = 12.6 dBm. In FIGURE 41 P_{DC} vs. P_{OUT} for the highest power mode is displayed. Calculated P_{DC} at OCP_{1dB} = 252 mW, 163 mW lower than expected. In FIGURE 42 PAE vs P_{OUT} for the same measurement conditions is shown. Measured Peak PAE was 16 percentage points below expected (5.9 %), while PAE at OCP_{1dB} was 13.3 percentage points below (3.2 %). The obtained measurement results are summarized in TABLE 9.

FIGURE 40 – Measured P_{OUT} vs. P_{IN} at 2.5 GHz for mode “111”.

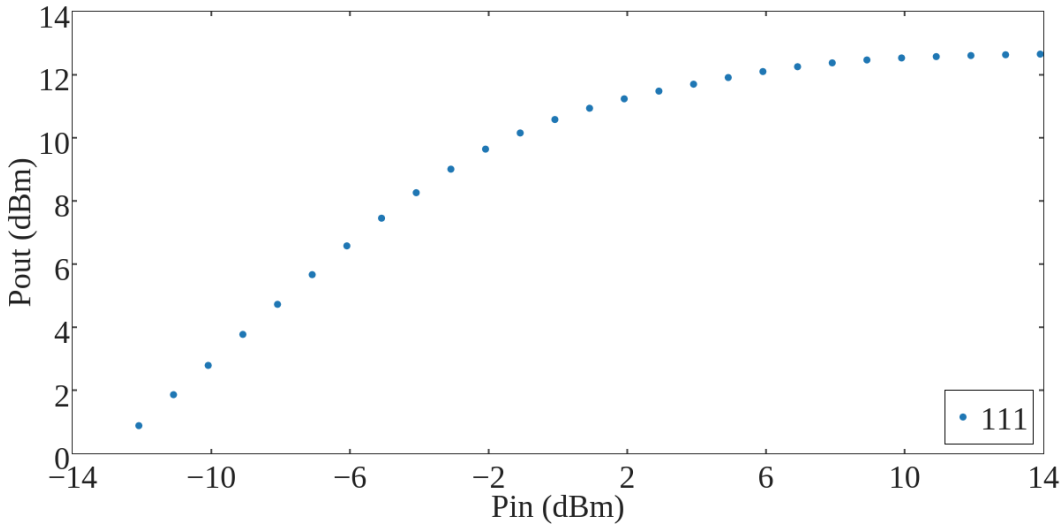


FIGURE 41 – Measured P_{DC} vs. P_{OUT} at 2.5 GHz for mode “111”.

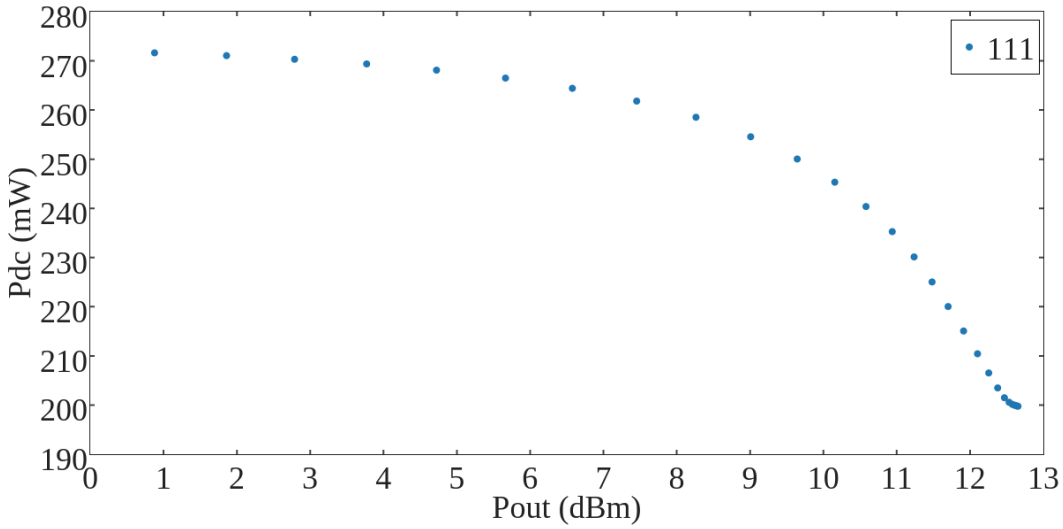


FIGURE 42 – Measured PAE vs. P_{OUT} at 2.5 GHz for mode “111”.

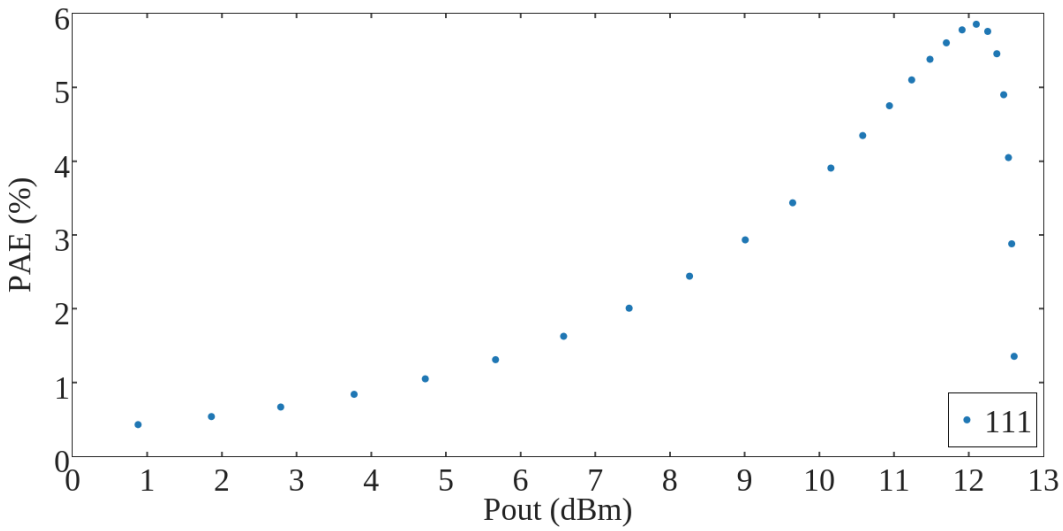


TABLE 9 – Measured results of the PA. S parameters are measured at 2.4 GHz while large signal measurements were performed at 2.5 GHz.

Mode	***OCP_{1dB} (dBm)***	***P_{SAT} (dBm)***	***Peak PAE (%)***	***PAE @ OCP_{1dB} (%)***	***P_{DC} @ OCP_{1dB} (mW)***	***S_{21} (dB)***	***S_{12} (dB)***	***S_{11} (dB)***	***S_{22} (dB)***
001	-	-	-	-	-	2.6	-45.3	-7.2	-4.4
010	-	-	-	-	-	6.6	-44.1	-7.3	-4.8
100	-	-	-	-	-	9.0	-43.2	-7.5	-6.7
011	-	-	-	-	-	9.5	-44.0	-7.7	-4.6
101	-	-	-	-	-	11.1	-42.9	-7.8	-6.7
110	-	-	-	-	-	12.3	-41.9	-8.0	-6.9
111	9.4	12.6	5.9	3.2	252	12.8	-41.2	-8.0	-8.3

4.5. CONSIDERATIONS ON POST-LAYOUT VS. MEASURED RESULTS

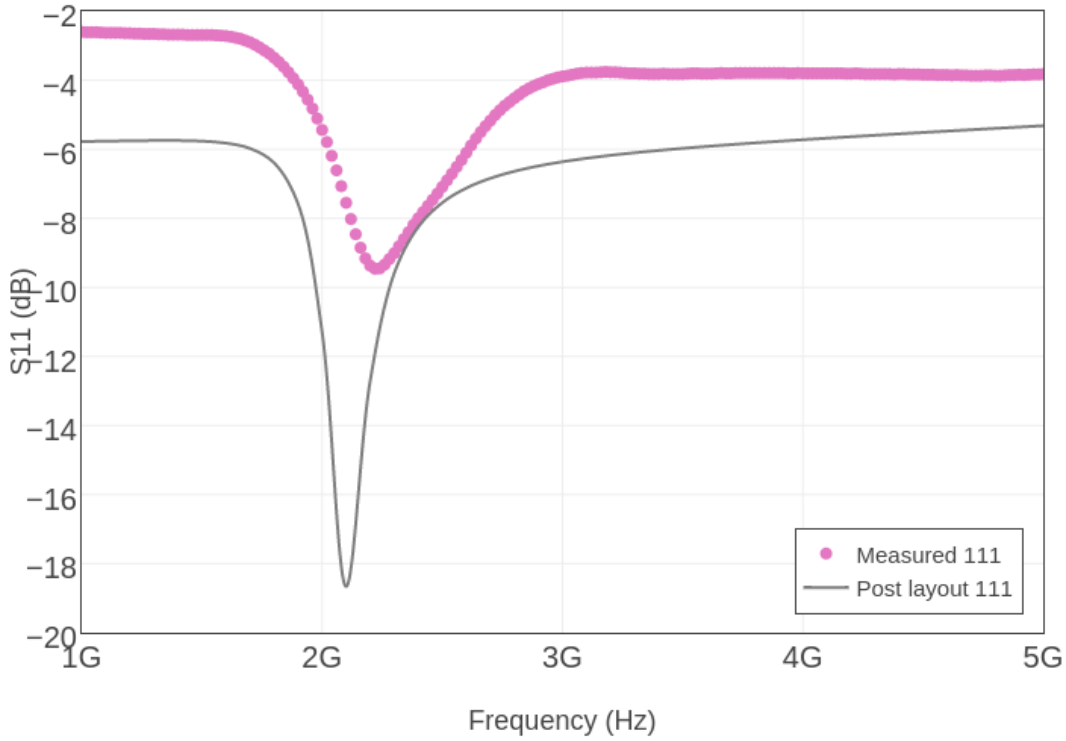
In an overall evaluation, measured results performed well below post-layout results: measured results are situated between post-layout modes “001” and “010”, the lowest power modes available. At least four main considerations were considered to explain the discrepancy:

a) Passives issues
   a. Fabricated passive impedances comply with passive impedances models (for the employed passives, indp_inh, mimcap_inh, oprppres_inh);
      i. Post-layout and measured S_{11} perform almost the same. Input matching is performed by means of passive components and depends on probe’s impedance and input impedance of gain stage. Thus, it is possible to imply that employed probes are calibrated & providing (approximated) 50 + j0 Ω, fabricated passives comply with extracted passives and fabricated & extracted input impedance of gain stage comply.

b) Devices issues
   a. Output impedance of fabricated MOSFETs does not comply with device models (for the employed devices lvtnef_rf and nfet) for the aimed power level and for the employed widths (≤ 400 μm);
      i. Considering that S_{11} performed as expected (as is presented in FIGURE 43) while other S parameters that accounts output port did not (S_{12}, S_{22} and S_{21}).
   b. Output impedance of fabricated MOSFETs is being altered due to the ESD protection diode.
      i. Diodes may affect the operation of the fabricated circuit.

c) General issues
   a. Leakage substrate current causing isolation to degrade (comparing post-layout and measured S_{12});
   b. Bias circuits are not generating adequate voltages;
   c. Fabricated pads impedances do not comply with model pad impedances (passives are over or under dimensioned);

FIGURE 43 – Comparison between measured “111” and post-layout “111”.



d. Parasitic extraction is not being performed correctly;

d) Measurement issues and layout problems

a. Incorrect measurement procedure;

b. Probes impedance causing mismatch.

i. The hypothesis is weak, as preparation and measurement were conducted by experienced professional.

Some steps are listed below in order to debug future revisions of the hardware:

a) Key power modes should be chosen to be measured to facilitate measurement;

b) Internal bias circuitry should be removed or new pads connected to the gate of gain and power stages should be added;

c) Verify the possibility to remove ESD protection diodes;

d) Separate the PA into gain only and power only PAs;

e) Independently characterize MOSFETs device models, such as nfet and lvtnfet_rf.

4.6. EVALUATING SOME CONSIDERATIONS

In this section, some evaluations on the schematic will be tested in order to approach post-layout and measured results. To do so, optimization was employed. The method consisted on optimizing the post-layout circuit up to the point were obtained S parameters are similar to measurement. After optimization, simulation with updated values on the highest power mode is performed and obtained results are compared to measured results.

- Biasing circuits are not generating adequate voltages.
    - Bias was adjusted to emulate the measured circuit. Obtained gain and power stages gate voltages are 594.3 mV and 304.5 mV, meaning that the voltage applied to V_{BIAS1} and V_{BIAS2} pads should be 800 mV and 320 mV, respectively. Although it is known that during measurement the voltage applied to V_{BIAS1} and V_{BIAS2} were 1.8 V, it is not possible to fully evaluate this hypothesis, as no gate biasing voltages are accessible. Obtained results are presented in TABLE 10, in the “Bias adjustment” header. Even with bias adjustment, post-layout and measured circuits perform very differently.
- Fabricated pads impedances do not comply with model pad impedances
    - Pads were removed in order to understand possible effects. Results are presented in TABLE 10, in the header “RF pads removed”. Results concerning input impedance were the most affected. S_{11} improved 7.2 dB at expense of efficiency (11.1 percentage points degradation). Removing pads showed a high degradation on the performance of the circuit. This could mean that employed pads models are not as accurate as expected.
- Parasitic extraction is not being performed correctly
    - Several alternative parasitic extractions were performed with Assura and PVS. Due to some errors, some extraction files were not generated. Obtained extraction files are:
        - Assura: 20160617_extracao_B: Capacitance coupling mode: coupled.

- Assura: 20160617_extracao_E: Capacitance coupling mode: decoupled.
- PVS: none could be generated.

- Apart from some small signal parameters improvements or degradations, no significant large signal variation was observed, as is presented in TABLE 10. It is not possible to determine which capacitance coupling extraction should be performed for this circuit.

TABLE 10 – Post-layout results at 2.4 GHz of the alternative circuits to test different conditions to approach post-layout and measured results.

Scenario	*Measured*	*Post-layout*	*Bias adjust-ment*	*20160617_ extracao_B*	*20160617_ extracao_E*	*RF pads removed*
S_{11} *(dB)*	-8.0	-8.2	-9.3	-14.5	-9.4	-15.4
S_{22} *(dB)*	-8.3	-22.5	-7.7	-24.7	-20.2	-20.1
S_{12} *(dB)*	-41.2	-74.3	-68.1	-64.3	-75.0	-71.8
S_{21} *(dB)*	12.8	21.1	15.2	25	22.1	26
$OC1P_{dB}$ *(dBm)*	9.4	18.2	5.0	18.6	18.6	9.6
P_{SAT} *(dBm)*	12.6	18.9	15.4	18.4	18.4	15.9
Peak PAE (%)	5.9	21.9	10.2	21.9	22.0	10.8
PAE @ OCP_{1dB} *(%)*	3.2	16.5	2.3	17.1	17.1	1.9
P_{DC} *@* OCP_{1dB} *(mW)*	252.0	415.0	132.0	426.0	425.0	464.0

4.7. ACCOUNTING PROCESS VARIATIONS DURING FABRICATION

Another project requirement is that the IC must be process-robust. This means that the circuit must function over a range of expected process variations during manufacturing, temperature and voltage. CMRF8SF has essentially two types of simulations to account those variations: corner simulations as a PVT analysis and Monte Carlo statistical simulation.

4.7.1. Process-Voltage-Temperature analysis of the proposed circuit

In order to characterize the PA operation limits, a PVT analysis may be employed. This analysis accounts variations on the CMOS fabrication process and circuits' operating temperature and supply voltage. Due to doping variations during fabrication process, MOSFETs may operate faster (lower parasitic capacitances) or

slower, affecting directly on the gain, load impedance and bandwidth of PA. Temperature and supply voltage directly affect the output power capability of the PA [3].

4.7.1.1. Corners, voltage and temperature variation

The considered corners were Typical (TT), Fast-Slow (FS), Slow-Fast (SF), Fast-Fast (FF), Slow-Slow (SS), Fast-Fast Functional (FFF) and Slow-Slow Functional (SSF). TT corresponds to the simulation where corners parameters represent the nominal process fabrication. Due to channel length and dopant variations, it is possible for NFETs to run faster and PFETs slower (FS) and vice versa (SF). In their turn, FF and SS corners represent fast and slow timing for both CMOS devices. These four corners are known as performance corners and their corner parameters are varied for less than ± 3 σ deviations. Functional corners FFF and SSF, in their turn, account critical parameters at ± 3 σ deviations. While testing the processes, V_{DD} was varied ± 10 % at two temperature extremes of 40 °C and 125 °C. Both V_{DD} tolerance and temperature range consider consumer electronics operating variations. The 20 percentage points are intended to accommodate conventional consumer electronics supply voltage variations and the temperature interval to contain the range of 0 °C to 85 °C with a 40 °C offset to accommodate the temperature rise caused by the power handled by the PA. This analysis accounts the highest power mode only.

4.7.1.2. Post-layout PVT analysis results

In order to determine extreme operation scenarios, the PA's OCP_{1dB} was evaluated. FIGURE 44 presents the obtained results. The best scenario obtained was a combination of FF corner and V_{DD} of 1.98 V at 40 °C while the worst was a combination of SSF corner and V_{DD} of 1.62 V at 125 °C. The typical case considers a V_{DD} of 1.8 V at 70 °C.

FIGURE 44 – Post-layout PVT analysis in terms of OCP_{1dB} of the proposed PA. Each set of symbols represents a different corner. The pink dashed circle indicates the highest OCP1dB while the purple dashed circle the lowest. Extreme cases obtained at V_{DD} = 1.8 V (SSF and FF) were evaluated at V_{DD} = 1.8 V (SSF and FF varying V_{DD} ±10 %). From [3].

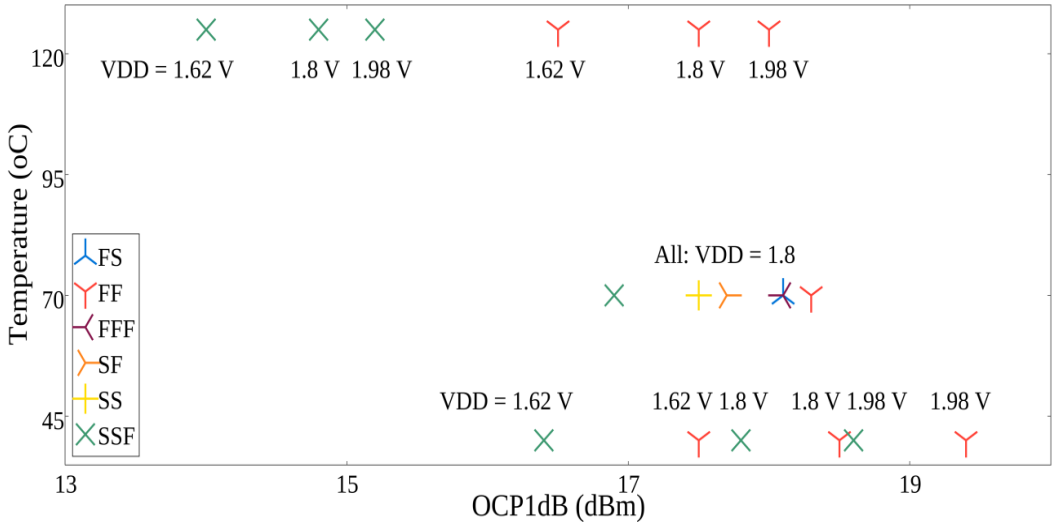


FIGURE 45 details the simulated μ stability factor as a function of frequency for typical and extremes scenarios. All scenarios are unconditionally stable and the global minimum μ is 1.05 at 100 Hz. Considering the average value of μ at a 5 GHz bandwidth, the least stable combination is FF corner, V_{DD} of 1.98 V and 40 ºC while the most stable is composed by SSF corner, V_{DD} of 1.62 V and 125 ºC. At 2.4 GHz, TT performs a power gain (S_{21}) of 21.1 dB while FF achieves 23.5 dB and SSF 16.9 dB (FIGURE 46). TT performs an input port voltage reflection coefficient (S_{11}) of -8.2 dB and reverse gain (S_{12}) of -72.8 dB. FF, in its turn, achieves S_{11} of - 9.2 dB and an S_{12} of -75.2 dB, respectively. Lastly, SSF reaches -7 dB and -72.8 dB, respectively (FIGURE 47 and FIGURE 48).

FIGURE 49 presents the power performance of the PA. Typical scenario presents an OCP_{1dB} of 18.2 dBm and P_{SAT} of 18.9 dBm, while best and worst scenarios reach an OCP_{1dB} of 19.4 dBm and a P_{SAT} of 19.9 dBm and an OCP_{1dB} of 14 dBm and a P_{SAT} of 16.2 dBm, respectively.

FIGURE 45 – Post-layout μ vs. frequency for typical and extreme scenarios. The PA is unconditionally stable. From [3].

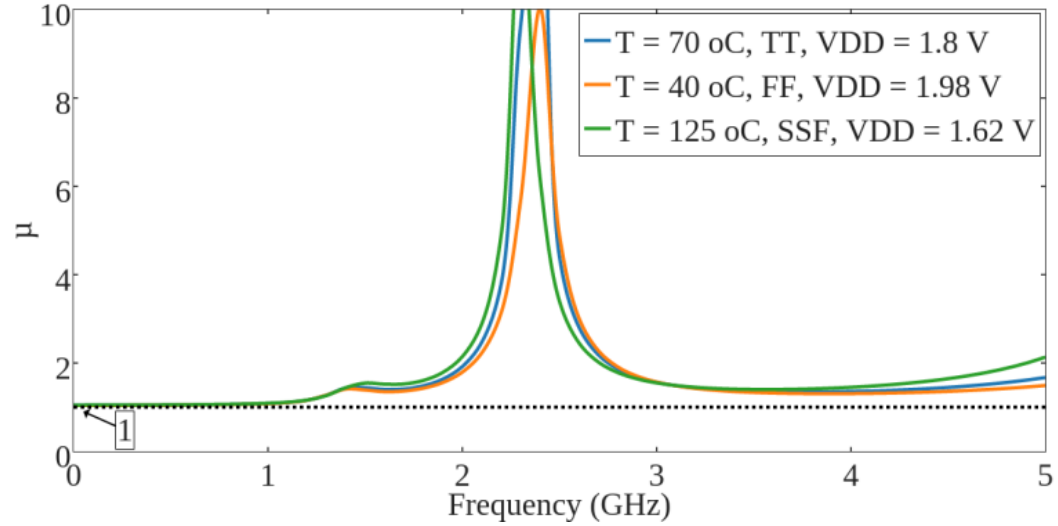


FIGURE 46 – Post-layout S_{21} vs. frequency for typical and extreme scenarios. At 2.4 GHz, TT performs S_{21} of 21.1 dB, FF 23.5 dB S_{21} and SSF 16.9 dB S_{21}. From [3].

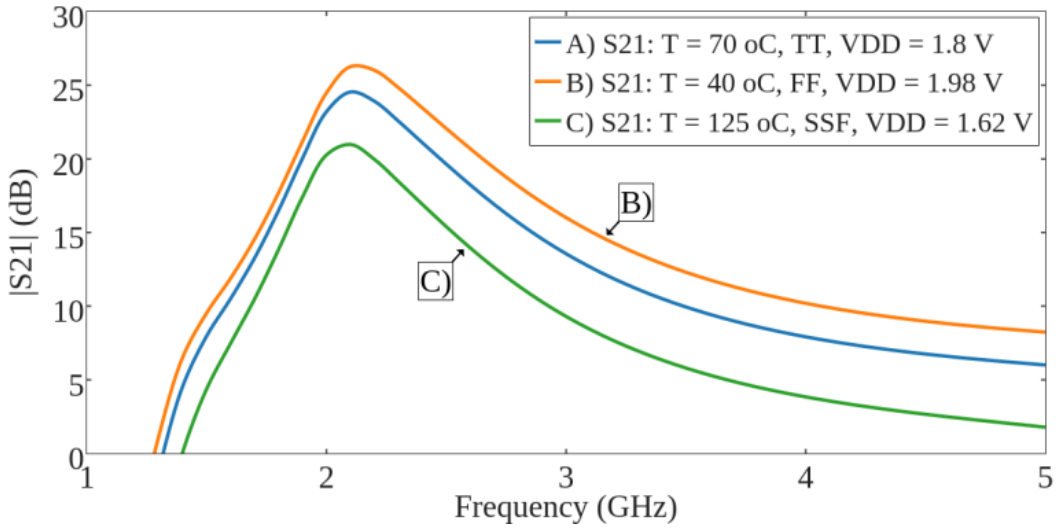


FIGURE 47 – Post-layout S_{11} vs. frequency for typical and extreme scenarios. At 2.4 GHz, TT performs S_{11} of -8.2 dB, FF -9.2 dB S_{11} and SSF -7 dB. From [3].

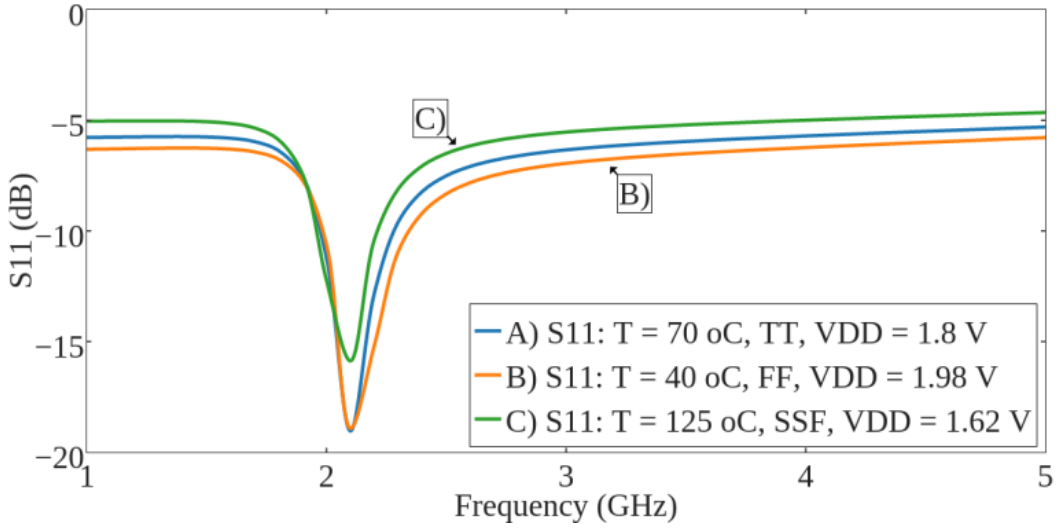


FIGURE 48 – Post-layout S_{12} vs. frequency for typical and extreme scenarios. At 2.4 GHz, TT performs S_{12} of -72.8 dB. FF -75.2 dB and SSF -70.3 dB. From [3].

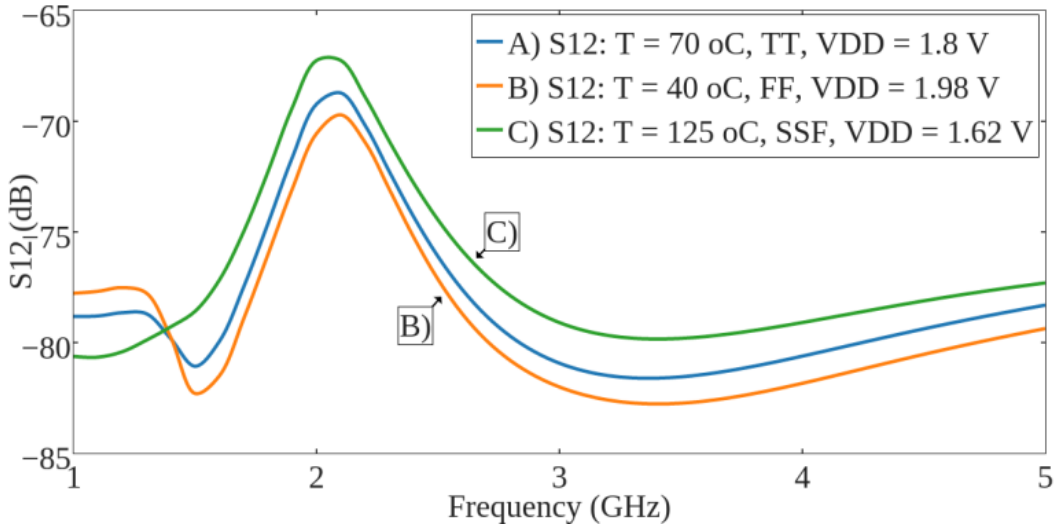
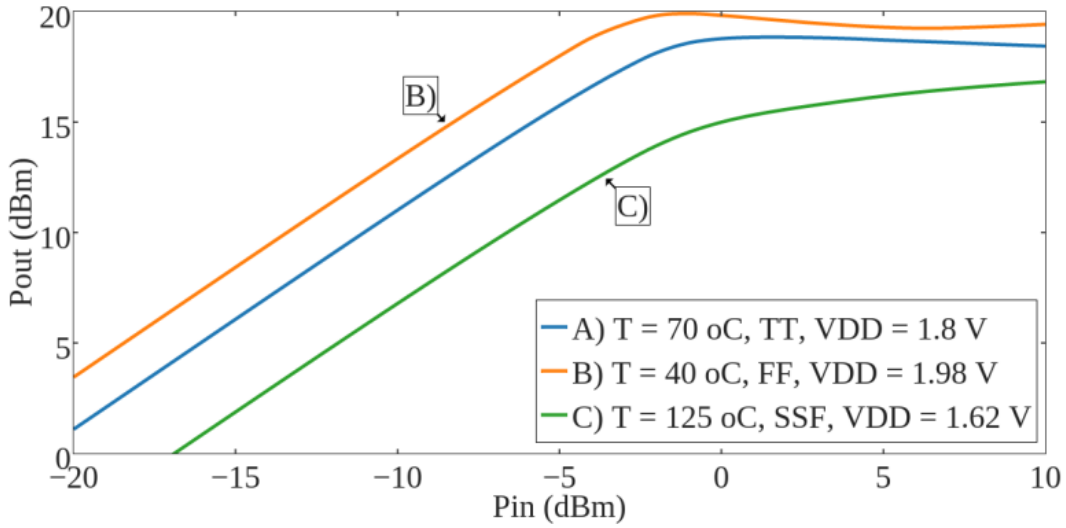


FIGURE 49 – Post-layout P_{OUT} vs. P_{IN} for typical and extreme scenarios. Highest OCP_{1dB} reaches 19.4 dBm and lowest 14 dBm. P_{SAT} are 19.9 dBm and 16.2 dBm, respectively. From [3].



In FIGURE *50* P_{DC} is presented as a function of RF output power. Considering linear operation in all three scenarios, the least power consuming combination is SSF corner with a supply voltage of 1.62 V at 125 ºC. This scenario consumes a peak P_{DC} of 26.3 dBm and a P_{DC} at OCP_{1dB} of 25.9 dBm. The most P_{DC} consuming scenario has a peak P_{DC} of 27.2 dBm and a P_{DC} at OCP_{1dB} of 26.6 dBm. If a 14 dBm P_{OUT} is considered, the corners SSF, TT and FF consumes 25.9 dBm, 26.6 dBm and 27.1 dBm, respectively.

FIGURE 51 depicts PAE in terms of P_{IN}. Considering PAE at OCP_{1dB}, corner SSF reaches 7.1 %, TT performs 16.5 % and FF presents 17.4 %. For a -2 dBm P_{IN}

value, SSF reaches 7.1 %, TT 15.7 % and FF 20.2 %. TABLE 11 summarizes obtained post-layout results across the extreme and typical scenarios.

FIGURE 50 – P_{DC} vs. P_{OUT} for typical and extreme scenarios. The worst scenario consumes 25.9 dBm at OCP_{1dB} while the best 26.6 dBm. From [3].

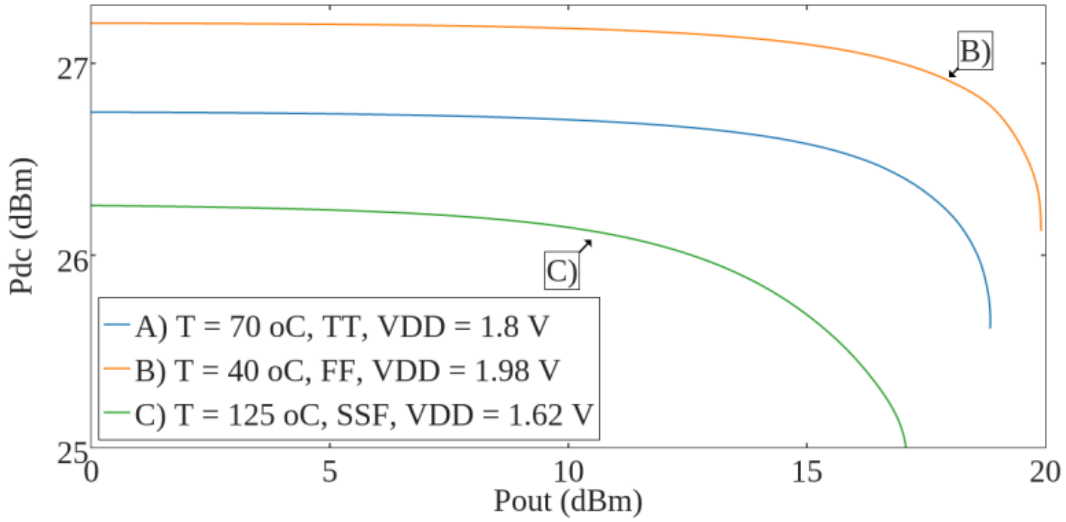


FIGURE 51 – PAE vs. P_{IN} for typical and extreme scenarios. At OCP_{1dB} corner SSF reaches 7.1 %, TT 15.7 % and FF 17.4 %. From [3].

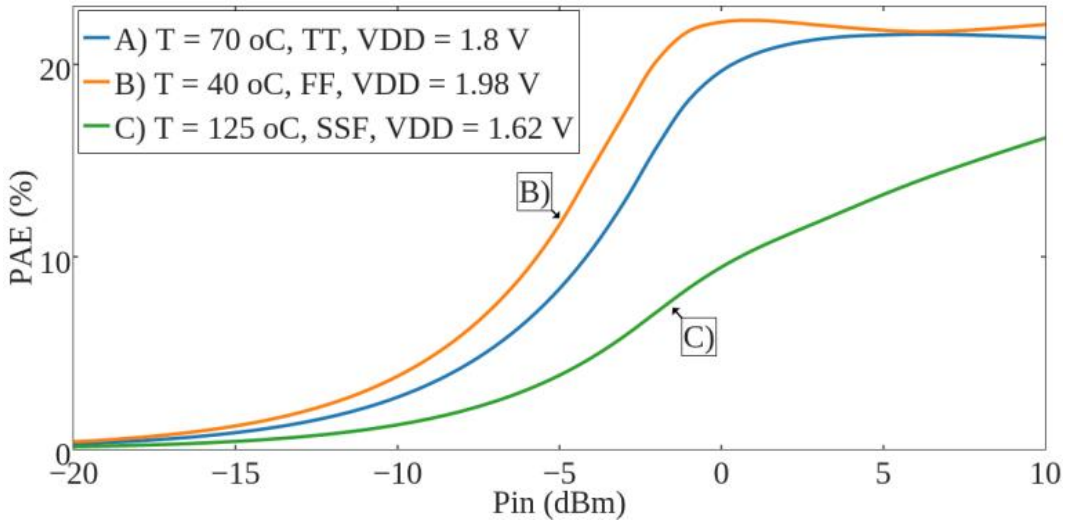


TABLE 11 – 2.4 GHz results of extremes and typical scenarios. From [3].

Scenario	***Corner***	***Temperature (°C)***	***OCP_{1dB} (dBm)***	***P_{SAT} (dBm)***	***P_{DC} @ OCP_{1dB} (mW)***	***Gain (dB)***
Worst	SSF	125	14	16.2	385	16.9
Typical	TT	70	18.2	18.9	415	21.1
Best	FF	40	19.4	19.9	456	23.5

4.7.2. Monte Carlo statistical simulation

Monte Carlo statistical simulation is, in its essence, a batch of single run simulations. Each one of those simulations is set in a random fabrication corner. In this way, it is possible to observe the tendency of operation of the designed circuit for a large amount of samples. Differently from the PVT analysis that assists in operation extremes, Monte Carlo is a representation of long-term manufacturing performance, scalable throughout the process: it represents lot to lot, wafer to wafer or chip to chip variations. This is because of global and mismatch variations. Global variations are a set of parameters that affect device performance over manufacturing window while mismatch variations are those that generate device differentiation in a batch. Differently from PVT analysis, Monte Carlo is computational costly, as it demands a large sample group. This is why the Monte Carlo analysis was run only in one power mode and in a schematic only simulation for this work.

The power mode “111”of this work was submitted to a Monte Carlo simulation with a batch of 300 simulations. In TABLE 12 the obtained results for a schematic-only simulation are presented. Target values were obtained from a previous batch of 100 Monte Carlo simulation. Each range was obtained from the mean value ± 2 σ deviations. The results showed a batch yield of 86 %, meaning that 258 samples pass all the imposed targets. It is important to observe that the remaining 42 samples are not “bad” samples or “fabrication waste” – they just do not comply with the “pass” criteria. If the pass criteria were more elastic, the batch yield certainly would be higher. Stricter pass criteria are used to filter samples that operate in a controlled region of operation, and thus, guarantees the consumer a uniform application for the circuit. Column “Yield (%)” shows the individual yield of each simulated parameter. This means that, for example, 97 % of the tested devices “pass” the OCP_{1dB} target range.

TABLE 12 – Monte Carlo statistical simulation results for mode “111” for a batch of 300 simuations. Batch yield presented 86 % pass, meaning that 258 samples comply integrally with the imposed targets. The presented results are schematic only simulation.

Power mode	111	***Batch size***	**300**	*Batch yield (%)*		86
Obtained values	***Yield (%)***	***Minimum***	***Target***	***Maximum***	***Mean***	***Std Dev***
OCP_{1dB} (dBm)	97	14.99	17.74 to 20.44	20	19.08	649m
P_{SAT} (dBm)	96	14.86	16.49 to 20.35	20.62	-11.52	877m
Peak PAE (%)	96	22.85	27.37 to 34.49	34.77	30.82	1.87
PAE @ OCP_{1dB} (%)	95	15.9	20.05 to 27.09	26.8	23.49	1.69
Peak Gain (dB)	94	26.26	27.48 to 31.46	32.73	29.27	1.03
Peak P_{DC} (mW)	96	217.1	289.32 to 522.48	554.6	406.1	55.19m
P_{DC} @ OCP_{1dB} (mW)	96	187.5	251.98 to 446.22	477.5	348.9	45.11m

4.8. SIMULATED STANDARDS COMPLIANCE RESULTS

The post-layout simulation results of four different standards, 802.15.4, 802.15.4g, 802.11n, and LTE are presented in this section. The simulator used was Spectre RF version 15.1 running an envelope analysis in wireless mode, an automated simulation flow for modulated sources. In order to obtain the simulated results, the PA was set to operate in the highest power mode, the digital modulation source output power was set to -2 dBm and its SNR to 62 dB. The -2 dBm was chosen due to this value being the ICP_{1dB}, and thus, the PA operation is boundary non-linear. The SNR value, in its turn, is based on the assumption that noise added by mixer, I-Q modulator and LPF are negligible – thus, the available SNR is due only to the DAC. In order to obtain 62 dB, the SNR relation for a 10 bits ideal converter was employed and rounded up.

4.8.1. 802.15.4

FIGURE 52 presents the reference (filled red circles) and simulated (blue circles) symbols for 802.15.4 standard operating under O-QPSK PHY and transmitting 1280 chips at 2 M chips/s and channel number 11 (carrier frequency at 2405 MHz). The EVM is 0.35 %, 34.65 percentage points lower than the maximum allowed EVM (35 %). FIGURE 53 presents the spectral mask (wider blue trace) and the output power (red trace) of the PA over a 12 MHz bandwidth for a 2405 MHz carrier. The simulated main channel power is 18.73 dBm (the large signal simulation

returned 18.2 dBm as P_{OUT} for the same P_{IN}), the ACPR at -5 MHz is -35.71 dBc and at 5 MHz is -35.67 dBc. As the P_{OUT} of the PA is lower than the spectral mask, the PA complies with the standard.

FIGURE 52 – Reference (filled red circles) and simulated (blue circles) constellation for PA operating under 802.15.4 standard.

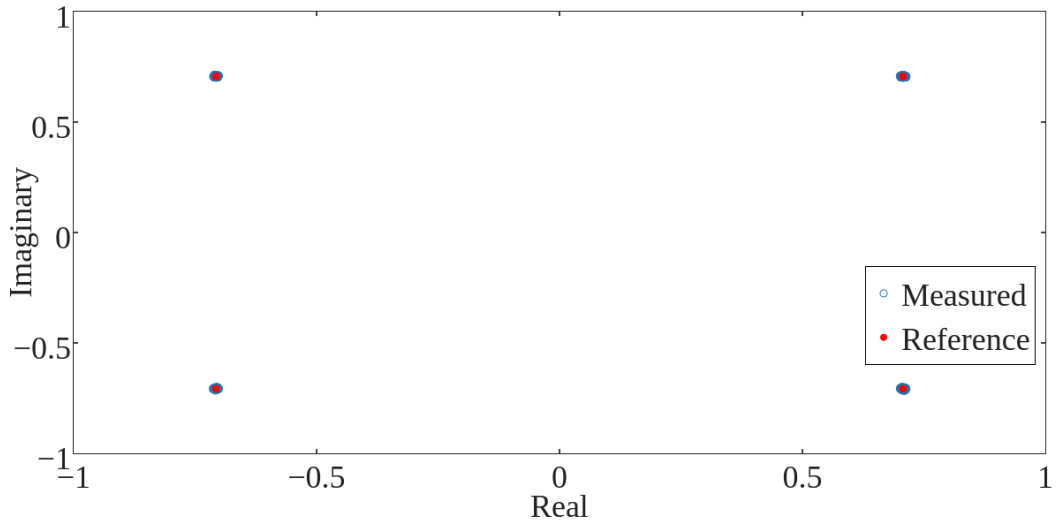
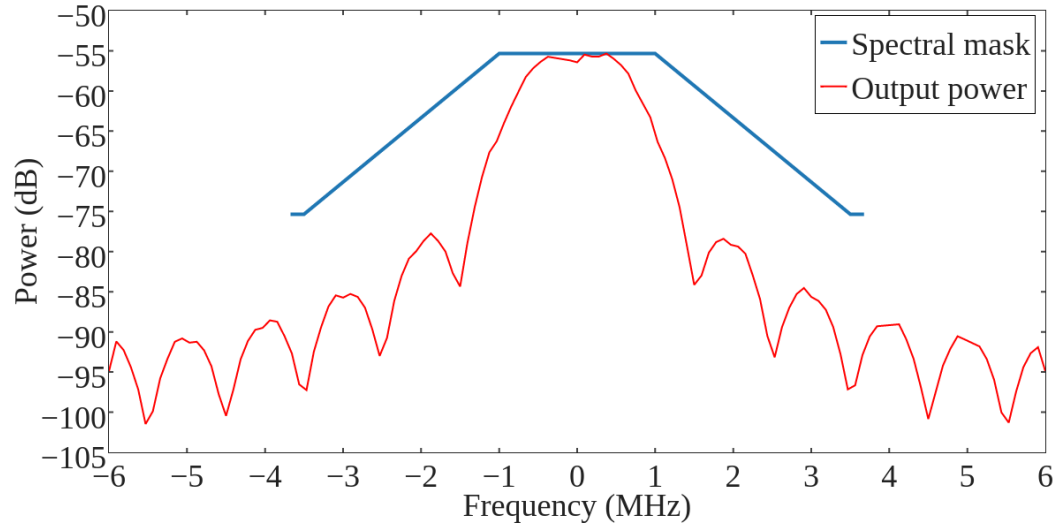


FIGURE 53 – Spectral mask (wider blue trace) and simulated PA P_{OUT} (red trace) under 802.15.4 standard operation.



4.8.2. 802.15.4g

FIGURE 54 presents the reference (filled red circles) and simulated (blue circles) symbols for 802.15.4g standard operating under O-QPSK PHY and transmitting 1280 chips and channel number 0 (carrier frequency at 2405 MHz). The obtained EVM is 0.19 %, 34.81 percentage points lower than the maximum allowed EVM (35 %). FIGURE 55 presents the spectral mask (wider blue trace) and the P_{OUT} (red trace) of the PA over a 16 MHz bandwidth for a 2405 MHz carrier. The main channel

power obtained is 18.7 dBm (the large signal simulation returned 18.2 dBm as P_{OUT} for the same P_{IN}), the ACPR at -5 MHz is -37.31 dBc and at 5 MHz is -37.48 dBc. As the P_{OUT} of the PA is lower than the spectral mask, the PA complies with the standard.

FIGURE 54 – Reference (filled red circles) and simulated (blue circles) constellation for PA operating under 802.15.4g standard.

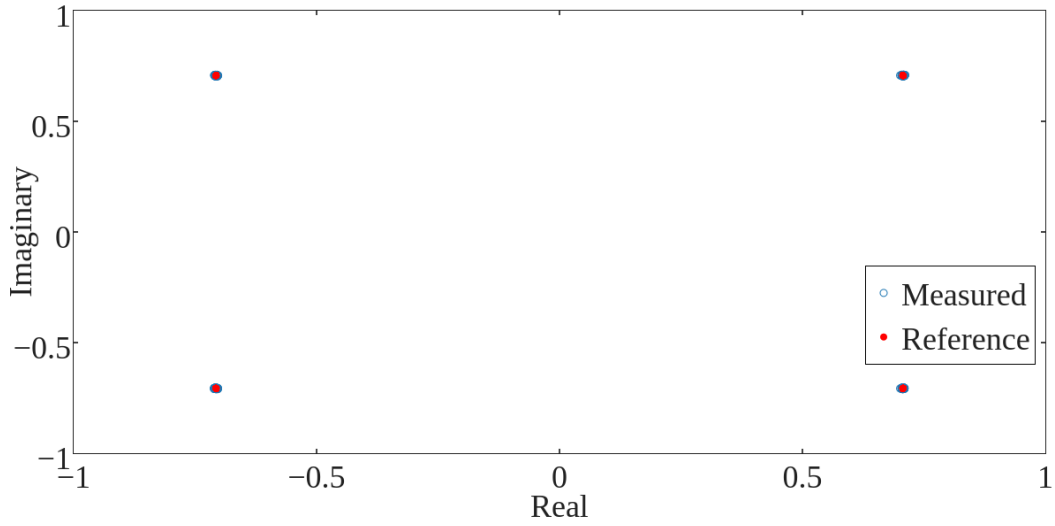
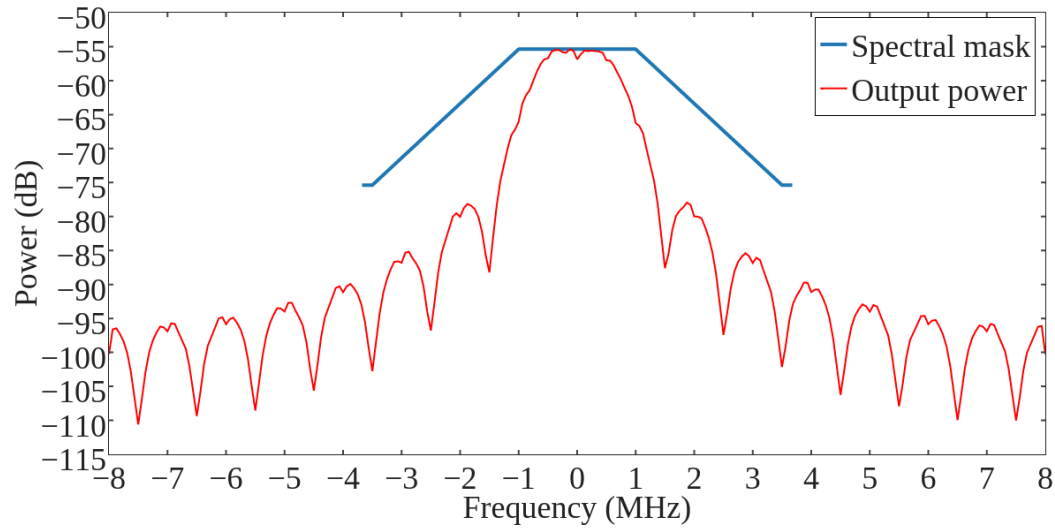


FIGURE 55 – Spectral mask (wider blue line) and simulated PA P_{OUT} (red line) under 802.15.4g standard operation.



4.8.3. 802.11n

FIGURE 56 presents the reference (filled red circles) and simulated (blue circles) symbols for 802.15.4g standard operating under MIX PHY (Legacy and Green devices are communicable), 20 MHz bandwidth, long guard interval and transmitting 1120 chips at channel number 1 (carrier frequency at 2412 MHz). The obtained EVM is -12.14 dB, 15.86 dB higher than the maximum allowed EVM

(-28 dB). FIGURE 57 presents the spectral mask (wider blue trace) and the P_{OUT} (red trace) of the PA over an 80 MHz bandwidth for a 2412 MHz carrier. The main channel power obtained is 17.29 dBm (the large signal simulation returned 18.2 dBm as P_{OUT} for the same P_{IN}), the ACPR at -20 MHz is -19.49 dBc and at 20 MHz is -19.64 dBc. The P_{OUT} of the PA is lower than the spectral mask up to |11| MHz, thus, the high-power mode of the PA does not comply with the standard for -2 dBm P_{IN}.

FIGURE 56 – Reference (filled red circles) and simulated (blue circles) constellation for PA operating under 802.11n standard.

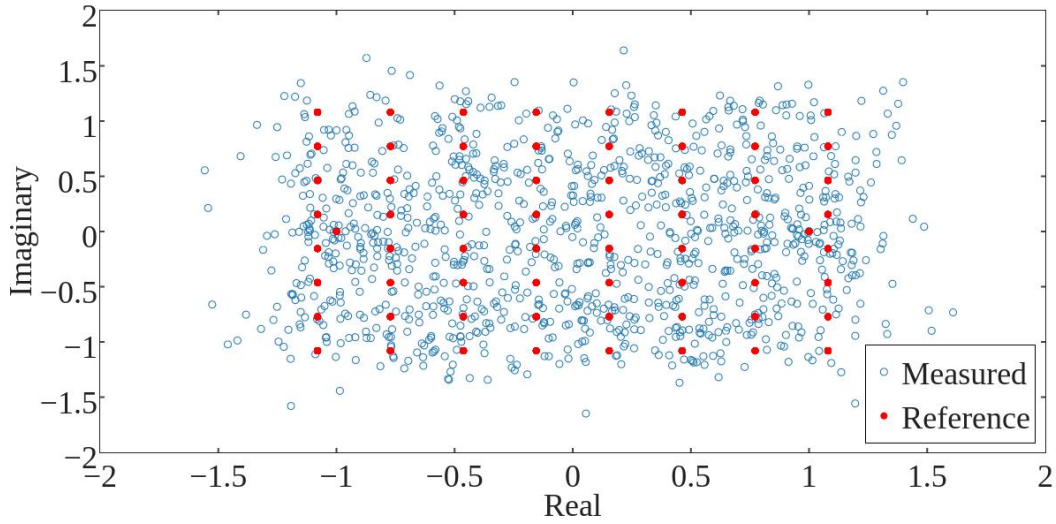
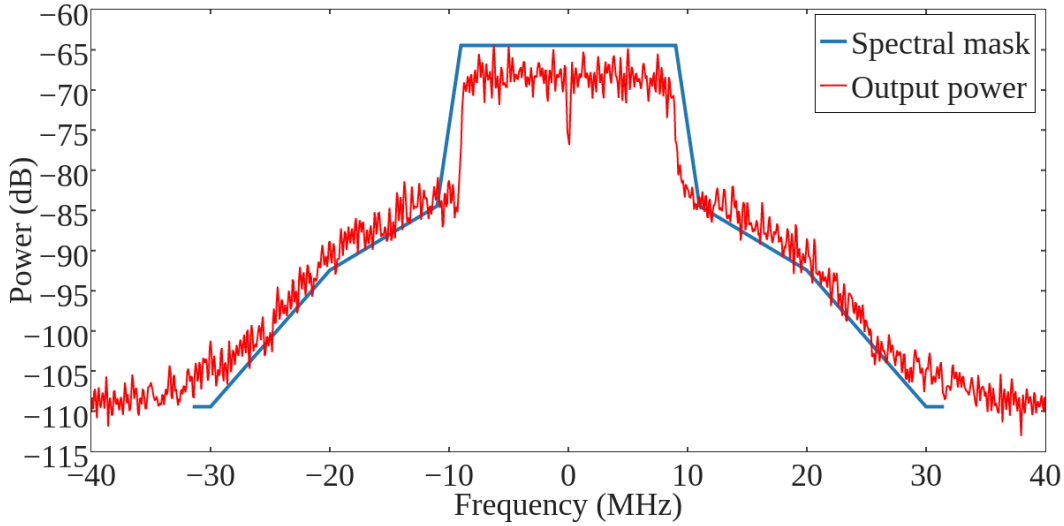


FIGURE 57 – Spectral mask (wider blue line) and simulated PA P_{OUT} (red line) under 802.11n standard operation.



4.8.4. LTE

FIGURE 58 presents the reference (filled red circles) and simulated (blue circles) symbols for LTE standard operating under QPSK PHY, 5 MHz bandwidth and transmitting 3600 chips at operating band 30 and channel 27710 (carrier frequency at 2310 MHz). The EVM is 16.56 %, 0.94 percentage points lower than the maximum

allowed EVM (17.5 %). FIGURE 59 presents the spectral mask (wider blue trace) and the P_{OUT} (red trace) of the PA over a 120 MHz bandwidth for a 2410 MHz carrier. The main channel power obtained is 18.46 dBm (the large signal simulation returned 18.2 dBm as P_{OUT} for the same P_{IN}), the ACPR at -5 MHz is -20.74 dBc and at 5 MHz is -20.46 dBc. The P_{OUT} of the PA is lower than the spectral mask up to |3.5| MHz, thus, the high-power mode of the PA does not comply with the standard for -2 dBm P_{IN}.

FIGURE 58 – Reference (full red dots) and simulated (hollow blue dots) constellation for PA operating under LTE standard operation.

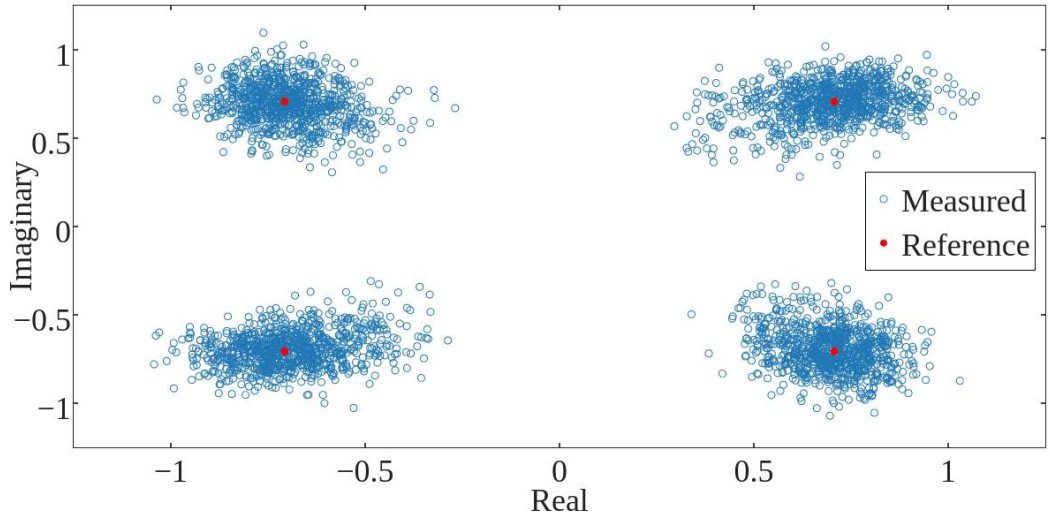
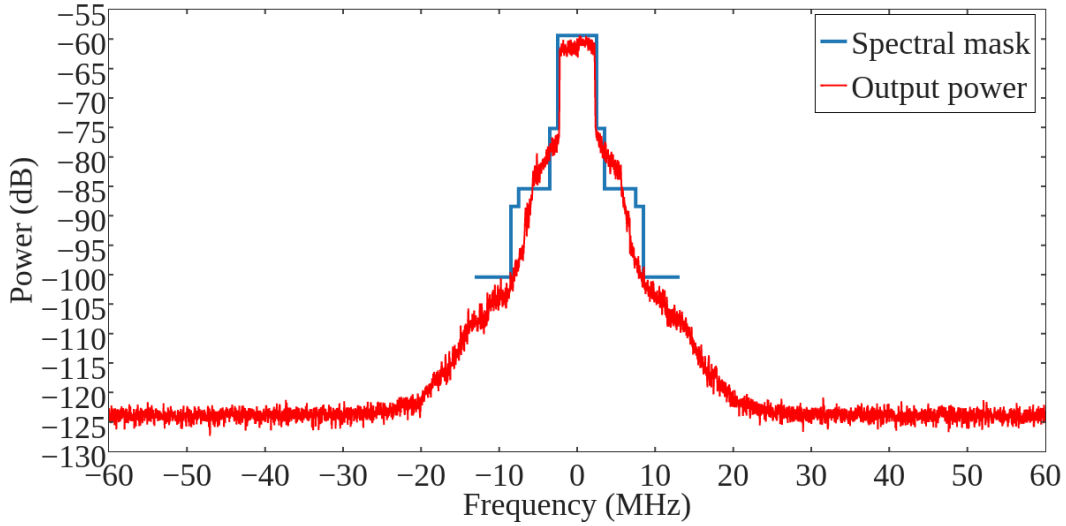


FIGURE 59 – Spectral mask (wider blue line) and simulated PA P_{OUT} (red line) under LTE standard operation.



5 FINAL CONSIDERATIONS

This work presented the design, implementation and characterization of a linear, fully integrated, two-stage low power 2.4 GHz output power programmable CMOS PA using *GlobalFoundries* 130 nm process. The general architecture is based on a fixed gain stage and a programmable power stage. The programmable power stage is composed of power cells and a cell selector. The power cells are three differently sized parallel cascode amplifiers. The cell selector is the common gate transistor of each cascode structure. By applying high logic to the gate of the common gate transistor in the cascode structure, local amplification is enabled. On the contrary, by applying low logic to the gate of common gate transistor, local amplification is disabled. By selecting which cell will be enabled or disabled independently, seven univocal power modes are achievable.

The design of the PA consisted on comprehending what is a PA and where it is situated in a transceiver system; on the impact the PA has on the power usage in the transmitter chain and how modern standards and consumer requirements demand low power solutions; on what are the benefits and challenges on using CMOS technology for power RF design; on what the employed technology affects the implementation of this work and on what metrics should be used to characterize such sub-system.

The implementation, in its turn, presented a literature review of recent output power reconfigurable PA architectures; presented the building blocks of the proposed PA and its schematic view; determined which metrics are used to analyze the performance of the amplifier and how it was laid out.

Finally, characterization presented the post-layout results and preliminary physical measurements and their comparison; evaluated some considerations on elucidating the discrepancies between post-layout and measurement results; performed a PVT and Monte Carlo analysis to determine operation extremes and production batch operation tendency and determined which standards the PA complies.

During characterization, measured results performed well below expected, being measured “111” mode between post-layout “001” and “010” modes. Post-layout results performed close to state of art. The lowest power mode achieves an 8.1 dBm P_{SAT}, a 13.5 dB power gain and consumes P_{DC} = 171 mW at an OCP_{1dB} of

6 dBm, whereas the highest power mode reaches an 18.9 dBm P_{SAT} a 21.1 dB power gain and consumes P_{DC} = 415 mW at an OCP_{1dB} of 18.2 dBm.

This work branched into two papers and several documents and presentations.

5.1. PERSPECTIVES FOR FUTURE WORK

Perspectives for future work are:

a) To measure remaining power modes;
b) To discover which parameters during circuit design and layout caused the difference between post-layout and measured results;
c) To characterize remaining power modes using digital channel metrics;
d) To run post-layout Monte Carlo simulations;
e) To evaluate the effect of wirebond and pin package on the IC;
f) Explore other possibilities employing the PA's output power.

6 SCIENTIFIC PRODUCTION

- F. Santos, A. Mariano, B. Leite, "2.4 GHz CMOS Digitally Programmable Power Amplifier for Power Back-off Operation", *7th Latin American Symposium on Circuits & Systems (LASCAS)*, Florianópolis.
- F. Santos, A. Mariano, B. Leite, "PVT Analysis of a 2.4 GHz 19.9 dBm Fully Integrated CMOS Power Amplifier with 23.5 dB Gain", *XXII Iberchip Workshop*, Florianópolis.

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